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Simulation of High k dielectric MOS with Hfo_2 as a gate dielectric

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Abstract- *Conventional MOS over 40years has been fabricated using Silicon substrate with polysilicon in gate material. As scaling of SiO_2 increases, a serious issue in terms of tunneling current and oxide breakdown raises. To overcome of these problems, silicon based MOS with High-k dielectric material in gate is becoming a strong alternative for replacing the conventional SiO2 dielectrics gates MOSFETs. High-k oxides provide a solution to leakage problems and improve performance such types of MOS can be used in both application of high performance and low power consumption. In this paper, HFO_2 based high k dielectric gate is used for the formation of device because HFO_2 is having high dielectric constant value and improves the performance of the device. On the basis of some electrical parameters, a comparative study in between conventional MOS and High k dielectric MOS is also presented.*

Keywords: High k material, Hfo_2, Leakage current, power consumption, output resistance, gate oxide.

1. Introduction:

The National Technology Roadmap of semiconductor (NTRS) and ITRS having scaling predication from 100 components per IC in 1965 to 15 billion in the current state. There are less gain in device performance i.e. power Consumption, short channel effects and parasitic capacitance as scaling goes further below sub-100 nm. In 2007, the use of high-k dielectrics [6] is first time introduced, to show gate leakage issues.

High K dielectric devices have applications in low power dissipation, low leakage current and high performance over conventional MOS. Basic difference in structure of conventional MOS over high k dielectric device is gate material. The materials used for the conventional MOS is SiO_2 but in high K dielectric based device gate material can be HFO_2, Al_2O3, Y_2O_3, La_2O_3, Sc_2O_3 [7]. For further downward scaling, dielectric having a higher dielectric constant will be the solution for achieving the same transistor performance while maintaining a relatively thick physical thickness [6].

Table: 1 Electrical properties of high k material [5-6].

Gate dielectric Material	Dielectric constant (k)	Energy band gap Eg (eV)	Applications
SiO_2	3.9	9	Passivation
Al_2O_3	8	8.8	High channel mobility
TiO_2	80	3.5	Low leakage current up to 1 nA/ cm^2
ZrO_2	25	5.8	high-permittivity
HfO_2	35	5.7	Higher Breakdown voltage
Ta_2O5	25	6	high durability and stability to heat
Y_2O_3	13	6	effective mobility

As from above table, it can be seen that HFO_2 is having higher dielectric constant value and it is widely used material for the simulation of MOS device. In the below figure the schematic of high k dielectric based gate oxide is shown.

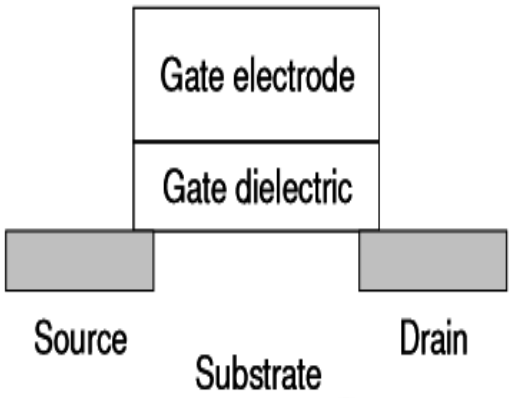

Fig.1 Schematic of high K dielectric based MOS [5].

Table: 2 Comparison of High K dielectric MOS with Conventional MOS [8].

Parameters	**Conventional MOS**	**High k dielectric material**
Leakage current	As the thickness decreases below 2 nm, leakage current increase drastically and leading to high power consumption problem and reduces device reliability.	Increased gate capacitance and reduced leakage effects.
Gate resistance	It is having higher gate resistance.	Metal gate has much lower gate resistance and desirable work
Mobility	Mobility of silicon based MOS was less which increases leakage current.	Effective mobility increased and leakage current decreased in the case of HfO_2.

As from above table 2, it is shown that conventional MOSFET have higher leakage current, offer high value of gate resistance and having less speed.

The used of high k-dielectric based material providing improvement in the performance of the device. Among the three main terminals of the MOS transistor – gate stack (Scaling of the gate stack is a key to enhancing the performance of complementary metal-oxide-semiconductor (CMOS), field-effect transistors (FETs) of past technology generations).Source/drain, and channel length; gate stack is most sophisticated and sensitive part for performance, yield and reliability [1]. Many alternate of high-k gate dielectrics have been studied to replace SiO_2.Among them, Hf-based oxides has been recently highlighted as the most suitable dielectric materials because of its comprehensive performance.

2. Evolution & Device Development:

1. The industry has employed oxy-nitride gate dielectrics since the 1990s, but in conventional silicon oxide dielectric is infused with the help of small amount of nitrogen. [2].

2. In early 2007, Intel has announced the deployment of hafnium-based high-k dielectrics with a metallic gate for components worked one the technology of 45 nanometer and has been used it in the 2007 processor series.[5]

3. In 2007, IBM also announced the transition to high-k materials, also hafnium-based, for some products in 2008.

4. NEC Electronics has also announced the use of an HfSiON dielectric in their 55 nm.

5. The 2006 ITRS roadmap predicted that the implementation of high-k materials to be commonplace in the industry by 2010[6].

3. Modeling and Simulation of HfO2 based MOSFET:

Fabrication process flow is:

1. Define silicon substrate.

2. Deposition of high k dielectric HFO2 in gate.

3. Partially etch out the high k material (HFO_2).

4. Formation of drain and source using ion implantation having phosphorous impurity.

5. Deposition of electrodes using aluminum material.

6. Deposition of tungsten material on HFO_2 layer for the formation of gate.

7. Deposition of low resistance material (aluminum) on the tungsten layer.

Step: 1 For <100> boron is used to doped silicon wafer, choose ADD region from Region menu and from right side window click on silicon material and select set base impurity.

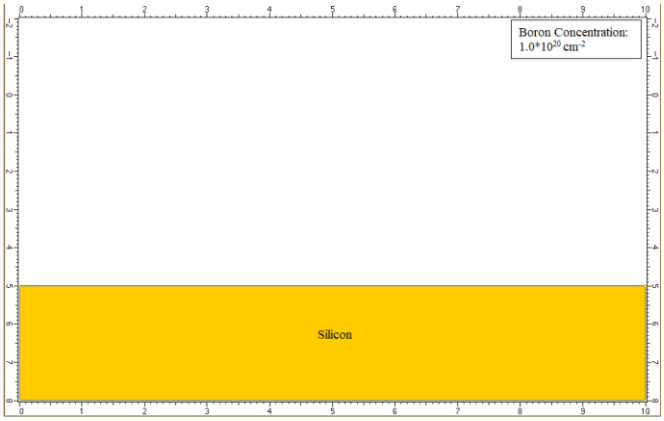

Fig.1 Deposition of silicon substrate.

Step: 2 $HFO_2$is thermally grown from the region menu, then from the Right window select materialHFO_2.

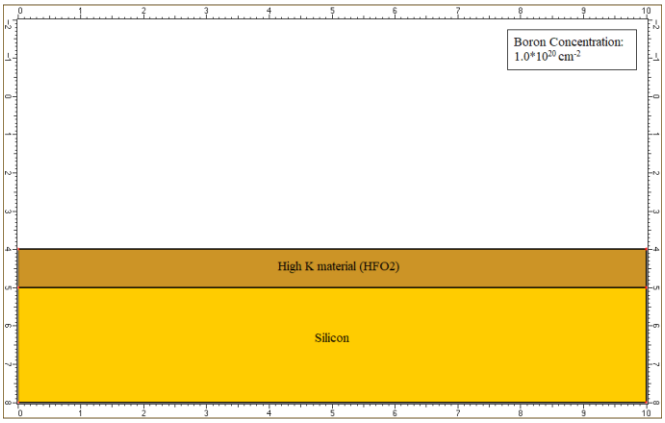

Fig.2 Deposition of high k-dielectric layer (HFO2).

Step: 3 HFO_2 is etched out first and etching of silicon substrate, for this chooses the region which will etch out and click on apply button.

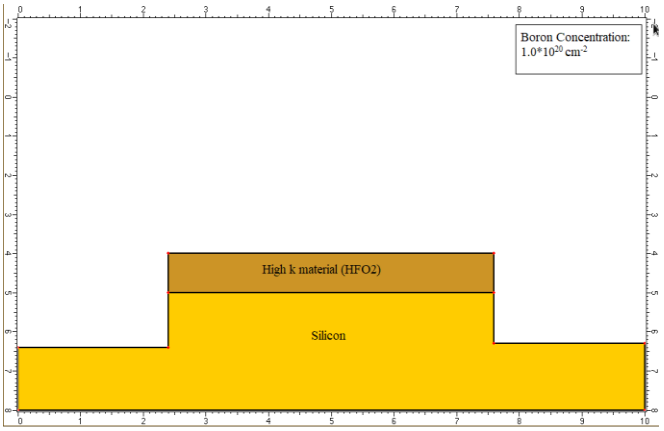

Fig.3 Etch out the extra material.

Step: 4 Drain and source is created using phosphorus impurity.

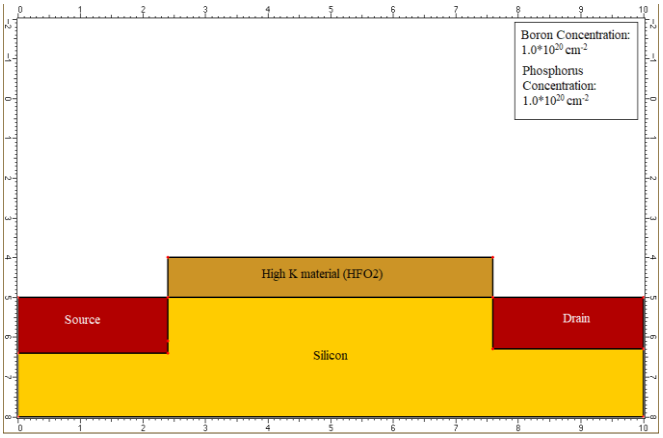

Fig.4 Drain and source is doped.

Step: 5 Aluminum materials are used for the formation of electrodes.

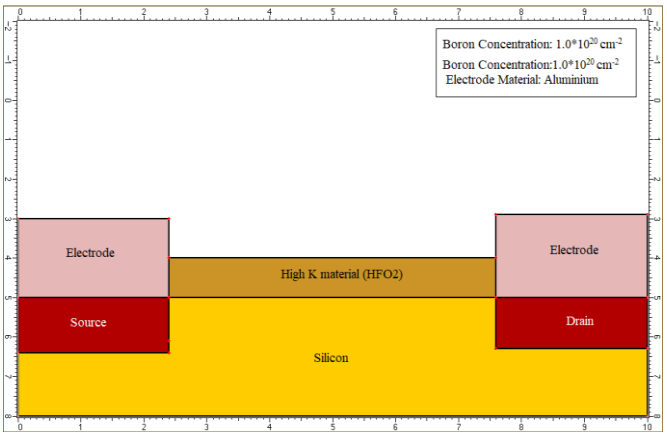

Fig.5 Electrodes are deposited

Step: 6 Gate is placed on the high k material using tungsten material.

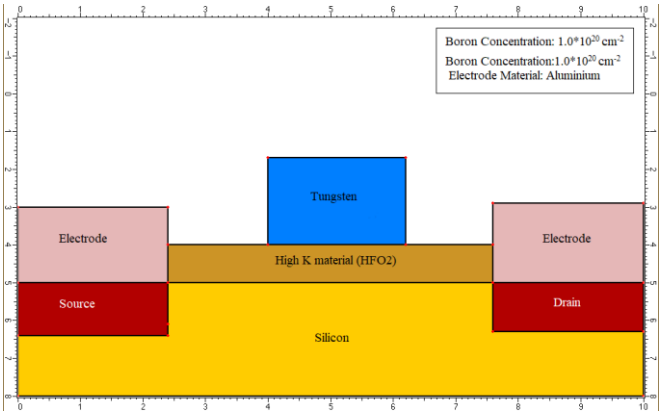

Fig 6.Making of gate

Step: 7 High k devices are ready by applying the low resistance metal layer on the gate.

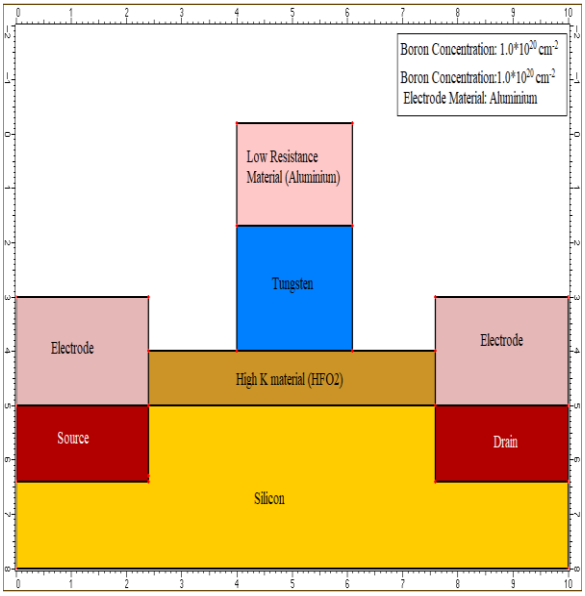

Fig.7 High k-dielectric based device.

IV. Software details:

Dr. Ivan Pasic founded Silvaco in 1984. Silvaco is an interactive tool. It has different parts such as Deck build, Tony plot, Maskview. Silvaco is used to provide analog semiconductor process, device and design automation solutions in CMOS. Among these interactive tools, Devedit is a tool of silvaco which is used for simulation of device, it will be used to either create a device by remesh or edit an existing device. It helps to create standard silvaco structure which can be easily integrated into 2D or 3D simulators of silvaco tool.

V. Conclusion:

When decreasing size of MOS technology it required the replacement of the SiO_2 with gate dielectrics material that have a high dielectric constant value (high-k). When the thickness of SiO2 is decreased below 1.4 nm then electron tunneling effects and high leakage currents will occur which causes a serious obstacles for device reliability. Therefore, MOSFET structure with high k dielectric is useful to improve electrical performance of the design.

VI. References:

[1]George James T, Saji Joseph and Vincent Mathew, "Effect of counter-doping thickness on Double-Gate MOSFET characteristics", Journal of Semiconductor Technology and Sciences, Vol.10, No. 2, pp. 130,132, June 2010.

[2] M. H. Chowdhury, M. A. Mannan and S. A. Mahmood, "High-k Dielectrics for Submicron MOSFET", IJETSE International Journal of Emerging Technologies in Sciences and Engineering, vol. 2, no. 2, pp. 8-10, July 2010.

[3] MaizanMuhammad, SunailyLokman, HaninHussin, "optimization in fabricating 90nm NMOS transistors using silvaco", IEEE student conference on research and development. pp. 2, 2009.

[4] L. Manchanda etal.,"High K Gate Dielectrics for the Silicon Industry," Ext. Abst.IWGI, pp.56-60, 2001.

[5] A. P. Huang1, Z. C. Yang and Paul K. Chu, "Hafnium-based High-k Gate Dielectrics", Advances in Solid State Circuits Technologies, Book edited by: Paul K. Chu, ISBN 978-953-307-086-5, pp. 446, April 2010.

[6] Prerna "Review Literature for Mosfet Devices Using High K", international journal for research in applied science, Vol.1IssueIV, November 2013.

[7] Saied Mohsenifar*, M. H. Shahrokhabadi,"Gate Stack High-κ Materials for Si-Based MOSFETs Past, Present, and Futures", Microelectronics and Solid State Electronics 2015, 4(1): 12-24.

[8] A thesis on "Preparation and Characterization of High-k Aluminum Oxide Thin Films by Atomic Layer Deposition for Gate Dielectric Applications", by Anu Philips, Chapter 1, 2010.