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FPGA IMPLEMENTATION OF EFFICIENT MUF GATE BASED MULTIPLIERS

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Abstract - *In recent years, the area of reversible logic grabs the interests of many researchers. There was certainly a need to reduce size and heat dissipation, hence the growth of VLSI technology made it alive. In 1961, Landauer stated that "losing a bit in digital circuits causes a smallest amount of heat dissipation". Reversible logic concepts hold a great applications in the field of Nano technology, signal processing etc, due to its ability to implement low power loss digital circuits. In this project, various conventional operations by this proposed gate is discussed. The main purpose of designing reversible logic is to decrease depth of the circuits. In reversible logic number of inputs and outputs must be equal. Here, MUF gate is used to analyze the Multipliers. This proposed gate will be simulated by Xilinx 12.3 ISE and implemented in the SPARTAN-FPGA.*

Key Words: Reversible, MUF gate, garbage, Xilinx, VHDL, etc.

1. INTRODUCTION

The most concerning issue in the design of very large scale integration is power consumption. Theoretically, zero internal power dissipation is achieved by reversible logic circuits as they do not lose information. In 1961, according to Landauer, smallest amount of heat dissipation in digital circuits' leads to losing of a one bit would be KTln2. Later in 1973, C.H.Bennet [4] showed that there will be no energy loss when the system is built using reversible logics. In low power CMOS VLSI design, a reversible circuit replaces irreversible circuits for a better performance. The reversible logic is designed mainly to reduce the number of garbage outputs, quantum cost and depth of the circuits. The one to one mapping between output and input vectors in this logic greatly helps in recovery of bit from loss.

1.1. LOGIC OF REVERSIBILITY

a. Reversibility:

The circuit is said to be reversible if, the reversible circuit must have equal no .of inputs and outputs[6] .The unique mapping should be there for each output pattern.

b. Garbage output:

The unused output that is left in the reversible circuit is called garbage output [4]. The greater performance can be achieved by lower values of garbage outputs.

c. Quantum costs:

It refers to the cost of the circuit in terms of the cost of a primitive gate. It is said that the quantum cost of 1*1 reversible gates is zero and the costs of 2*2 reversible gates is one [5].

d. Delay:

The delay in a logic circuit is defined by the maximum no. of gates occurring in the path joining the inputs and the outputs.

i. In a given circuit, one unit time is computed for any gate in all internal logic operations.
ii. The circuit gets all its input before the computation process takes place.

e. Power:

The sum of all the powers of each independent gate in the given logic circuit determines the total power of the circuit**.**

2. PROPOSAL AND REALIZATION OF REVERSIBLE MUF GATE

In this paper, a reversible MUF gate is proposed [5].The truth table clearly shows the unique pattern determined for input corresponding to its output, in the below gate, input vector I=(A,B, C) and output vector O=(P,Q,R).

The conventional digital gates can be designed by using reversible MUF gate. The operations like AND, NOT, NAND,NOR, EXOR, EXNOR, OR and COPYING can also be realized by this proposed gate.

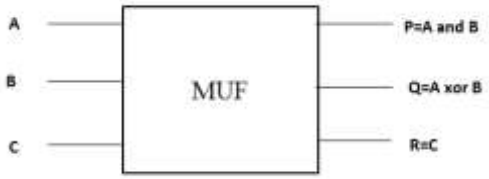

Fig -1: **Reversible MUF Gate**

2. PROPOSED DESIGN FOR REVERSIBLE 4-BIT MULTIPLIER

The fundamental and the most often used arithmetic operations in the high performance systems such as digital signal processing and Micro Processor etc., are addition and multiplication of binary numbers. Survey shows that 70% of all the instructions and algorithms perform addition and multiplication [2]. The execution time is dominated by these operations. Hence high speed multipliers play an important role in expanding computer and signal processing applications [1]. An important issue in multiplier design is power consumption. Reducing the number of operations reduces dynamic power which plays a major part of total power consumption. A good multiplier should provide high speed, reduced area and less heat dissipation [2].

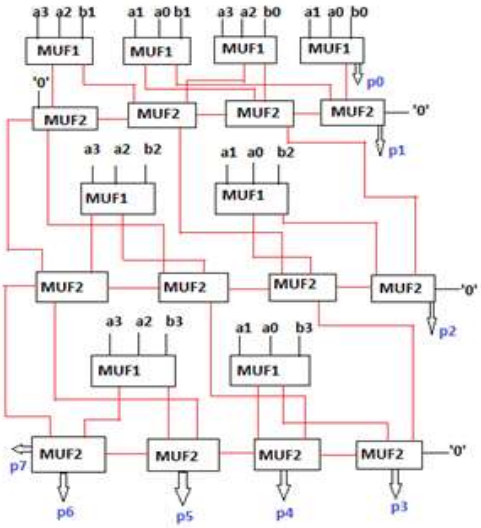

Fig -2: **MUF based Array Multiplier**

In the above proposed array multiplier, the conventional full adders were replaced by using reversible MUF Gate which results in the low power consumption [3].

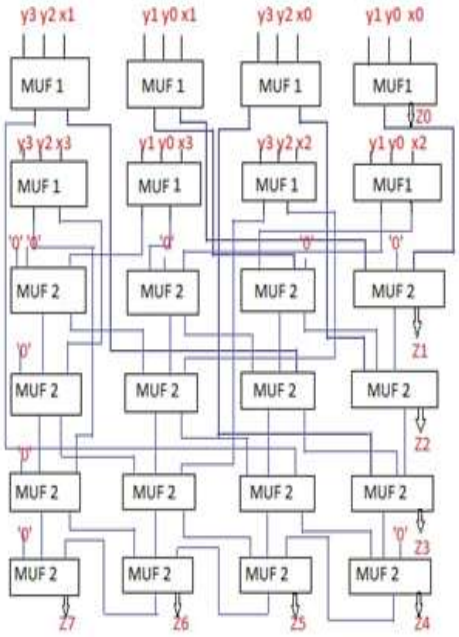

Fig-3: **MUF based Systolic Multiplier**

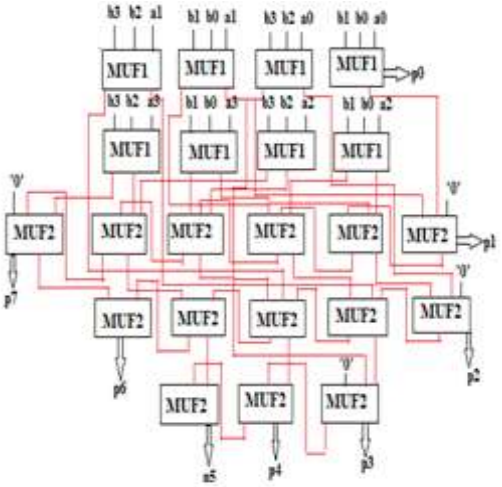

Fig-4: **MUF based Wallace Tree Multiplier**

3. COMPARISON RESULTS

The proposed MUF gate based Multipliers were compared with the existing multipliers in terms of area and delay.

EXISTING MULTIPLIERS	NO.OF.GATES	DELAY
Array Multiplier	28 gates AND – 16, FA-12	18.951ns
Wallace Multiplier	30 gates AND-16, FA-14	15.947ns
Systolic Multiplier	32 gates AND-16, FA-16	15.223ns
PROPOSED MUF BASED MULTIPLIERS	**NO.OF.GATES**	**DELAY**
Array Multiplier	20 gates	17.592ns
Wallace Multiplier	22 gates	15.747ns
Systolic Multiplier	24 gates	15.168ns

Table (a). Comparison of Existing and Proposed Multipliers

From the above table, it is clear that the Delay and Number of Gates were reduced in proposed MUF based multipliers. In terms of delay, proposed MUF based systolic multiplier has 19.96% and in case of number of gates MUF based array multiplier has 28.57% of efficiency when compared to their existing methods.

Fig- 5: Output of MUF based Wallace Tree Multiplier

Fig-6: Output of MUF based Systolic Multiplier

Fig-7: Output of MUF based Array Multiplier

5. CONCLUSION

This paper presents a method to reduce the area of Array Multiplier, Wallace Tree Multiplier and Systolic Multiplier. In the proposed architectures of these proposed multipliers uses a reversible MUF gate to reduce the area of Multiplier. These designs are simulated in Xilinx ISE 12.3i using VHDL language. The simulation results verify that the proposed multipliers, as expected, as the smallest area, low power consumption and high speed as compared to the Existing multipliers. As our future work, we plan to implement the designs using reversible MUF gate for higher-end multipliers to improve more efficiency that can be highly used in Nano Technology, DNA Computing, and Quantum Computing and in DSP Applications.

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