International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395-0056
Volume: 06 Issue: 04 | Apr 2019 www.irjet.net p-ISSN: 2395-0072

Review Paper on Radix-2 DIT Fast Fourier Transform using Reversible Gate

Sourabh Sharma[1], Prof. Gurpreet Singh[2]

[1]*Research Scholar, Trinity Institute of Technology & Research, Bhopal, India*
[2]*Faculty Electronics & Communication Dept., Trinity Institute of Technology & Research, Bhopal, India*

Abstract - *It is also a well-known fact that the multiplier unit forms an integral part of processor design, due to this, high speed digital processor architecture become the need of the day. In his paper a novel programmable FFT architecture for radix-2 DIT algorithm using reversible DKG gate is implementation.DKG gate is 4×4 reversible gate and working on both adder and sub-tractor. Recent advances in reversible logic using and quantum computer algorithms allow for improved computer architecture and arithmetic logic unit designs. The proposed design is synthesized using Xilinx ISE software and simulated using VHDL test bench.*

Key Words: Reversible Gates, Adder/ Sub tractor, Fast Fourier Transform, DKG Gate

1. INTRODUCTION

The Fourier Transform is an inevitable approach in signal processing [1], the Discrete Fourier Transform decomposes a set of values into different components of frequency. The Fast Fourier transform (FFT) is an appropriate technique to do manipulation of DFT. The algorithm of FFT was devised by Cooley and Tukey in order to decrease the amount of complexity with respect to time and computations [2].

The hardware of FFT can be implemented by two types of classifications- memory architecture and pipeline architecture. The memory architecture comprises a single processing element and various units of memory [3]. The merits of memory architecture include low power and low cost when compared to that of other styles. The specific demerits are greater latency and lower throughput. The above demerits of the memory architecture are totally eliminated by pipeline architecture at the expense of extra hardware in an acceptable way. The various types of pipeline architecture include Single delay feedback (SDF), Single delay commutator (SDC) and multiple delay commutators (MDC). The pipeline architecture is a regular structure which can be adopted by using hardware description language in an easy manner.

The algorithms of FFT can be grouped into fixed-radix, mixed-radix and split radix algorithms in a rough manner [5]. The basic categories of algorithms of FFT include - Decimation in-frequency (DIF) and the Decimation-in-time (DIT) as shown in Figure 1. Both of these algorithms depend on disintegration of transformation of an N-point sequence into many subsequences in a successive manner. There is no major difference between them as far as complexity of computation is concerned. Generally DIT deals with the input and output in reverse sequence and normal sequence respectively, while DIF deals with input and output in normal sequence and reverse sequence respectively. Only Decimation-in-Time (DIT) algorithm is taken into consideration. In this paper for implementation & result comparison, however DIT algorithm can also be use the proposed methodology.

In modern VLSI system power dissipation is very high due to rapid switching of internal signals. The complexity of VLSI circuits increases with each year due to packing more and more logic elements into smaller volumes. Hence power dissipation has become the main area of concern in VLSI design. Reversible logic has its basics from thermodynamics of information processing. According to this, traditional irreversible circuits generate heat due to the loss of information during computation. In order to avoid this information loss the conventional circuits are modeled using reversible logic. Landauer [1961] showed that the circuits designed using irreversible elements dissipate heat due to the loss of information bits [1]. It is proved that the loss of one bit of information results in dissipation of KT*log2 joules of heat energy where K is the Boltzmann constant and T is the temperature at which the operation is performed. Benett [1973] showed that this heat dissipation due to information loss can be avoided if the circuit is designed using reversible logic gates [2]. A gate is considered to be reversible only if for each and every input there is a unique output assignment. Hence there is a one to one mapping between the input and output vectors. A reversible logic gate is an n – input, n- output device indicating that it has same number of inputs and outputs.

Hence it is not possible to determine a unique input that resulted in the output zero. In order to make a gate reversible additional input and output lines are added so that a one to one mapping exists between the input and output. This prevents the loss of information that is main cause of power dissipation in irreversible circuits. The input that is added to an m x n function to make it reversible is known as constant input (CI). All the outputs of a reversible circuit need not be used in the circuit. Those outputs that are not used in the circuit is called as garbage output (GO). The number of garbage output for a particular reversible gate is not fixed.

2. LITERATURE REVIEW

Fahad Qureshi et al. [1], this paper presents a novel runtime-reconfigurable, mixed radix core for computation 2, 3, 4-point fast Fourier transforms (FFT). The proposed architecture is based on radix-3 Wingorad Fourier transform; however multiplication is performed by constant multiplication instead of general multiplier. The complexity is equal to multiplier-less 3-point FFT in terms of adders/subtractors with the exception of a few additional multiplexers. The proposed architecture supports all the FFT sizes which can be factorized into 2, 3, 4 point systems. We also show that the proposed architecture has the same bound on the accuracy as the classical one.

Fahad Qureshi et al. [2],this paper presents area-efficient building blocks for computing fast Fourier transform (FFT): multiplier-less processing elements to be used for computing of radix-3 and radix-5 butterflies and reconfigurable processing element supporting mixed radix-2/3/4/5 FFT algorithms. The proposed processing elements are based on Wingorad Fourier transform algorithm.

However, multiplication is performed by constant multiplier instead of a general complex-valued multiplier. The proposed process elements have potential use in both pipelined and memory based FFT architectures, where the non-power-of-two sizes are required. The results show that the proposed multiplier less processing elements reduces the significant hardware cost in terms of adders.

Shashidhara. K. S., et al. [3], Fast Fourier Transform (FFT) and Inverse Fast Fourier Transform (IFFT) is an integral part of Orthogonal Frequency division multiplexing (OFDM) systems. This forms the physical layer architecture of wireless systems and is designed to consume low power. This paper presents a low power and area efficient architecture for the FFT implementation. FFT involves more complex addition and multiplication operations. It is essential to reduce computational complexity of this FFT. Hence, the redundancy in intermediate stages of FFT is minimized in the proposed FFT architecture through decomposition techniques with reusable data approach. A common sub expression is identified to achieve reusability which leads to area and power efficient design. Also design is realized based on Multiplier-less arithmetic unit with retiming logic. FFT architecture is synthesized using Xilinx ISE Tool, and compared with the results so obtained with the Xilinx IP core 7.1. The power reduction, and area optimization is shown to be improved by 6% and 74% respectively.

LekshmiViswanath et al [4], reversible or information-lossless circuits have applications in digital signal processing, communication, computer graphics and cryptography. Reversibility plays an important role when energy efficient computations are considered. Reversible logic is used to reduce the power dissipation that occurs in classical circuits by preventing the loss of information. They propose a reversible design of a 16 bit BCD. This BCD consists of eight operations, three arithmetic and five logical operations. The arithmetic operations include addition, subtraction, multiplication and the logical operations include NAND, AND, OR, NOT and XOR. All the modules are being designed using the basic reversible gates. The power and delay analysis of the various sub modules is performed and a comparison with the traditional circuits is also carried out.

Akanksha Dixit et al [5], reversible logic has received great attention in the recent years due to its ability to reduce the power dissipation which is the main requirement in low power digital design. It has wide applications in advanced computing, low power design, Optical information processing,. Conventional digital circuits dissipate a significant amount of energy because bits of information are erased during the logic operations. Thus, if logic gates are designed such that the information bits are not destroyed, the power consumption can be reduced dramatically. The information bits are not lost in case of a reversible computation. This has led to the development of reversible gates. BCD is a fundamental building block of a central processing unit (CPU) in any computing system; reversible arithmetic unit has a high power optimization on the offer. By using suitable control logic to one of the input variables of parallel adder, various arithmetic operations can be realized.

3. REVERSIBLE GATES

Several reversible gates have come out in the recent years. The most basic reversible gate is the Feynman gate and is the only 2x2 reversible gates available and is commonly used for fan out purposes. The 3x3 reversible gates include Toffoli gate, Fredkin gate, new gate and Peres gate, all of which can be used to realize various Boolean functions.

BASIC REVERSIBLE GATES

Several reversible logic gates are used in previous design. In figure 1, show the block diagram of two input (A, B) and two output (P, Q) Feynman gate.

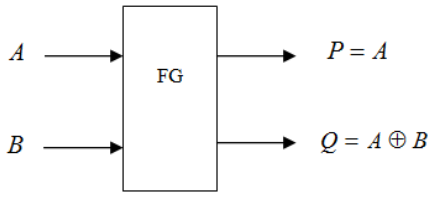

Fig -1: Feynman gate

In figure 2, show the block diagram of the three inputs (A, B, C) and three output (P, Q, R) Fredkin gate.

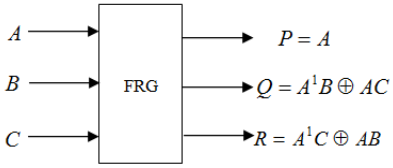

Fig -2: Fredkin gate

Figure 3 shows the Peres gate. A portion of the 4x4 doors are intended for executing some imperative combinational capacities notwithstanding the fundamental capacities. The

vast majority of the aforementioned entryways can be utilized as a part of the outline of reversible adders.

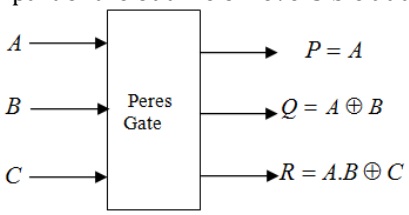

Fig -3: Peres gate

The HNG gate, presented in [10], produces the following logical output calculations:

$$P = A$$
$$Q = B$$
$$R = A \oplus B \oplus C$$
$$S = (A \oplus B).C \oplus (AB \oplus D)$$

The quantum cost and delay of the HNG is 6. At the point when D = 0, the consistent estimations created on the R and S yields are the required total and complete operations for a full snake. The quantum representation of the HNG is exhibited in Fig. 4.

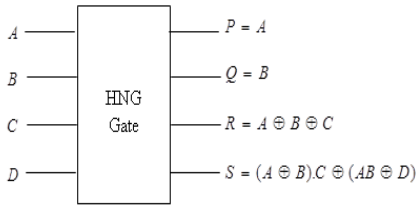

Fig -4: Block Diagram of the HNG Gate

A new programmable 4x4 reversible logic structure - Peres And-Or (PAOG) gate – is presented which produces outputs

$$P = A$$
$$Q = A \oplus B$$
$$R = AB \oplus C$$
$$S = (AB \oplus C).C \oplus ((A \oplus B) \oplus D)$$

Fig. 5 shows the block diagram of the PAOG gate. This gate is an extension of the Peres gate for ALU realization.

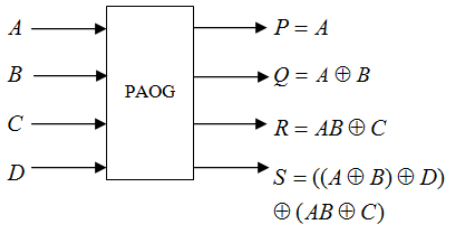

Fig -5: Block Diagram of the PAOG

Several 4x4 gates have been described in the literature targeting low cost and delay which may be implemented in a programmable manner to produce a high number of logical calculations. The DKG gate produces the following logical output calculations:

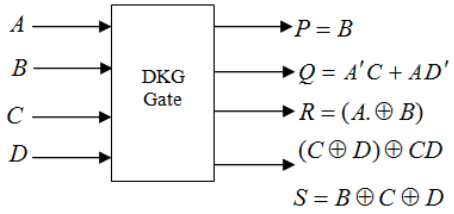

Fig -6: DKG Gate

$$P = B$$
$$Q = A'C + AD'$$
$$R = (A. \oplus B)(C \oplus D) \oplus CD$$
$$S = B \oplus C \oplus D$$

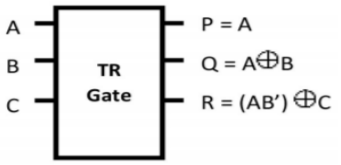

Fig -7: TR Gate

4. MULTIPLIER-LESS TECHNIQUE

The number of add operations required in a constant coefficient multiplication equal one less than the number of non-zero bits in the constant coefficient. In order to further reduce the area and delay consumption, the constant coefficient cab be encoded such that it contains the fewest number of nonzero bits, which can be accomplished using CSD representation.

An algorithm for computing the CSD format of a W-bit number is presented in.

Denote the two's complement representation of the number A as A = $\hat{a}_{W-1}, \hat{a}_W$ ..... $\hat{a}_1$and its CSD representation A = a_{W-1}, a_W..... a_1. The conversion is illustrated using the following iterative algorithm:

$$\hat{a}_{-1} = 0 \quad (3.13)$$
$$\gamma_{-1} = 0 \quad (3.14)$$
$$\hat{a}_W = \hat{a}_{W-1}$$

For (i=0 to W-1)

{

$$\theta_i = \hat{a}_i \oplus \hat{a}_{i-1}$$
$$\gamma_i = \overline{\gamma_{i-1}}\theta_i$$
$$a_i = (1 - 2\hat{a}_{i-1})\gamma_i$$

}

Here, the symbol ⊕ denotes XOR gate.

5. PROPOSED METHODOLOGY

DFT is a most important transform among the transforms that are widely used. The DFT is used to perform the Fourier

transform efficiently. The FFT algorithm is the most efficient and most preferred algorithm that is used in DFT computation. The FFT algorithm is preferred the most for DFT computation because of the need of less arithmetic resources when compared to that of the conventional method of DFT computation.

$$X(k) = \sum_{m=0}^{N-1} f(m) W_N^{km}$$

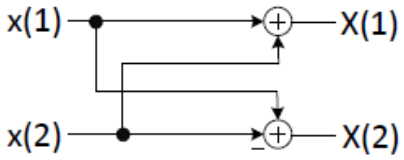

Fig -8: Radix-2 Butterfly

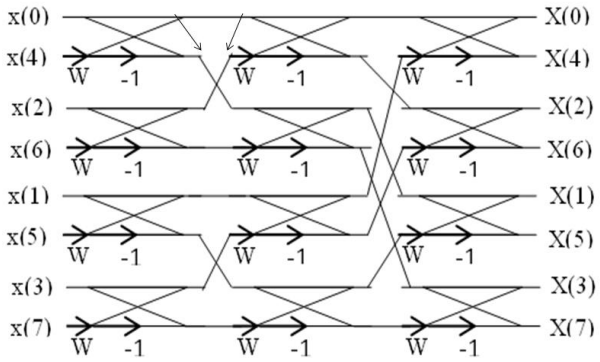

Fig -9: Flow Diagram of FFT using Multiplier-less Technique

6. SIMULATION RESULT

All the designing and experiment regarding algorithm that we have mentioned in this paper is being developed on Xilinx 6.2i updated version. Xilinx 6.2i has couple of the striking features such as low memory requirement, fast debugging, and low cost. The latest release of ISE™ (Integrated Software Environment) design tool provides the low memory requirement approximate 27 percentage low. ISE 6.2i that provides advanced tools like smart compile technology with better usage of their computing hardware provides faster timing closure and higher quality of results for a better time to designing solution.

6. CONCLUSIONS

The Fast Fourier transformation (FFT) is a frequently used Digital signal processing (DSP) algorithms for the applications of Orthogonal Frequency Division multiplexing (OFDM).

The performance evaluation of the various sub modules are carried out using Xilinx 14.1 ISE Simulator and it was found that the circuits designed using reversible logic showed a reduced delay and power. As a future work more arithmetic and logical function can be used.

REFERENCES

[1] Fahad Qureshi, JarmoTakala, Anastasia Volkova, Thibault Hilaire, "Multiplierless Unified Architecture for Mixed Radix-2/3/4 FFTs", 2017 25th European Signal Processing Conference (EUSIPCO), IEEE 2017.

[2] Fahad Qureshi, Muazam Ali, and JarmoTakala, "Multiplierless Reconfigurable Processing Elementfor Mixed Radix-2/3/4/5 FFTs", 978-1-5386-0446-5/17/$31.00 ©2017 IEEE.

[3] Ms. A. Anjana and Mrs. A.V Ananthalakshmi, "Design of Reversible 32-Bit BCD Add-Subtract Unit using Parallel Pipelined Method", International Conference on Advances in Electrical, Electronics, Information, Communication and Bio-Informatics (AEEICB16) 978-1-4673-9745-2 ©2016 IEEE.

[4] Matthew Morrison and NagarajanRanganathan, "Design of a Reversible ALU based on Novel Programmable Reversible Logic Gate Structures", 2015 IEEE Computer Society Annual Symposium on VLSI.

[5] LekshmiViswanath and Ponni.M, "Design and Analysis of 16 Bit Reversible ALU", ISSN: 2278-0661 Volume 1, Issue 1 (May-June 2014), PP 46-53.

[6] Akanksha Dixit and VinodKapse, "Arithmetic & Logic Unit (ALU) Design using Reversible Control Unit", International Journal of Engineering and Innovative Technology (IJEIT) Volume 1, Issue 6, June 2014.

[7] Mr. Abhishek Gupta, Mr. UtsavMalviya and Prof. VinodKapse, "Design of Speed, Energy and Power Efficient Reversible Logic Based Vedic ALU for Digital Processors", 2012 IEEE Computer Society Annual Symposium on VLSI.

[8] H. Thapliyal and N. Ranganathan, "Design of Efficient Reversible Binary Subtractors Based on A New Reversible Gate," Proc. of the I ComputerSociety Annual Symposium on VLSI, 2009.

[9] M. Morrison and N. Ranganathan, "Design of a Reversible ALU Based on Novel Programmable Reversible Logic Gate Structures," IEEE International Symposium on VLSI, 2011, pp. 126-131.

[10] M. Haghparast, S. J. Jassbi, K. Navi and O. Hashemipour, "Design of a NovelReversible Multiplier Circuit using HNG Gate in Nanotechnology", WorldApplied Sci. J., Vol. 3, , 2008, pp. 974-978.

[11] H. Thapliyal, N. Ranganathan, and R. Ferreira, "Design of a Comparator Tree Based on Reversible Logic," 10th Proceedings of the IEEE International Conference on Nanotechnology, 2010, pp 1113-6.

[12] P. Gupta, A. Agarwal, and N. K. Jha. An algorithm for synthesis of reversible logic ciruits. IEEE Trans. Computer-Aided Design, 25(11):2317–2330, Nov 2006.

[13] D. Maslov and G. W. Dueck. Reversible cascades with minimal garbage. IEEE Trans. Computer-Aided Design, 23(11):1497–1509, November 2004.