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Design of Area Efficient and Highly Reliable RHBD 10T Memory Cell for Aerospace Applications

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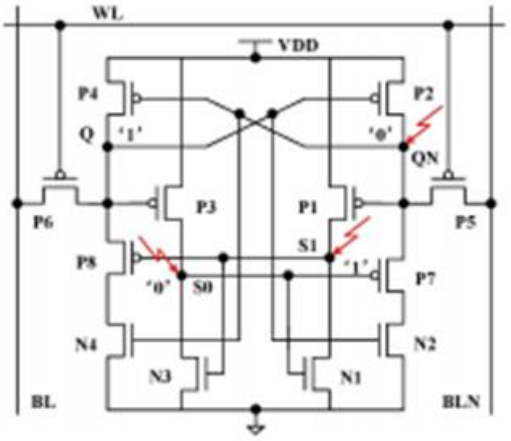
Abstract - *Based on upset physical mechanism together with reasonable transistor size, a robust 10T memory cell is first proposed to enhance the reliability level in aerospace radiation environment, while keeping the main advantages of small area, low power, and high stability. Using the TANNER EDA tool, simulations performed demonstrate the ability of the proposed radiation-hardened-by-design 10T cell to tolerate both 0 _ 1 and 1 _ 0 single node upsets, with the increased read/write access time. However, when considering the constraints of the target applications, compared with other hardened memory cells, the proposed RHBD 10T cell can be regarded as a good choice for aerospace applications as it provides a good balance among performance, area, power, and reliability for memories working at radiation environment.*

1.INTRODUCTION

In Aerospace applications, MEMORIES are the medium to store data, in which single event upsets (SEUs) are induced by radiation particles. They can conduce to the data corruption in a memory chip and the circuit itself is not permanently damaged, SEUs are also described as the soft errors. SEUs can cause a malfunctioning of an electronic system. Radiation hardening techniques for memories are one of the bottlenecks in providing fault tolerance. Some RHBD techniques have been used to tolerate soft errors in memories using standard commercial CMOS foundry processes, with no violation of design rules.

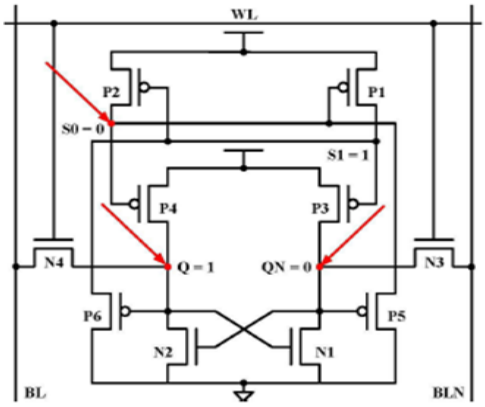
1.1 Existing 12T Cell:

An RHBD 12T memory cell is proposed at the cost of large area overhead. However, the common drawback of 11T, DICE, and 12T cells is that their area overheads are larger, which are not suitable. Hence, RHBD memory cells with both area-efficient and high reliability properties are required for Aerospace applications. In order to solve this contradiction, an area efficient RHBD 10T memory cell is proposed using a circuit-level hardening technique.It can provide high radiation hardening capability at the cost of write and read access times.

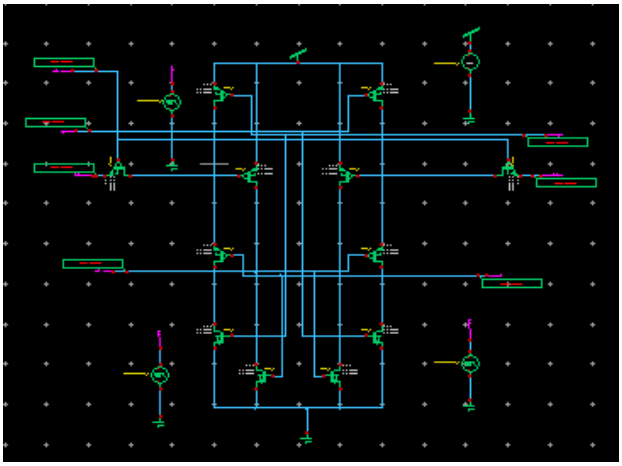


2. Proposed System:

The proposed RHBD 10T memory cell, Fig. 1 describes its basic schematic structure. From this figure, it can be seen that the proposed RHBD memory cell consists of ten transistors in which PMOS transistors are transistors (P1-P6), and the remaining transistors (N1-N4) are NMOS transistors. Both NMOS transistors N4 and N3 are defined as the access transistors, and their gates are connected with a word line (WL). Hence, when WL is in high mode (WL = 1), two access transistors are turned ON. At this moment, write/read operation can be implemented. The stored nodes are nodes Q, QN, S1, and S0 in which these four nodes are responsible for keeping the stored value correctly. In order to quickly transmit the digital signal to the output port during a read operation, a differential sense amplifier has to be employed and connected with two bit lines BL and BLN.

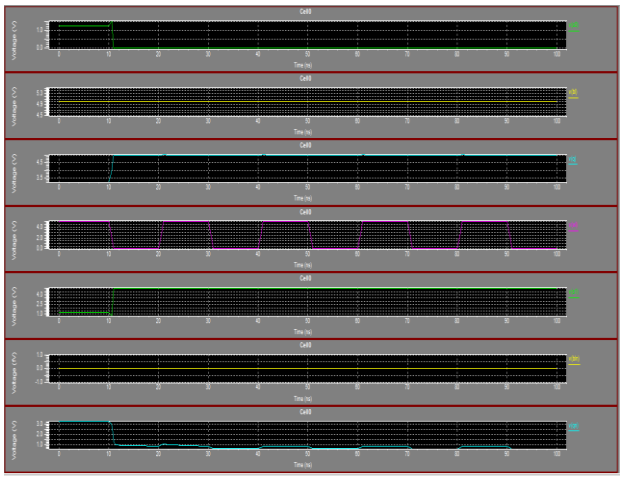


3. Implementation of Existing 12T RHBD:

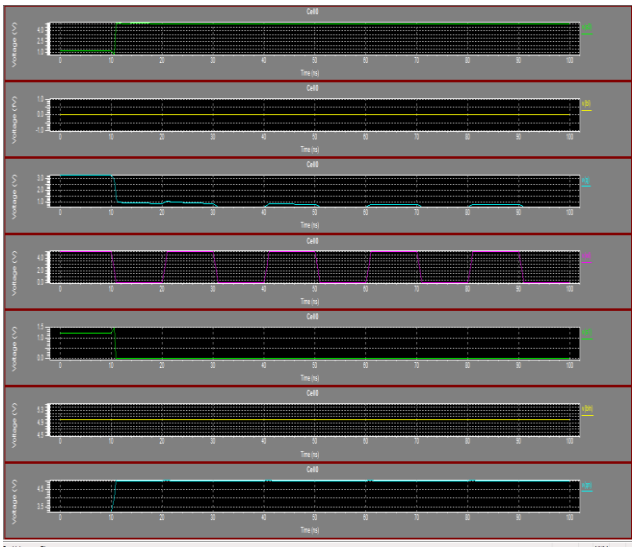


3.1 Outputs:

Considering **the stored 1 state** (i.e., QN = 0, Q = 1, S0 = 0, and S1 = 1) for the proposed RHBD 12T cell



To write data 0 into the proposed 12T cell, word-lineWL and bitline BL need to be 0 state, and bitline BLN must be 1 state. Subsequently, node Q will be pulled down to 0 state, and node QN will be pulled up to 1 state.



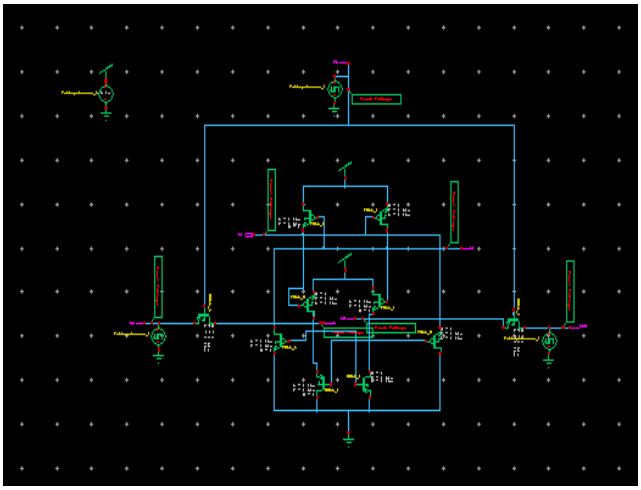
3.2 Timing Analysis:

```
Parsing                 0.01 seconds
Setup                   0.01 seconds
DC operating point      0.00 seconds
Transient Analysis      0.00 seconds
Overhead                0.99 seconds
-------------------------------------
Total                   1.01 seconds
```

3.3 Power Analysis:

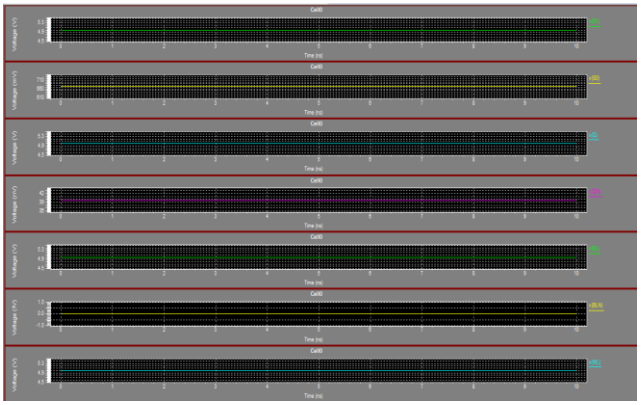
```
Power Results
Total Power from time 0 to 1e-009
Average power consumed -> 8.255343e-003 watts
```

4. Implementation of Proposed 10T RHBD :

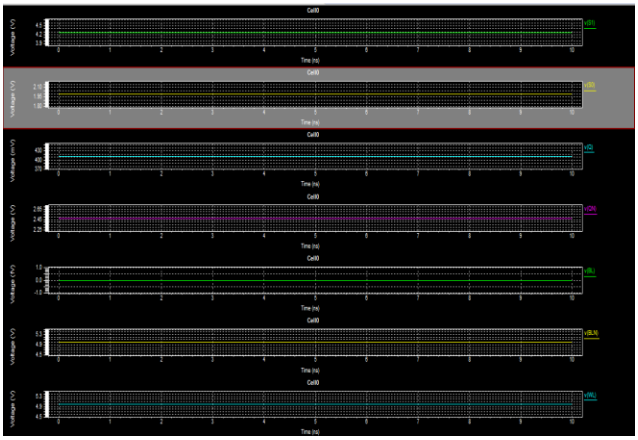


4.1 Outputs:

When BL = 1, BLN=0, Q=1, QN=0



When BL = 0, BLN=1, Q=0, QN=2.5v



4.2 Timing Analysis:

```
Parsing                          0.01 seconds
Setup                            0.01 seconds
DC operating point               0.05 seconds
Transient Analysis               0.00 seconds
Overhead                         0.06 seconds
-----------------------------------------------
Total                            0.13 seconds
```

4.3 Power Analysis:

```
Power Results
Total Power from time 0 to 1e-008
Average power consumed -> 1.460419e-002 watts
Max power 1.460419e-002 at time 0
Min power 1.460419e-002 at time 0
```

Radiation hardening is the act of making electronic components and systems resistant to damage or malfunctions caused by ionizing radiation. Such radiations are those encountered in outer space and high-altitude flight, around nuclear reactors and particle accelerators, or during nuclear accidents or nuclear warfare. Radiation-hardened components are based on their non-hardened equivalents, with some design and manufacturing variations that reduce the susceptibility to radiation damage. Due to the extensive development and testing required to produce a radiation-tolerant design of a microelectronic chip, radiation-hardened chips tend to lag behind the most recent developments.

5. Conclusion:

DESCRIPTION	TIMING ANALYSIS	POWER ANALYSIS
12 T RHBD	1.01s	8.255*e-003 watts
10T RHBD	0.13 s	1.4608* e -002 watts

A novel RHBD 10T cell in TANNER EDA tool, CMOS process is proposed in this brief. Compared with previous Hardened 10T memory cell, the proposed cell can recover an error in any one sensitive node. The simulation results presents that the penalty introduced for the proposed 10T cell is the increased write/read access time that may affect its applications with high speed requirements. However, when considering the constraints of the target applications, compared with other hardened memory cells the proposed RHBD 10T cell can be regarded as a good choice for Aerospace applications as it provides a good balance among performance, area, power and reliability for memories working at radiation environment.

6. References:

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