International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395-0056
Volume: 06 Issue: 03 | Mar 2019 www.irjet.net p-ISSN: 2395-0072

127 MULTILEVEL INVERTER

VIGNESH. S[1], RAM KUMAR. S[2]

[1]*PG Student, Department of Electrical and Electronics Engineering, Muthayammal Engineering College, Tamil Nadu, India*
[2]*Assistant Professor, Department of Electrical and Electronics Engineering, Muthayammal Engineering College, Tamil Nadu, India*

Abstract - *In recent years, high power apparatus are mostly used in industrial applications. Some utility applications and medium voltage motor drives requires megawatt power level and medium voltage. For a medium voltage grid, it is hard to connect only one power semiconductor switch openly. As a result, a multilevel power converter structure has been introduced as an option in medium voltage and high power situations. It also achieves high power ratings, and enables the use of renewable energy sources. Several multilevel converter topologies have been developed like seven levels, nine level etc., up to 72 levels by using different topologies. Here new topology was introduced. The simulation and implementation of this new topology through the 127 level inverter have been demonstrated. The modified PWM signal is generated to reduce the switching losses. Also, the proposed scheme can reduce the number of required power switches compared to a traditional multilevel inverter. A proto type model of 1 kW rating has been developed. The proposed scheme was simulated and discussed.*

Key Words: PWM, Cascaded, Hybrid, Multi level inverter, Harmonics, Bye pass diode

1. INTRODUCTION

Now a days, for and high-power medium voltage applications multilevel inverters (MLIs) are highly used in industries as an option of electronic power conversion. It reduces its respective harmonic content, the size of the filter used and the level of electromagnetic interference (EMI) generated by switching operation and also main function is improves the output waveforms. It is highly used in high power applications. In fussy, these include ability to synthesis voltage waveforms with lower harmonic content than two level converters and operation at higher DC voltages using series connected semiconductor switches. The desired output from an inverter is a sinusoidal waveform which is a continuous function of time. However, use of power switches to implement a static inverter results in output waveform composed of discrete values. In other words, the waveform has fast transitions (dv/dt) rather than smooth ones. In order to imitate a sinusoidal waveform, two (or three) level inverters use pulse-width modulation (PWM) operation with high switching frequency, so that the fundamental component of the output is sinusoidal. This also eliminates the lower order harmonics.

Apart from the issue of high switching losses due to high switching frequency, another issue that limits the feasibility of conventional two-level inverters for high-power high or medium–voltage applications is unavailability of high voltage/high power semiconductor switching devices. They are an attractive alternative to get better the output by synthesizing a staircase waveform imitate a sinusoidal waveform. That waveform has a low distortion, and also reduces the dv/dt stress.

Multilevel inverter topologies have the advantages of having better harmonic profile, overcoming voltage limit capability of semiconductor switches and also high voltage capability. Various multilevel inverter (MLI) structures are suggested but the cascaded MLI (CMLI) appears to be high used other than inverter topologies in application at high power rating due to its modular nature of modulation, control and protection requirements of each full bridge inverter (FBI).It gives high quality output voltages and input currents.Many of the modulation methods developed for MLI is based on multiple-carrier arrangements with pulse width modulation (PWM). The carriers can be arranged with vertical shifts or with horizontal displacements .Space-vector modulation (SVM) is also extensive for the MLI operation, it gives good harmonic performance.

The topological structure of multilevel inverter must cope with the points such as it should be capable of enduring very high input voltage such as HVDC transmission for high power applications. Each switching device should have lower switching frequency owing to multilevel approach. Various Topologies are implemented; common ones are diode-clamped, flying capacitor or multicell, cascaded H-bridge, and hybrid H-bridge multilevel. Some of the common problems identified in the conventional inverters are Such as Higher THD in output voltage; more switching stresses on switching devices, not applicable for high voltage applications, higher voltage levels are not produced

The proposed hybrid multilevel inverter use bye-pass diode and common H-bridge techniques to produce 31- voltage levels in the output of the inverter with overcoming all drawbacks in conventional inverter. The hybrid multilevel inverter is significantly advantageous over other topologies; it has less power switches ,less anti-parallel diodes, power diodes and less number of capacitors for same number of output voltage levels, Ability to reduce the voltage stress on each power device, Reduced electromagnetic compatibility

(EMC) when operated at high voltage, Lower EMI due to small output voltage steps, Smaller rating of semiconductor devices, Better feature in output voltage in terms of less distortion

This project recounts the development of a novel hybrid multilevel single phase inverter that has 8 power switches and 4 power diodes to produce 31-levels in the output voltage with incorporating all features listed above. The topology was applied to an induction motor and the performance of the inverter is studied using MATLAB/ SIMULINK. And the hardware prototype is developed for the verification of concept and the output results are clearly presented.

1.1 OBJECTIVE:

The main objectives of the project are:

- To reduce the number of power switches used with the help of new multilevel inverter topology.
- To study the performance of 31-level inverter with the help of MATLAB/SIMULINK.
- To reduce the Total Harmonic Distortion in the output of the inverter.

2. LITERATURE REVIEW

Jinn-Chang Wu(2010) has proposed a three-phase three-wire hybrid power filter configured by a three-phase passive power filter and a three-phase diode-clamped multi-level power converter with a small power capacity of zero-sequence current loop connected in series to compensate for the harmonic currents of non linear load. The salient feature is that a small power capacity of zero-sequence current loop is applied to overcome the problem of balancing voltages of two DC capacitors for a diode-clamped multi-level power converter applying in the three-phase three-wire hybrid power filter. A laboratory prototype is developed to verify the performance of the proposed three-phase three-wire hybrid power filter. The experimental results have demonstrated the feasibility and practicality of the proposed three-phase three-wire hybrid power filter. The main disadvantage of this method is high harmonic content in the output current i.e. THD is nearly 22% and more number of clamping diodes is used.

Mohamed Abbes et al (2012) have presented a new control strategy for the three-level, neutral point clamped (NPC), voltage source converter. The converter can be used in many high-power renewable energy systems such as direct drive wind turbines and hybrid generating units. The developed control algorithm proposes an improved solution to balance DC bus intermediate voltages using space vector modulation (SVM) techniques. It aims to guarantee fault ride-through (FRT) capabilities of renewable energy plants equipped with multilevel converters. Since the main attention of this paper is the grid side converter control, the energy generating system was simplified to an equivalent variable current source. The grid side converter is connected to the grid through an LCL filter. Two controllers are developed to achieve grid currents regulation. The control of DC bus voltage is achieved by PI-regulation. Performances of the two controllers and the improved modulation technique are compared and evaluated in terms of accordance with the grid connection requirements (GCR) including, low voltage ride-through capabilities, frequency variation and reactive power control. The main shortcoming of this system are12 switches are required for 3-level output itself.

Rabia Guedouani et al (2012) have proposed a control strategy of a three –phase five-level double converter for induction motor drives. The converter consists of the five-level NPC rectifier, DC link, and the five-level NPC inverter. In this control strategy, the DC link voltages are controlled by using a closed loop with an optimized stabilization system called clamping bridge. It provides a fast and flexible control of the converter capacitor voltage. This method will redress the imbalance of DC link voltage. This control strategy is completely independent from the load control, leading to a simpler implementation. The three-phase five-level NPC rectifier-inverter system is an ideal interface between a utility and renewable energy sources such as photovoltaic or wind generator. The main shortcoming of this system is addition of NPC rectifier block to input side of the inverter for balancing capacitor voltage. So the cost of the system is high.

Sakthivel Muragan (2009) has discussed about the transistor clamped inverter with the conventional diode clamped inverter. In this method the gate driver concept is introduced and this method is simple because only one switch is turned ON at a time. By utilizing this concept a eleven level multilevel inverter has been developed and the THD is found to be much less than the conventional method. The main shortcoming of this method is that, n number of gate driver circuits are required for n number output levels.

Jing Zhao (2011), has present multilevel circuit topologies based on switched-capacitor and diode-clamped converters (MCT-BSD). The topology structure and the operation principle, including the working states transitions of the diode-clamped part, the volt-ages balancing mechanism of the dc link capacitors, and the pulse width modulated carrier control strategy are presented. The switched-capacitor circuits contribute not only to balancing the voltages of capacitors but also to boosting the output voltage with a certain input dc voltage. The results show that balancing the voltages of capacitors, boosting the output voltages, and operating under the three-phase condition are all realized effectively in the MCT-BSD. In this method more number of

power switches and capacitor are used and the THD is around 13% these are major drawbacks of this method.

Miao Chang-xin et al (2010), have presented Flying capacitor multilevel inverters. In order to improve the harmonic performance of the output voltage under low modulation index region, the paper presents a novel PWM method for flying capacitor multilevel inverters based on the idea of controlling freedom degree. The novel PWM method can balance the flying capacitor voltage in a certain period. The validity of the novel PWM method is demonstrated by the experimental results. The proposed PWM method is efficient for five-level output only, as the number of output level increase the THD in the output also increase.

Jaison Mathew(2011), has present a multilevel inverter topology suitable for the generation of dodecagonal space vectors instead of hexagonal space vectors as in the case of conventional schemes. This feature eliminates all the 6n+1,(n=odd), harmonics from the phase voltage and current in the entire modulation range with an increase in the linear modulation range. The topology is realized by flying capacitor based three level inverters feeding from two ends of an open end winding induction motor with asymmetric dc links. The flying capacitor voltage is tightly controlled throughout the modulation range using redundant switching state for any load power factor. The main drawbacks of the system are control is complex; more number of freewheeling diodes are used.

Pengwei sun (2012), has present a new type of cascade inverter based on dual buck inverter with phase-shift control scheme. The proposed cascaded dual buck inverter with phase shift control inherits all the merits of dual buck type inverters and overcomes some of their drawbacks (i.e) improved system reliability. Here the phase-shift control and cascade topology reduce the ripple current or cut down the size of the passive components by increasing the equivalent switching frequency. Even though cascade topology solve the issue of zero crossing distortion by using phase shift control scheme the main drawback of this inverter we should turn on the switches based on the direction of the output current. Moreover when phase shifted PWM is fed to different cascade unit, current zero-crossing distortion is theoretically eliminated.

Thamizharasan (2012) has construct a new hybrid multilevel dc-link inverter (MLDCLI) topology with a focus to synthesize a higher quality sinusoidal output voltage. The idea emphasizes the need to reduce the switch count considerably and thereby claim its superiority over the existing multilevel inverter (MLI) configurations. The structure incorporates a new module along with a differently used H-bridge that facilitates the increase in levels with much lower switch counts. The proposed dual bridge MLDCLI (DBMLDCLI) is evaluated using phase disposition (PD) multi-carrier pulse width modulation (MC-PWM) strategy in a field programmable gate array (FPGA) platform. The MATLAB/System generator based simulation results validated through FPGA based prototype for a typical output level exhibit the drastic enhancement in the quality of output voltage. The total harmonic distortion (THD) obtained using a harmonic spectrum reveals the mitigation of the frequency components of output voltage other than the fundamental and paves the way to open a new avenue for nurturing innovative applications in this domain. The drawbacks of the system are THD is around 7.8% and 15 switches are used for 15-levels and the forward blocking voltage is low.

Himanshu Misra (2011), has discussed about the multilevel voltage source inverters using unique structure so it produce high output voltages with low harmonics without the use of transformers or series-connected synchronized switching devices. The inverter consists of eleven switches and five separate dc sources with a load to produce 11 level output voltage. In this method less number of switches is used compare to the conventional methods. The simulation of eleven level multilevel inverter is done with pulse width modulation technique. In this topology the switches in the upper leg have high voltage rating than the switches in the lower leg and the upper two batteries of the circuit are used for more number of times compare to other three batteries.

3. PROPOSED WORK

The proposed topology comprises bye-pass diode technique and common H-Bridge configuration to form hybrid multilevel inverter shown in Figure 1. The bye-pass diode technique is used to produce only positive voltage steps. In this technique a special circuit is employed i.e the power switches and the DC source are connected in series and the diodes are connected in parallel. To increase the number of voltage levels in the output a source, switch and diode is added to the byepass diode technique topology.

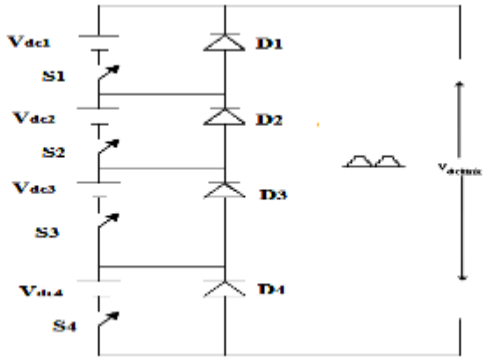

Figure 1 Byepass Diode Technique

The H-bridge circuit is used to produce both positive (Q_1, Q_3) and negative (Q_2, Q_4) waveform in the output. The common H-bridge configuration is shown in the above figure 2. This H-bridge circuit remains constant for any number of levels produced by byepass diode technique. The switches

(Q_1, Q_3) will conduct during the positive half cycle and the switches (Q_2, Q_4) will conduct during the negative half cycle.

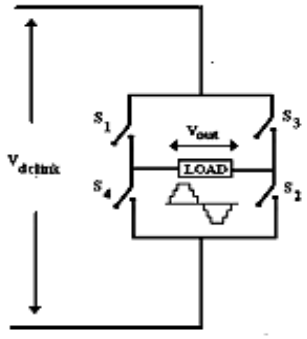

Figure 2 Common H-Bridge Configuration

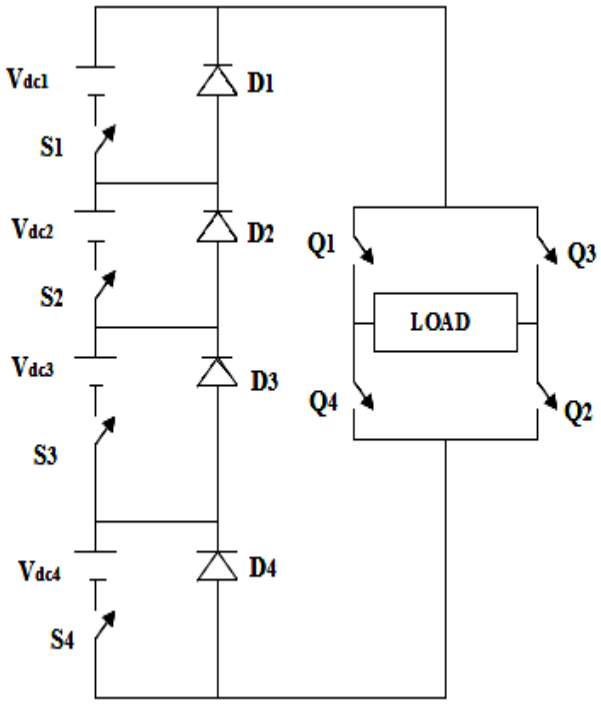

Figure 3 Proposed Circuit Diagram.

3. 1 VOLTAGE EQUATION OF INVERTER

The main advantage of modified hybrid multilevel inverter is high number of levels with reduced number of switches. The S number of dc source or stages and the associated number output level can be calculated by using the equation

$$N_{level} = 2^{s+1}\text{-}1 \qquad 3.1$$

For example if S=3, the output wave form has 15 levels (±7, ±6, ±5, ±4, ±3, ±2, ±1 and 0),

Voltage on each stage can be calculated by using the equation

$$V = 2^{s-1}.Vdc \qquad 3.2$$

The number switches used in this topology is given by the equation

$$N_{switch} = S+4 \qquad 3.3$$

3.2 SWITCHING SEQUENCE OF THE INVERTER

The switching order for each switch for the proposed hybrid multilevel inverter is shown in table 1. The zero level is common for both positive and negative set of cycles, i.e. zero state occur twice in a one cycle. To get positive half cycle switches are operated from I to XV(output voltage zero to peak voltage value) then the switches are operated from XV to I(peak voltage value to zero voltage) this process is repeated for negative half cycle. Here IGBT is used as a power switch for the inverter.

Table 1 Switching Table

S.NO	INTERVALS	ON SWITCHES	CURRENT FLOW	VOLTAGE LEVELS
1	I	S_1	$S_1D_4D_3D_2$	+1Vs
2	II	S_2	$S_2D_1D_4D_3$	+2Vs
3	III	S_1S_2	$S_1S_2D_4D_3$	+3Vs
4	IV	S_3	$S_3D_1D_2D_4$	+4Vs
5	V	S_1S_3	$S_1D_4S_3D_2$	+5Vs
6	VI	S_2S_3	$S_3S_2D_1D_4$	+6Vs
7	VII	$S_1S_2S_3$	$S_1S_2S_3D_4$	+7Vs
8	VIII	S_4	$S_4D_3D_2D_1$	+8Vs
9	IX	S_1S_4	$S_4D_3D_2S_1$	+9Vs
10	X	S_2S_4	$S_4D_3S_2D_1$	+10Vs
11	XI	$S_1S_2S_4$	$S_4D_3S_2S_1$	+11Vs
12	XII	S_3S_4	$S_4S_3D_2D_1$	+12Vs
13	XIII	$S_1S_3S_4$	$S_3D_2D_1D_4$	+13Vs
14	XIV	$S_2S_3S_4$	$S_4S_3S_2D_1$	+14Vs
15	XV	$S_1S_2S_3S_4$	$S_1S_2S_3S_4$	+15Vs
16	XVI	NIL	NIL	0

4. PERFORMANCE ANALYSIS

4.1 SIMULATION STUDIES

MATLAB (matrix laboratory) is a multi-paradigm numerical computing environment and proprietary programming language developed by Math Works. MATLAB allows matrix manipulations, plotting of functions and data, implementation of algorithms, creation of user interfaces, and interfacing with programs written in other languages, including C, C++, C#, Java, Fortran and Python. The results or output was taken for both Fuzzy and ANN. The outputs were compared and the better was taken down. The MATLAB/SIMULINK toolbox is mainly used.

4.2 SIMULATION RESULTS

4.2.1 SIMULATION OF 31-LEVEL SINGLE PHASE INVERTER

The simulation circuit of the proposed inverter which comprises 10 IGBT switches and 4 diodes for producing 31-output voltage levels is shown in the figure 4

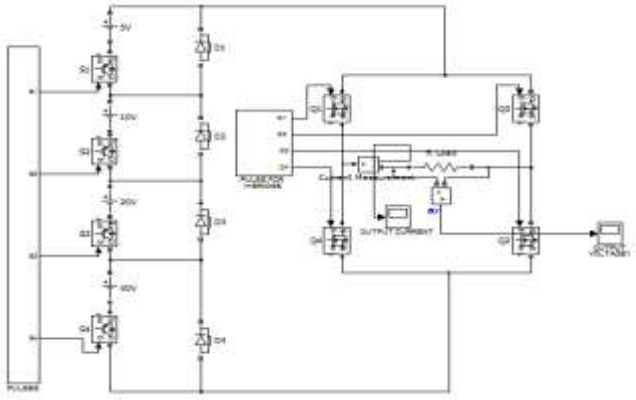

Figure 4 Simulink Model For single Phase system

To place the IGBT switches, select the power electronics block from the power system block. Connect the pulse generators to the gate terminal of each IGBT. Four electrical sources are chosen from electrical source block and each value are asymmetric and the diodes are taken from the power electronic component in the simulink power system. The electrical sources are connecting in series with the IGBT and the diodes are connected in parallel with the sources. Then the series parallel connections are fed to the H-bridge inverter and the load is connected to the H-bridge inverter.

From the voltage waveform given below we identified that the peak voltage of 75V is achieved. The peak voltage value is the sum of all four voltage source (5V+10V+20V+40V). The waveform has 31-levels in both positive and in negative side with zero as common, which occurs twice per cycle. The figure 5 shows the single phase voltage waveform of the proposed hybrid multilevel inverter.

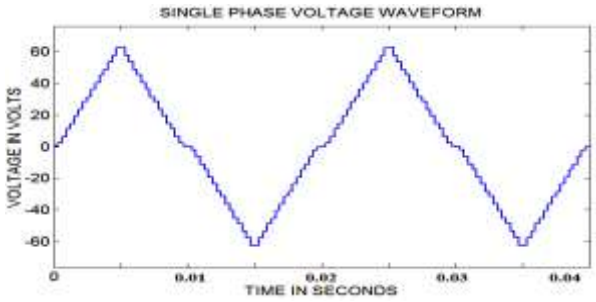

Figure 5 Single Phase Voltage Waveform

4.2.2 SIMULATION OF 31-LEVEL THREE PHASE INVERTER

The induction motor is taken as load for inverter from the electrical machines block in the power system. Since the phase displacement blocks are connected to each output of the single phase inverter to produce the proper phase delay between the each phase it is shown in the figure 6

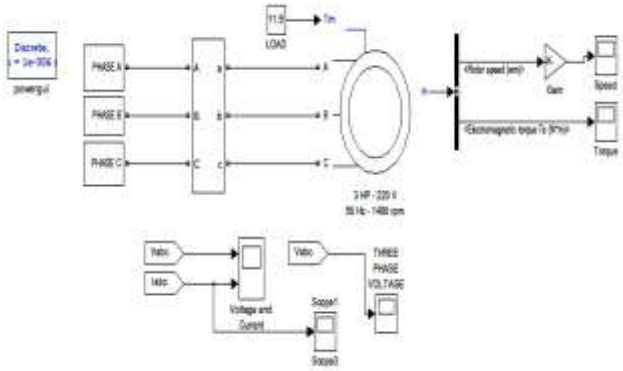

Figure 6 Simulink Model for Three Phase inverter.

To analyze various parameters like voltage waveform, current waveform, rotor speed and the electromagnetic torque of the induction motor scope is used. The output current waveform is used to analysis THD, which is select from powergui, then FFT analysis in which the signals are selected for the analysis and the THD will used to get displayed in FFT window.

The proper switching sequence should be provided to the IGBT, the pulse generator is used to produce the reference pulse AND, NOT logic is used to produce the pulse for switches. For H-bridge inverter also AND, NOT logic is used. This method is simple and easy to adapt which are taken from the commonly used blocks.

4.2.3 SIMULATION PARAMETERS

The following parameter are selected according to the induction motor specifications

Electrical source

$V_1 = 26.5V,$

$V_2 = 52.5V,$

$V_3 = 105V,$

$V_4 = 210V$

Motor Type: Induction motor

Number of Phase: 3-phase,

Stator resistance Rs=0.435 ohms,

Rotor resistance Rr=0.816 ohms,

Frequency=50 Hz, 3 HP, 220V.

4.2.4 SIMULATION RESULTS AND DISCUSSION

The computer simulation for the new topology of hybrid multilevel inverter has been done by using the MATLAB/SIMULINK. The output waveform has 31-levels in the positive side and 31-levels in the negative side and a zero level. This voltage levels are achieved with the help of four unequal voltage sources. The positive and negative waveforms are produced with the help of H-bridge inverter.

The figure 7 shows the 31-level inverter output voltage waveform for peak voltage of 400V. Induction motor is connected as a load. The output waveform has 31-levels in both positive and negative half cycle that include zero level that occur twice in a cycle. It can be archived by connecting three separate single-phase and the phase delay is given with the help of phase delay block. The Figure 8 shows the current waveform for three-phase inverter. From the curve we found that initially the current taken by the motor is high after a certain time it reaches the steady state. The current taken by the motor at steady state is 25A

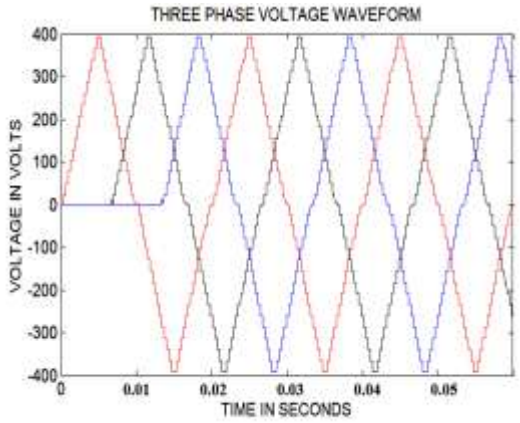

Figure 7 Three Phase Voltage Waveform

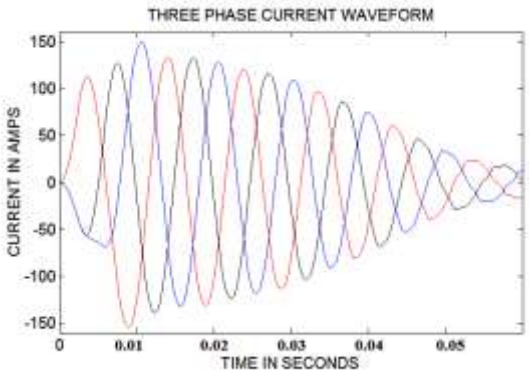

Figure 8 Three Phase Current Waveform

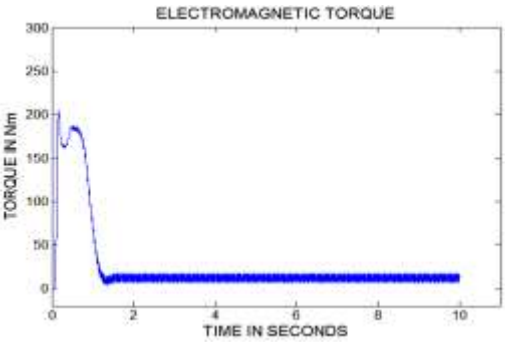

Figure 9 Electromagnetic Torque

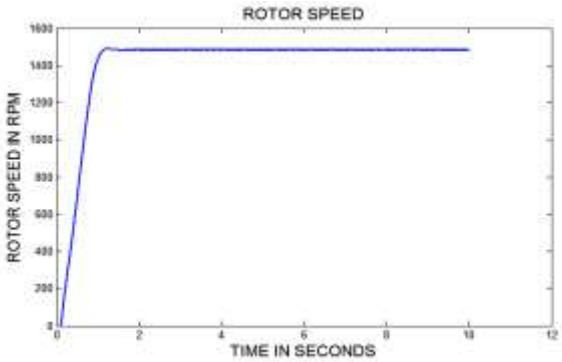

Figure 10 Rotor Speed of the Motor.

The figure 9 shows the electromagnetic torque of the induction motor. Initially the starting torque of the induction motor is very high up to 200Nm. Then in the steady state it reaches up to 20 Nm and maintain as a constant. Since the motor is connected to constant full load.

The figure 10 shows the rotor speed of the induction motor. It is observed in the graph the rotor speed of motor is 1480rpm under steady state. Since the motor is fully loaded and does not have any oscillation in the load.

4.2.5 FFT ANALYSIS

The output of the hybrid multilevel inverter is connected to the three-phase induction motor. This circuit is simulated in

the MATLAB software and the output current waveform is analyzed for THD using FFT method. Here 50 cycles of load current are taken as a sample for FFT analysis. The maximum frequency of 150Hz is taken as a limit for clear visibility of the harmonic spectrum. The figure 11 shows the harmonic spectrum obtained from FFT analysis for conventional CHB inverter.

From the Figure 11 we identified that the amount of harmonics present in the output and the THD is found to be 13.15%. The figure 12 shows harmonic spectrum for proposed method and the harmonic content is found apparently low 1.99% compare to the conventional method which satisfies IEEE standards.

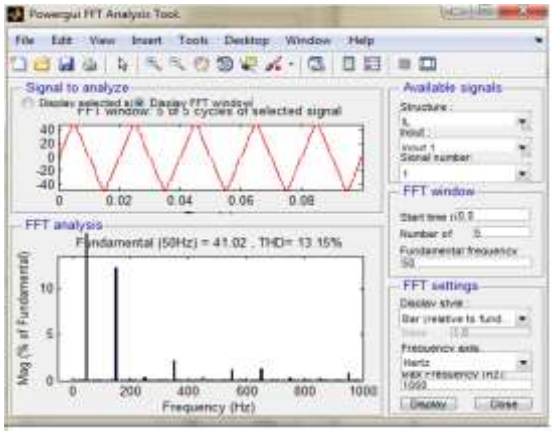

Figure 11 FFT analysis for conventional method

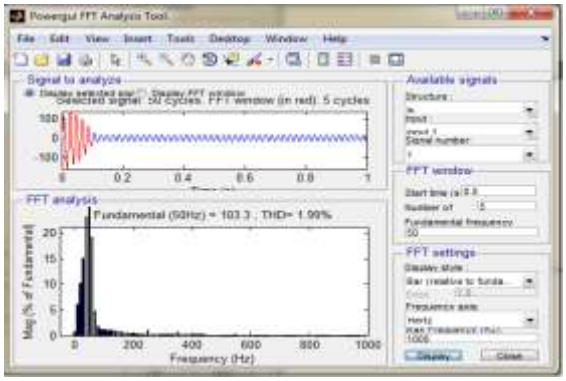

Figure 12 FFT analysis for proposed method

4.2.6 PROPOSED MODULATION SCHEME

In this proposed inverter switching pulse is given to each IGBT by pulse generator. The figure 13 shows the simulation model of proposed modulation technique. Since the switch S1 is most frequently operated nearly 16 times per half cycle. The switching frequency of the switch S1 is about 1600Hz. Hence IGBT are selected as power switches due to its high switching frequency nearly 40 KHz. Since the proposed hybrid multilevel inverter is employed with open loop control, the pulse generator is directly used to produce switching pulse to the device. For both bye pass diode technique and common H-bridge technique pulse generator are used. Both the operations are independent to each other. By producing correct triggering pulse to the switch, the switching losses can be minimized.

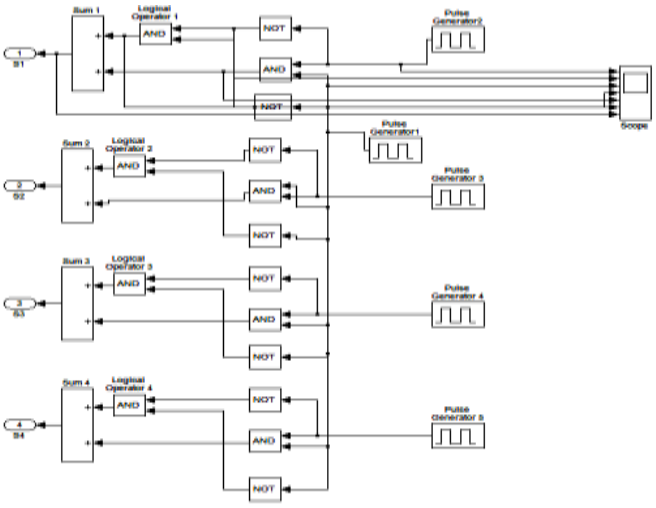

Figure 13 Simulink Model of Switching pulse generator.

The pulse generator 1 is used to generate the reference pulse in sample based and the width of the pulse is 50%, amplitude is 1 and the period of pulse is 0.01. The pulse generator 1 is taken as a reference for all switches S1, S2, S3, and S4. The figure 14 shows the pulse generator pulse waveform.

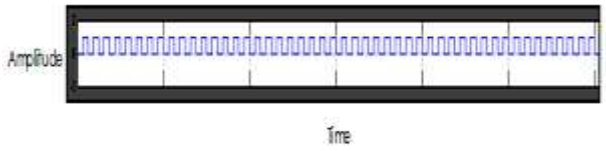

Figure 14 Pulse Generator Waveform

The pulse generator 2 is used to generate switching pulse for switch S1. The amplitude of the pulse is 1 and the conduction period is 50%, time period is (1/1600). The figure 15 shows the switching pulse for S1. The pulse generator 3 is used to generate switching pulse for switch S2. The amplitude of the pulse is 1 and the conduction period is 50%, time period is (1/800). The figure 16 shows the switching pulse for S2.

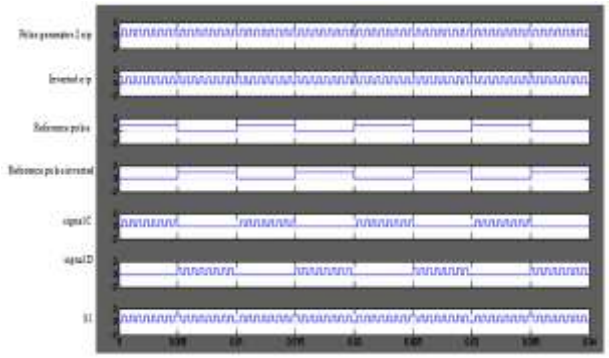

Figure 15 Switching pulse for switch S1.

The pulse generator 4 is used to generate switching pulse for switch S3. The amplitude of the pulse is 1 and the conduction period is 50%, time period is (1/400). The figure 16 shows the switching pulse for S3

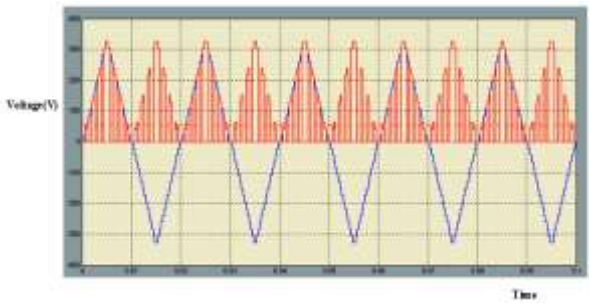

Figure 16 Switching pulse for switch S2.

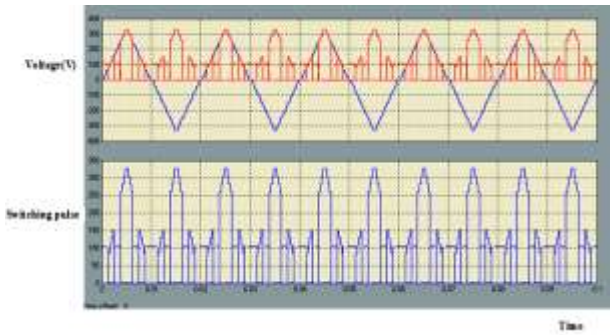

Figure 17 Switching pulse for switch S3.

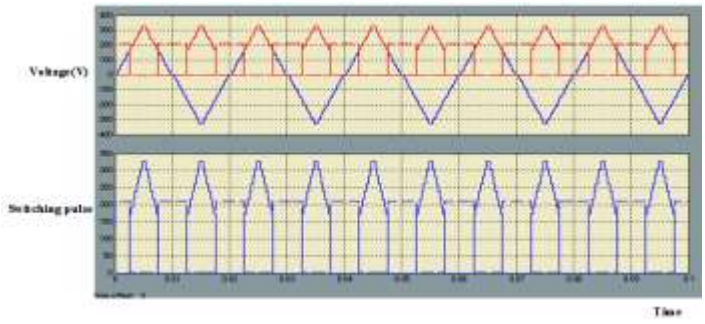

Figure 18 Switching pulse for switch S4

The pulse generator 5 is used to generate switching pulse for switch S4. The amplitude of the pulse is 1 and the conduction period is 50%, time period is (1/200). The figure 18shows the switching pulse for S4.

4.2.7 SWITCHING PULSE FOR H-BRIDGE

Since the main inverter circuit is used to produce stair case voltage waveform only in positive half cycle so H-bridge circuit is used to produce both positive and negative sine waveform. Figure 19 shows the H-bridge inverter circuit. One switch in the upper leg and one switch in the lower leg will conduct same leg switches are does not get conduct at same time to avoid the short circuit and damage of the switches. Figure 20 shows Pulse for H-Bridge Inverter.

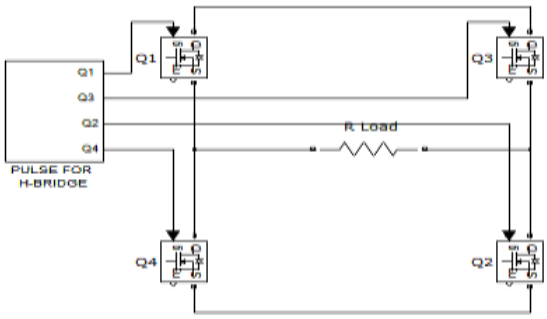

Figure 19 H-Bridge inverter Circuit

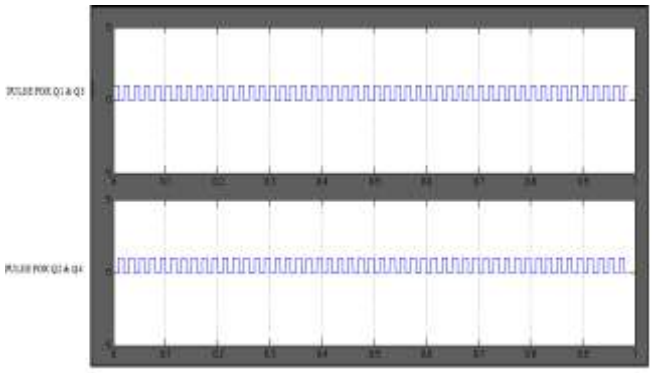

Figure 20 Pulse for H-Bridge Inverter

4.3 COMPARISONOF SIMULATION RESULTS

The proposed hybrid multilevel inverter is compared with series parallel switched multilevel DC link inverter topology and new dual bridge multilevel DC-link inverter topology with some of key factors that affect the inverter operations. The important key factors like

- switching device
- bye pass diode,
- clamping diodes,
- DC split capacitors,
- DC source,
- output voltage levels
- THD

are taken into account. The comparison results are shown in following table

Table 2 Harmonic Comparison

KEY FACTORS	SERIES PARALLEL SWITCHED MLI	DUAL BRIDGE MLI	PROPOSED HYBRID MLI
SWITCHING DEVICE	10	10	8
BYPASE DIODE	1	2	4

CLAMPING DIODE	-	-	-
DC SPLIT CAPACITOR	-	-	-
DC SOURCE	3	3	4
VOLTAGE LEVELS	15	15	31
THD	8.28%	8.18%	5.66%

From the above harmonic comparison table, we observe that the percentage of THD present in output of proposed inverter is low than the conventional method. These results indicate that the proposed inverter can be utilized for sensitive load and for standalone inverter operation

4.4 MODEL OF SWITCHING ON SIX BIT UP/DOWN COUNTER:

The counter switching scheme is not the only possible low frequency switching scheme that can be used to eliminate harmonics in the multilevel converter's output voltage. To illustrate this point, the proposed switching schemes for a multilevel inverter with six separate de sources for single phase (s = 6) and with the number of switching limited to 64 per quarter cycle. The other schemes are considered because they may produce a voltage waveform with lower THO than the counter method, particularly at lower amplitude modulation indices. V de is varied in order to keep the modulation index in a range for which the THD is minimum.

Table 3 Switching Sequence in counter

S. No	Order	Sequence(S1-S6)	Binary equivalent
1.	Increment	0 to 63	0 (000000) to 63 (11111)
2.	Decrement	63 to 0	63 (11111) to 0 (000000)

5. CONCLUSION AND FUTURE SCOPE

5.1 CONCLUSION

Multilevel inverters offer improved output waveforms and lower THD. This project presents a new topology of hybrid multilevel inverter with reduced number of switches. A bypass diode technique is introduced to the conventional H-bridge multilevel inverter topology which reduces the number of controlled switches in the system. Only one H-bridge is required for the single phase system, plus a switch and a diode for each voltage source. Due to involvement of high number of switches in the conventional method the harmonics, switching losses, cost and the total harmonics distortion are increased. This proposed topology increases the output voltage level with less number of switches. It dramatically reduces the switches for high number of levels that in turn reduces the switching losses; cost and low order harmonics and thus effectively improves Total harmonics distortion reduction. To verify proposed hybrid multilevel inverter concept simulation model is developed and tested.

5.2 FUTURE WORK

The major scope of the future work is hardware implementation of high power 31-level voltage source inverter for domestic home UPS. This system can be used for home UPS due to its nearby output sine waveform and less harmonic content. Since conventional home UPS inverter efficiency is only about 40%. The hybrid inverter use only less number of power switches so the inverter efficiency will be certainly high. The main applications of hybrid inverter are given below:

Air conditioner: The hybrid inverter can also be used in air conditioner to modulate the frequency of the alternating current to control the speed of the air conditioner motor to achieve continuous adjustment of temperature.

Stand alone inverter: They are commonly used in remote renewable energy systems producing power from photovoltaic panels and small wind turbines, most of these system use modified sine wave type inverter because load cannot tolerate the high harmonic content.

REFERENCES

1) Thamizharasan.S, Baskaran.J, Ramkumar.S and Jeevananthan.S, "A New Dual Bridge Dc-Link Inverter Topology" ELSEVIER, Electric Power and Energy Systems 45 (2013) 376-383.

2) Alireza Nami, Firuz Zare and Arindam Ghosh," A hybrid cascaded converter topology with series-connected symmetrical and asymmetrical diode clamped H bridge cells," IEEE Transactions on Power Electronics, Vol. 26, No. 1, January 2011.

3) Ebrahim Babaei, "A cascade multilevel converter topology with reduced number of switches" IEEE Transactions on Power Electronics, Vol. 23, No. 6, November 2008.

4) Ebrahim Babaei, "Reduction of dc voltage sources and switches in asymmetrical multilevel converters using a novel topology" ELSEVIER, Electric Power Systems Research 77 (2007) 1073–1085.

5) Ebrahim Babae "Optimal Topologies for Cascaded Sub-Multilevel Converters", Faculty of Electrical and Computer Engineering, University of Tabriz, Tabriz, Iran.

6) Franquelo LG, Rodriguez J, Leon JI, Kouro S, Portillo R, Prats MAM,"The age of multilevel converters arrives," IEEE Ind Electron Mag 2008;2(2):28–39.

7) Hammond PW. "A new approach to enhance power quality for medium voltage AC drives". IEEE Trans Indus Appl 1997; 33(1):202–8.

8) Jose Rodriguez, Jih-Sheng Lai, and Fang Zheng Peng, "Multilevel inverter; A survey of topologys, controls, and applications," IEEE Transactions on Power Electronics, Vol. 49, No. 4, November 2002.

9) Javad Ebrahimi, Ebrahim Babaei, and Goverg B. Gharehpetian, "A New Topology of Cascaded Multilevel Converters with Reduced Number of Components for High-Voltage Applications", IEEE Transactions on Power Electronics, Vol. 26, No. 11, November 2011.

10) EL- Kholy EE, EL-Sabbe A, El-Hefnawy A, Mharo HM," Three-phase active power filter based on current controlled voltage source inverter," Int J Elect Power Energy Syst 2006;28(8):537–47.

11) Meynard TA, Foch H, Forest F, Turpin C, Richardeau F, Delmas L, et al. "Multicell converters: derived topologies", IEEE Trans Indus Electron 2002;49(5):978–87.

12) Moreno-Munoz A, De-La-Rosa JJG, Lopez-Rodriguez MA, Flores-Arias JM,Bellido-Outerino FJ, Ruiz-de-Adana M. Improvement of power quality using distributed generation. Int J Elect Power Energy Syst 2010; 32(10):1069–76.

13) Munduate A, Figueres E, Garcera G. Robust model-following control of a threelevel neutral point clamped shunt active filter in the medium voltage range. Int J Elect Power Energy Syst 2009; 31(10):577–88.

14) Pengwei Sun and chuang Liu, "Cascade dual buck inverter with phase-shift control," IEEE Transactions On Power Electronics, Vol. 27, No.4, april 2012.

15) Rodriguez J, Franquelo LG, Kouro S, Leon JI, Portillo RC, Prats MAM, et al. "Multilevel converters: an enabling technology for high-power applications," Proc IEEE Int Conf 2009;97(11):1786–817.

16) Ramkumar.S and Kamaraj.V, "A new series parallel switched multilevel dc-link inverter topology". ELSEVIER, Electrical Power and Energy Systems 36(2012)93-99.