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Fin FET Two Bit Comparator for Low Voltage, Low Power, High Speed and Low Area in 18nm Technology

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Abstract - *Two-bit magnitude comparator style victimization totally different logic designs is planned during this temporary. Comparison is most elementary mathematical operation that determines if one range is larger than, equal to, or but the opposite range. Comparator is most elementary part that performs comparison operation. This temporary presents comparison between totally different logic designs wont to style 2-Bit magnitude comparator. Comparison between totally different styles is calculated by simulation that's performed at 18nm technology in cadence EDA Tool. It is observed from the Table 3, Proposed Fin FET Two Bit Comparator, We have reduced Dynamic Power 90%, Leakage Power Reduced 87%, Delay reduced 73% and Area Reduced 60% using Cadence 18nm Technology.*

Key Words: Fin FET Bit Comparator, high speed, low power and Low area, VLSI, DSP.

1. INTRODUCTION

There are unit 2 sources of power consumption in CMOS particularly dynamic and run. The dynamic power consumption in CMOS could be a quadratic operate of the availability voltage (VDD) and therefore the run power is its mathematical function[1]. Hence, the most effective thanks to cut back the facility consumption is thru VDD scaling. the acute case of VDD scaling is that the sub-threshold regime during which it's scaled below the threshold voltage (Vth) to attain extremist low power (ULP) consumption. The run current is employed as a driving current in sub-threshold circuits and thus, they are used just for low outturn applications[2]. Moreover, in sub-threshold region, exponential I-V characteristics makes device a lot of sensitive to method, voltage, and temperature variations. Hence, to increase the appliance domain of sub-threshold region, there's a requirement to deal with the speed and strength problems. This thesis explores different techniques to enhance the performance and strength of sub-threshold circuits and interconnects in order that they will even be utilized for moderate outturn applications[3]. It conjointly investigates techniques to reinforce the performance and robustness of sub-threshold FPGA in order that it will replace the overpriced and rigid ASICs for reconfigurable ULP applications.

In this work is designed as pursue category II today Literature survey on Fin FET 4:1 Multiplexer Category III today the methodology for Fin FET 4:1 Multiplexer and also discussed the High speed, low power and low area. Category IV shows the simulation results and they are explained clearly, after the work is concluded with category V.

2. LITERATURE SURVEY

A continuous scaling in VLSI technology with each method generation causes Associate in Nursing exponential increase in power dissipation that imposes a elementary limitation to increasing performance and practicality in high performance microprocessors. escape power has become thus vital that it can't be neglected[4]. The appearance of computationally advanced moveable devices and developments in wireless communications additionally demand a discount of power dissipation while not sacrificing abundant performance[5]. This provides the motivation to explore power reduction techniques in CMOS VLSI circuits. Historically, dynamic change power has been the dominant component of total power consumption.[6] Dynamic power may be quadratic ally reduced by lowering the provision voltage. Lowering the provision voltage reduces the circuit speed thanks to reduced junction transistor drain currents. Hence, threshold voltages square measure scaled all the way down to cut back the degradation in speed caused by provide voltage scaling. However, subjection in Vt threshold voltage causes Associate in Nursing expanding development in sub junction current or sub threshold escape currents[7]. Hence, as technology scales down, escape currents tend to dominate the overall power consumed by CMOS circuits. Therefore, energy economical circuit techniques aimed toward lowering escape square measure extremely fascinating. This provides the motivation to style digital circuits that have reduced escape with optimum performance. Also, stable and reliable operation of CMOS circuits gets degraded thanks to reduction in noise margin with lowered provide voltages and multiplied leakage[8]. Hence, noise margins of the circuits are measured. The initial phases of analysis and development efforts in VLSI design were familiarized towards achieving high speed and miniaturization. At present, the growing trends in transportable computing and wireless applications demand the necessity to hunt out new technologies and style circuits that consume low power[9]. This necessitates the necessity to orient the research towards reducing power dissipation in VLSI circuits. Recent trends within the growth and development of battery powered portable and mobile computing devices necessitate the necessity for extended battery life and thence lesser battery power consumption[10]. The battery life is more reduced by the

employment of high speed processors and huge recollections in them. Also, the magnitude of power dissipation per unit space within the integrated circuits of gift day microprocessors and recollections square measure chop-chop increasing due to the accumulated speed and flexibility[11]. This worsens the matter of warmth removal and cooling (Kaushik Roy 2000). Also, these high power densities reduce chip dependability and anticipation, increase cooling prices and will even cause environmental problems in giant knowledge centers. escape power is additionally increasing with technology scaling and can't be neglected. of these factors demand the necessity for value effective solutions to power problems; else improvements in chip technology can reach a standstill[12].

3. DESIGN METHODOLOGIES

3.1 BIT MAGNITUDE COMPARATOR

Two -Bit Magnitude Comparator Compares two numbers each having two bits (A1, A0 & B1, B0). For this arrangement truth table [5] has four inputs & six teen entries as in Table 1.

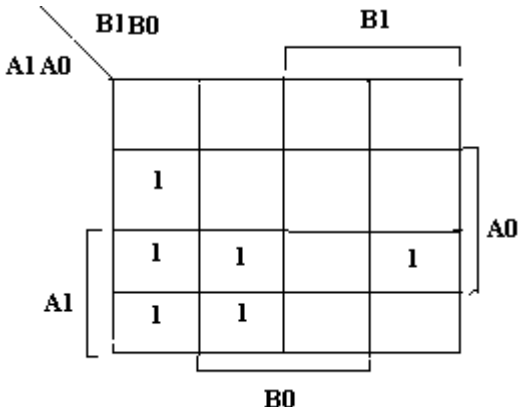
Table1:Truth table of 2bit magnitude comparator.

INPUT				OUTPUT		
A1	A0	B1	B0	A>B	A=B	A<B
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

3.2 Karnaugh Mapping

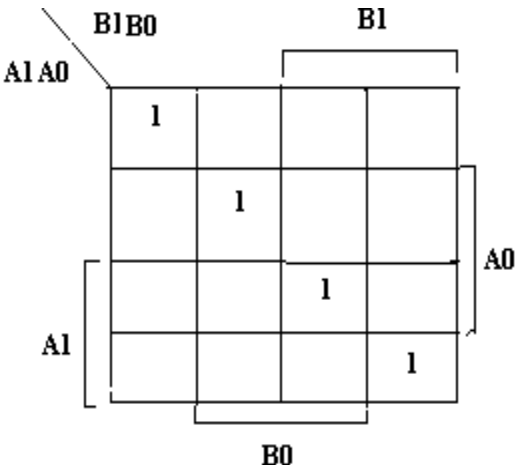
K-Map is used to minimize Boolean function obtained from truth table [5].

For A>B



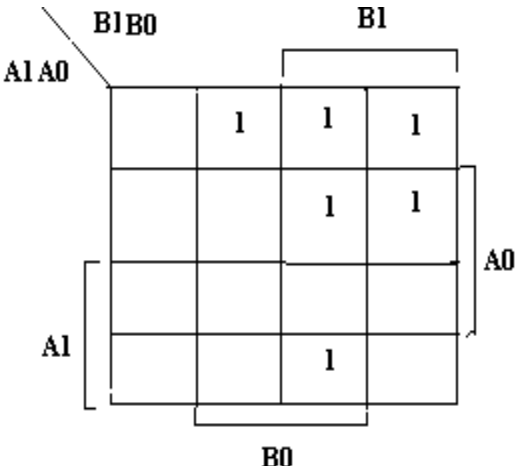
$$A>B: = A1B1'+A0B0'A1'B1'+A0B0'A1B1$$
$$= A1B1'+A0B0'(A1'B1'+A1B1)$$
$$= A1B1'+A0B0' X1$$

For A=B



$$A=B: = A1'A0'B1'B0'+ A1'A0B1'B0+A1A0'B1B0'+A1A0B1B0$$
$$= (A1'B1'+A1B1)\,(A0'B0'+A0B0)$$
$$= X1X0$$

For A<B



A<B: = A1'B1+A0'B0A1'B1'+A0'B0A1B1
= A1'B1+A0'B0(A1'B1'+A1B1)
= A1'B1+A0'B0 X1

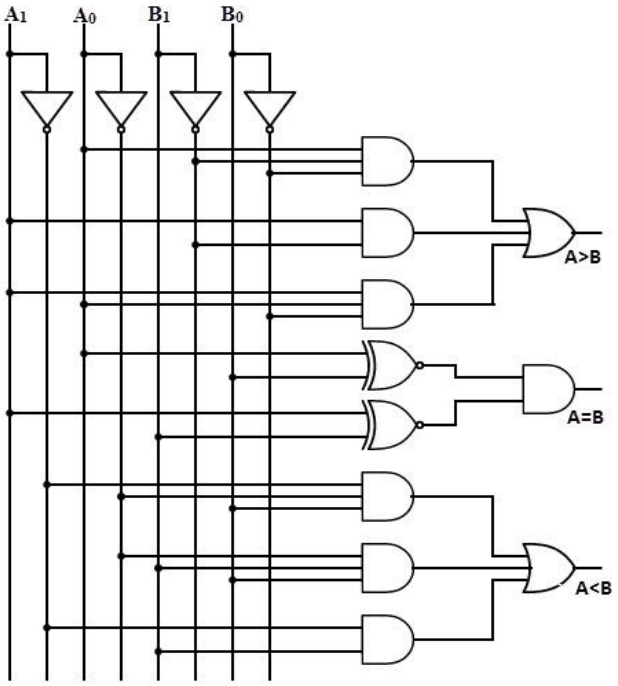


Figure 1. Logic Diagram of 2-Bit Magnitude Comparator

3.3 Power Dissipation

Low power circuit style has appear as a dominant theme in today's industry. within the past, major issues among researchers and designers for planning integrated circuits were on space, speed, and cost; whereas secondary importance was paid to power dissipation.

$$P_{Static} = I_{Static} * v_{dd} \quad [1]$$

$$P_{Dynamic} = \alpha * c_L * v_{dd}^2 * f \quad [2]$$

$$P_{Shortcircuit} = I_{SC} * v \quad [3]$$

$$P_{Leakage} = V_{dd} * (I_S + I_G + I_D) \quad [4]$$

$$P_{Total} = P_{Dynamic} + P_{Leakage} \quad [5]$$

$$P_{Total} = (\alpha * c_l * v_{dd}^2 * f) + V_{dd} * (I_S + I_G + I_D) \quad [6]$$

Where α is a transient (time) response, c_L is a load capacitance (charging or discharging), Vdd equal voltage, f equal frequency.

4. Simulation Results

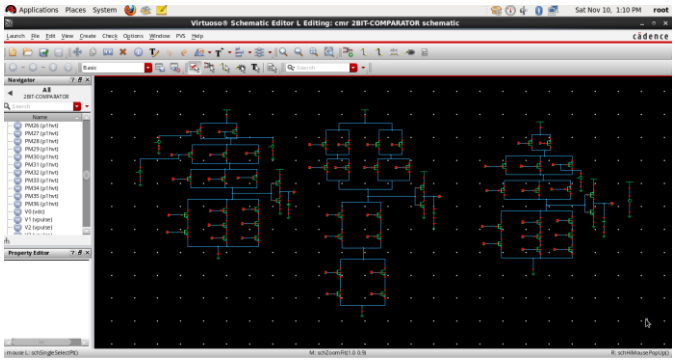


Figure 2: Fin FET Two bit comparator Schematic diagram.

It is observed from the Figure 2, The phvt and nhvt transistors schematic diagram consist of Fin Pitch are 48nm, Load capacitance is 10fF, at supply voltage from 1Volts. Conventional of Fin FET Two bit comparator Schematic diagram was carried out using Cadence 18nm technology.

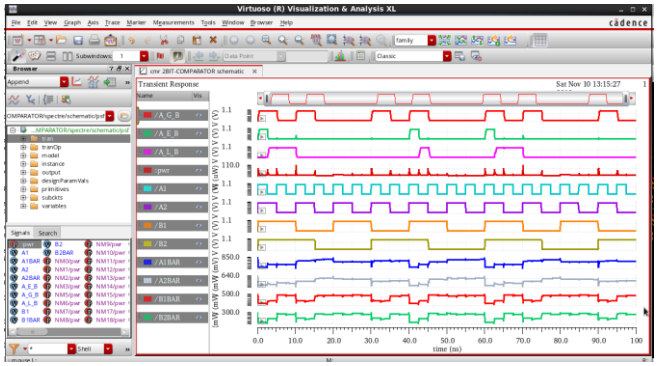


Figure 3: Fin FET Two bit comparator Output Waveform at 10MHz.

As shown in figure 3 Fin FET Two bit comparator Output Waveform simulation result of output waveform at 1Volts at the frequency 10MHz in 18nm technology.

Table 2: Fin FET Two bit comparator nhvt & Phvt Specifications

Specification	nhvt	phvt
Library name	gpdk (ff)	gpdk (ff)
Fin pitch	48 nM	48nM
Drawn Gate Length	18	18
Number of Fins per	2	2

Finger		
Number of Finger	1	1
Multiplier	1	1
Load Capacitance	10 fF	

Table 3: Simulation Results for Fin FET Two bit comparator with 1 V supply in 18nm Technology

Design	Voltage (V)	Dynamic power (µW)	Leakage power (nW)	Delay (nS)	Area (nm2)
Conventional	1	7.77	100.7	2.911	180.84
Proposed	0.5	0.7	12.71	0.7751	72.16

It is observed from the Table 3. Proposed Fin FET Two bit comparator, We have reduced Dynamic Power 90% , Leakage Power Reduced 87% , Delay reduced 73% and Area Reduced 60% using Cadence 18nm Technology.

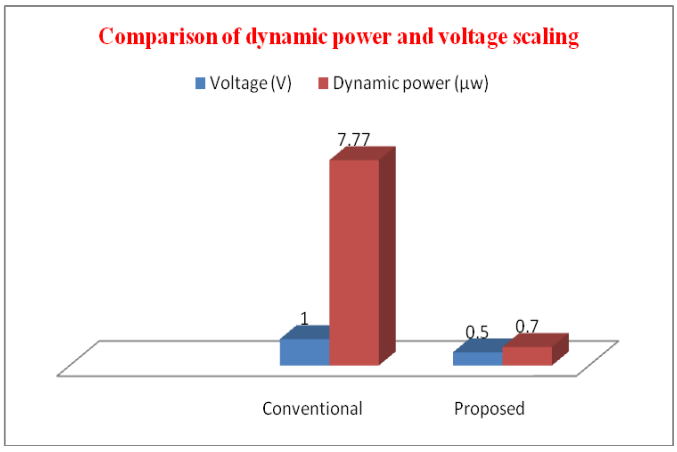


Figure 4: Comparison of dynamic power and voltage scaling Two bit comparator in 18nm Technology.

It is observed from the Figure 4, We have reduced Dynamic Power 90%.

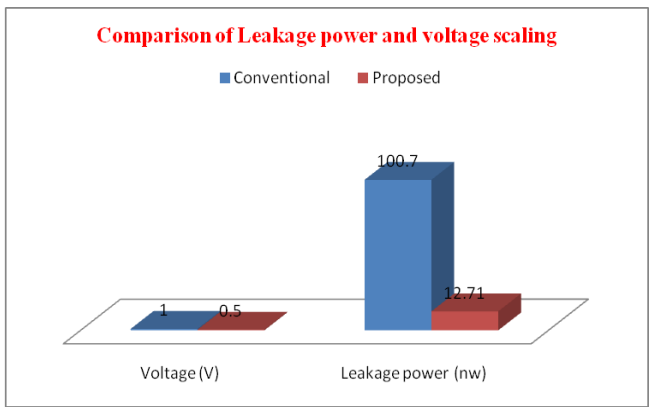


Figure 5: Comparison of Leakage power and voltage scaling

It is observed from the Figure 5, We have reduced Leakage Power 87%.

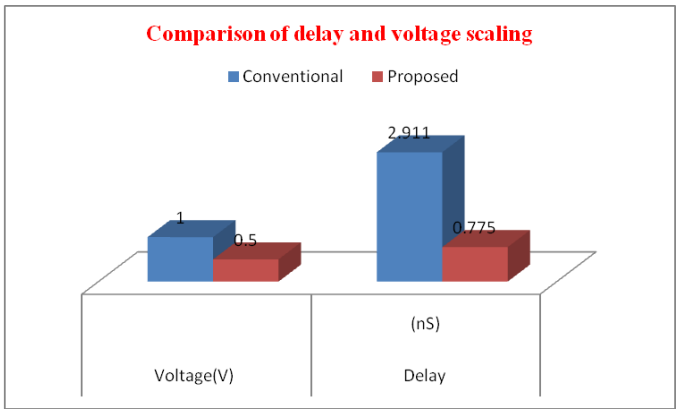


Figure 6: Comparison of delay and voltage scaling .

It is observed from the Figure 6, We have reduced Delay Power 73%.

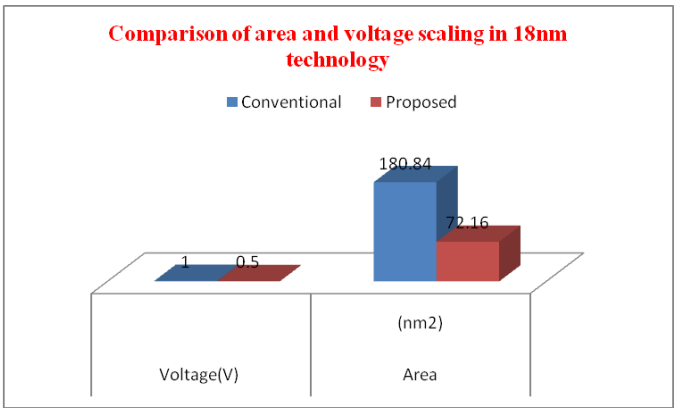


Figure7: Comparison of area and voltage scaling

It is observed from the Figure7, We have reduced Area Power 60%.

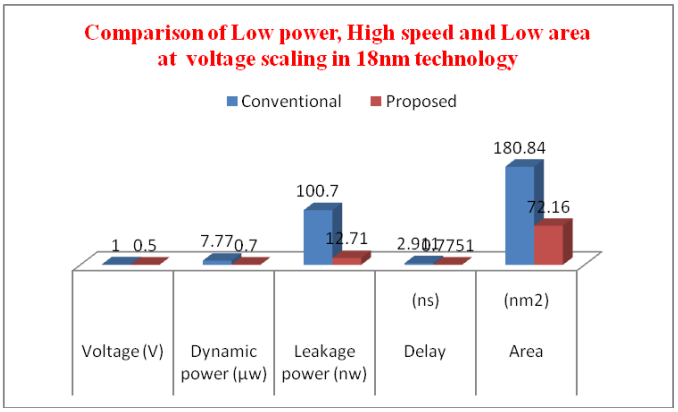


Figure8: Comparison of Conventional and Proposed Fin FET two bit comparator in terms of power ,delay and area at voltage scaling in 18nm technology

It is observed from the figure 8, Proposed Fin FET Two bit comparator, We have reduced Dynamic Power 90% , Leakage Power Reduced 87% , Delay reduced 73% and Area Reduced 60% using Cadence 18nm Technology.

5. CONCLUSION

Two-bit magnitude comparator style victimization totally different logic designs is planned during this temporary. Comparison is most elementary mathematical operation that determines if one range is larger than, equal to, or but the opposite range. Comparator is most elementary part that performs comparison operation. This temporary presents comparison between totally different logic designs wont to style 2-Bit magnitude comparator. Comparison between totally different styles is calculated by simulation that's performed at 18nm technology in cadence EDA Tool. It is observed from the Table 3, Proposed Fin FET Two Bit Comparator, We have reduced Dynamic Power 90% , Leakage Power Reduced 87% , Delay reduced 73% and Area Reduced 60% using Cadence 18nm Technology.

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