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DEISGN OF LOW POWER 16x16 SRAM WITH ADIABATIC LOGIC

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Abstract - *A SRAM or Static Random Access Memory is a type of semiconductor memory that uses bi-stable latching circuitry to store each bit. SRAM exhibits data remains, but it is still volatile in the conventional sense that data is eventually lost when the memory is not powered. SRAM is useful building blocks in many applications such as a data storage, embedded applications, cache memories, microprocessors. In microprocessors, large SRAM arrays are widely used as cache memory and application-specific integrated circuits can occupy a significant portion of the die area. SRAM arrays are high density circuits which are projected to occupy more than 90% of the SoC (System on Chip) area in the next 10 years. The performance of such chips is to optimized for which large arrays of fast SRAM are useful to boost of the performance. Besides, the impact of integrating large SRAM cells onto a chip will certainly lead to a higher chip cost, resulting in the involvement of millions of small size SRAM arrays are together integrated forming the densest circuitry on the chip. Access time, speed, and power consumption are the three key parameters of an SRAM memory design. In this paper an effort is made to design a low power consuming 16X16 SRAM memory array comprising of Adiabatic logic on 180nm CMOS technology using Cadence tool.*

Key Words: SRAM, Adiabatic logic, SOC, power consumption

1.INTRODUCTION

With the rapid growth of modern communications and signal processing systems, handheld wireless computers and consumer electronics are becoming highly popular. The design of 6T SRAM has become a challenge for storage purpose in System on Chip (SoC) using Nanometer technology because of variations in the threshold values. The read/write operations carried out in the SRAM and the stability of the SRAM are effected due to the threshold variations. The SRAM is major component only occupies a larger area of the chip die. The demand for static random-access memory (SRAM) is increasing with large use of SRAM in mobile products, System On-Chip (SoC) and high performance VLSI circuits. SRAM covers an area of about 70% of the System on Chip. SRAM is a crucial component which has embedded use such as many scientific and industrial subsystems, automotive electronics and can be used as a cache memory in CPUs, microcontrollers, external burst mode SRAM caches and handheld devices.

Cadence tool is used to design the SRAM cell which includes a 180nm CMOS technology, which is a standard base for the fabrication given directly to the fabrication unit.

The design of a low power SRAM includes the functioning of some internally connected circuits such as Row and Column Decoders, Sense Amplifiers, SRAM Cells and Pre-Charge circuit. This paper illustrates the successful outputs of read and write operations consuming proposed low power and proper Adiabatic logic.

2. ADIABATIC LOGIC

Adiabatic Logic is the term given to low-power electronic circuits that implement the reversible logic. The term comes from the fact that an adiabatic process is one in which the total heat or energy in the system remains constant. Research in this area has mainly been fueled by the fact that as circuits get smaller and faster, their energy dissipation greatly increases, a problem that adiabatic circuits promises to solve. Most research has focused on building adiabatic logic out of CMOS. However, current CMOS technology, though fairly energy efficient compared to similar technologies, dissipate energy as heat, mostly when switching. In order to solve this problem, there are two fundamental rules CMOS adiabatic circuits must follow, the reasons for which are explained below. The first is never to turn on a transistor when there is a voltage difference between the drain and source. The second says never to turn off a transistor that has current flowing through it..

3. SRAM ARCHITECTURE

Fig-1 shows the architecture of 16x16 bit SRAM. Each address accesses a single-bit as it is a bit oriented SRAM. The 16bit address from the column decoders or column multiplexers are accessed through a single sense amplifier up to 2 or more columns. The SRAM circuit must be designed in such a way that the read and write operations must be performed effectively. The crucial blocks of the SRAM are as follows:

1) Pre-Charge circuit.
2) SRAM Cell.
3) Column Decoder.
4) Row Decoder.
5) Sense Amplifier

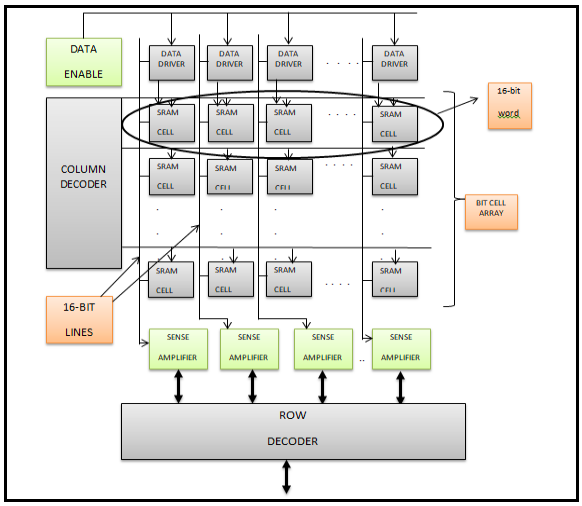

Fig -1: 256-bit SRAM Architecture

4. DESIGN OF THE SRAM CELL AND IMPLEMENTATION

This part illustrates the components of the SRAM circuit mentioned in the Section III

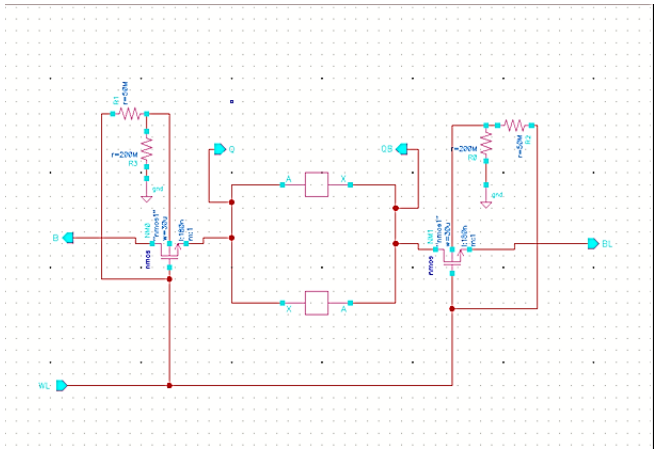

Fig -2: Schematic of the SRAM cell

4.1 The SRAM Cell:

The stable and robust operation of the SRAM is one of the essential design considerations for the SRAM cell. In order to enhance the on-chip storage capacity, the designers are asked over to increase the packing density. The SRAM cell must therefore have possibly small sizes in order to meet the stability, yield, power and speed constraints. The basic SRAM cell is designed with back to back connect CMOS inverters to form a latch for storing 1 bit of data storage (either 0 or 1). Two pass gates are arranged to access the data this connects the latch to two complementary bit line column's (BL and BL_B) and the two pass gates are activated when the word line asserted one (WL=1). The WL value must be equal to 1 in order to access the two pass transistors, however, if the value of WL is 0 then the circuit will be in the hold state. The SRAM cell design is used for the storage of data and it enables the non-destructive read operation and allows write operation in the cell. In the circuit, the width and length of NMOS transistor are 360nm and 180nm respectively, whereas the width and length of PMOS transistor are 720nm and 180nm respectively. Similarly. The width and length for pass transistors is 30um and 180nm respectively.

4.2 The Invertor circuit:

Here in this project, two CMOS inverters used which are connected back-to-back, such that they appear to be cross coupled. The two cross coupled inverters has the capability of holding the values of logic'1' and logic'0' as long as the circuit is powered up. A pair of cross coupled inverters have the output of one inverter going to the input of the other and vice versa, such that the output (and input) of one inverter is the complement of that of the other. Resistors are connected in order to withstand the voltage withstanding capability and also helps to regenerate the consumed power. Four resistors of certain values are taken and connected two for each one of the PMOS and NMOS transistors.

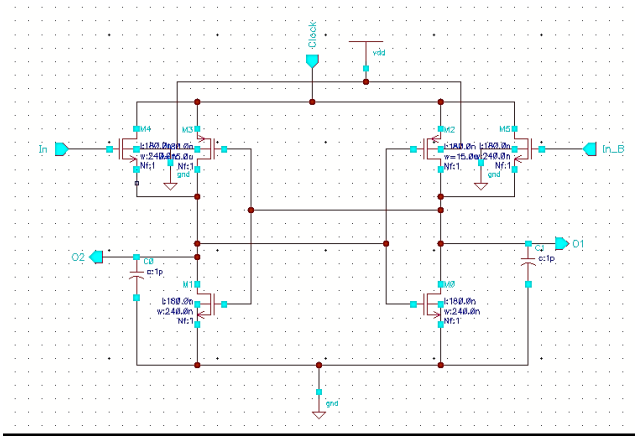

Fig -3: Schematic of the Inverter circuit

4.3 Sense Amplifier

Differential input sense amplifier is used in this project as shown in the above figure. A Sense Amplifier is one of the crucial elements of the SRAM cell which makes up the circuitry on a semiconductor memory chip. It is a part of the read circuitry and is used when there is a need to read the data from the memory. The Sense Amplifier role is to sense the low power signals which are the output from the Bitline, that represents a data bit (0 or 1), which is stored in the SRAM memory cell. It amplifies the small voltage levels received from the bit lines and attains a recognizable logic levels so that the data can be elucidated in a proper way outside the memory.

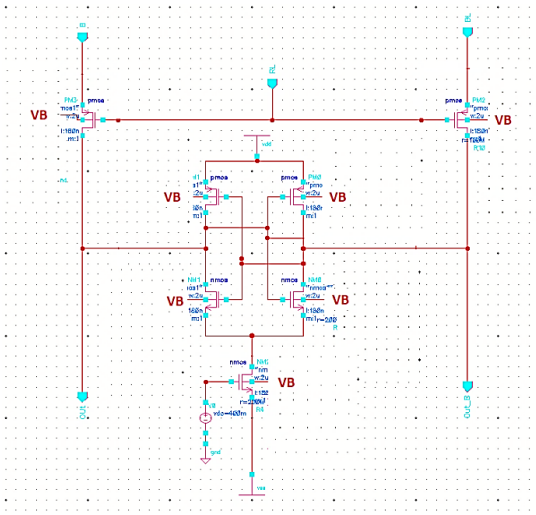

Fig -4: Schematic of Sense Amplifier

4.4 Row and Column Decoder

The most essential component of the entire SRAM cell is the decoder through which we can perform the read and write operations. It is also termed as the one of the important peripheral devices of the 16x16 array SRAM. Here a 4:16 decoder is used as row and column decoder to access the WL (Word Line) for each row/column of the circuit. The schematic of the 4:16 decoder is shown in the Fig 5.

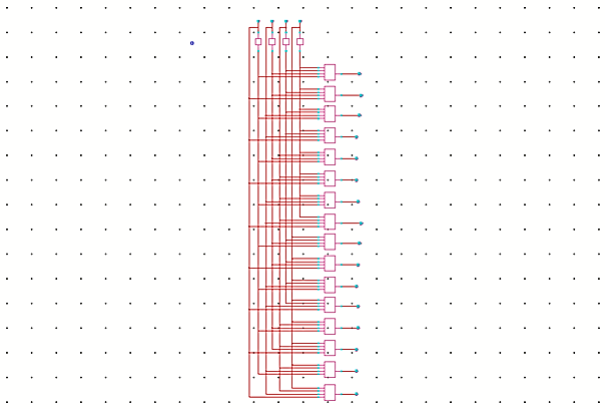

Fig -5: A 4:16 Decoder

The decoder has 4 input lines and 16 output lines. AND gate is one of the main crucial components of the decoder circuit. The type of AND gate used is conventional CMOS. Here the each output of the decoder acts as input i.e., Word line to each row containing the SRAM cells. For instance if we consider the input is given as A= '0', B= '1', C= '0', D= '0', then the fourth word line is chosen. The 4th word line is now further used for the read and write operations in the circuit.

The data inputs and the word line selections are illustrated in the following table as follows:

Table:1 Data and Word line Selection

Data Input Selection	Word line Selection
Datain0	1
Datain1	2
Datain2	3
Datain3	4
Datain4	5
Datain5	6
Datain6	7
Datain7	8
Datain8	9
Datain9	10
Datain10	11
Datain11	12
Datain12	13
Datain13	14
Datain14	15
Datain15	16

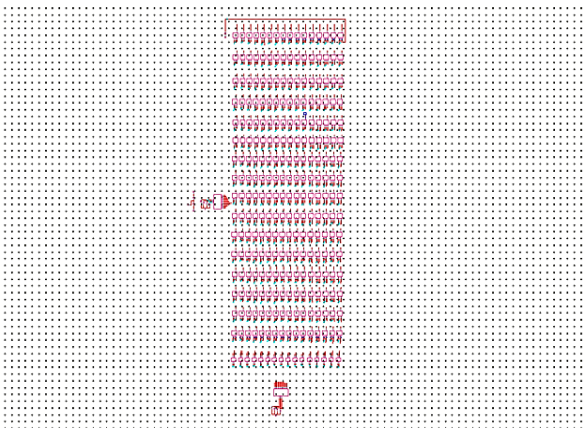

Fig -6: Schematic of 16x16 SRAM Memory array

The Fig-6 shows the 16x16 SRAM Memory array has a capability of storing 256 bits of memory. It consists of row decoder, column decoder, 16 Sense amplifiers, 256 bit SRAM cells. The outputs of the 16x16 memory array are readout and readout_bar, which are found to be complement to one another. The A, B, C, D are the row decoder inputs, depending on the particular input combination the corresponding word line and outputs are selected.

5. RESULTS

This section discusses the simulation results of 4:16 decoder and 16X16 memory array for write 1 and read 1 operation and write 0 and read 0 operations. The simulation tests are carried out using Cadence virtuoso with 180nm CMOS technology. During the output the transient response is taken in order to verify the read and write operations.

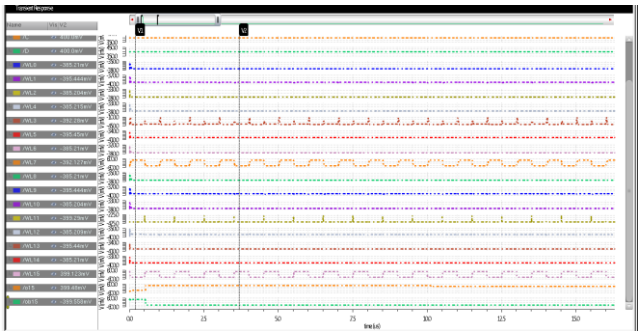

Fig -7: Transient Response of SRAM array for read 0 and read 1 operations

The above output signifies the successful execution of the read 0 and read 1 operations. Here the WL7 and WL 15 are activated so that the output can be easily verified. It is clearly seen that when the WL7 is low, the WL15 is appeared to be high, the output obtained at Q is high i.e., read 1 operation is performed and similarly at the same instance, the QB is appeared to be low i.e., the read 0 operation is performed. Hence, the read 0 ad read1 operations are successfully verified through the sense amplifiers

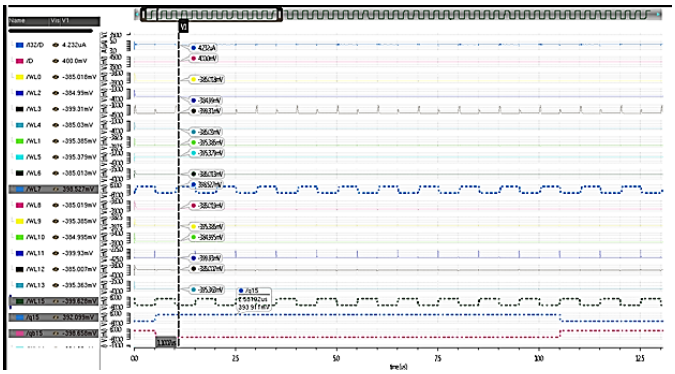

Fig -8: Transient Response of SRAM array for write 0 and write 1 operations

The Transient response for the write 0 and write 1 operations is as shown above. As in the read operation, also here the WL7 and WL15 are activated in order to perform the required operations. The WL7 when it is high at a point the WL15 is low, resulting in write 1 operation at Q and write 0 operation at QB. Therefore, the write 0 and write 1 operations are verified.

Table:2 Data and Word line Selection

PARAMETERS	RESULTS
Power Consumed	101uW
Supply Voltage	400mV p-p
Read access time	50uS
Write access time	50uS

6. CONCLUSION

A Low power 16X16 SRAM array is designed for storing 256 bits. Peripheral components such as row decoder, sense amplifier including and column decoder has been designed and assembled to form SRAM array. Differential type sense amplifier is used for noise reduction. Pulse input signal with a peak to peak voltage of 0.4V (rail-rail) and Supply voltage of 400mV is considered Transient responses for read and write operations for both logic -1 and logic -0 have been analyzed. Power consumption of 101uW is measured for complete SRAM array. SRAM array is designed in Cadence tool using Schematic editor Virtuoso. Standard gpdk180 library (i.e., 180nm technology node) is used for designing.

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