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Design and Implementation of Combinational Circuits using Reversible Gates

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Abstract *- Nowadays, the electronic systems are an important part of an human's life. As technology develops, the complexity of the system also increases. This leads to an increase in power consumption and causes a great issue faced in the world of electronics. Reversible logic reduces power consumption and zero-energy computation. The design of different combinational circuits like a full adder, subtract or, multiplexer and binary comparator circuits using reversible decoder is proposed with less Quantum cost.*

Keyword – Quantum Cost, Reversible Gate, Garbage Outputs, Number of Gate

1. INTRODUCTION

Reversible technology is used in various areas such as low power CMOS design, Nano-Technology, Quantum & Optical computing, DSP, etc. It is used for reducing power consumption and loss of data. In reversible technology there is no information loss at reversible logic so zero energy consumption takes place. It will help to avoid heat generation. In Digital Electronics, for design of combinational and sequential circuits various techniques are used. Design of a combinational circuit using binary decoder is one of them.

2. LITERATURE REVIEW

R. Landauer [1] proposed that the amount of energy (heat) dissipated for every irreversible bit operation is given by *KTln2*, where *K* is the Boltzmann's constant (1.3807×10-23 JK^{-1}) and T is the operating temperature. At room temperature (300 K), *KTln2* is approximately 2.8×10-21 J, this amount of energy is small but not negligible. He also proposed that only the logically irreversible steps in a computation carry an unavoidable energy penalty. If we could compute entirely with reversible operations, there would be low energy consumption. The amount of energy dissipated in a system has a direct relationship with the number of bits erased during computation [2]. If a computation is carried out in a reversible way then Energy dissipation would not occur. Ruqaiya Khanam, Abdul Rahman, Pushpam [3], proposed different applications of reversible gate. D. Maslov and G. Dueck [4] proposed the new reversible gates which differ only marginally from the generalized Toffoli gates. Reversible Cascade logic is used to minimize the most important factor of the reversible circuit cost which is the number of garbage output

3. REVERSIBLE LOGICS

A Reversible circuit design can be modelled as number of input equal to number of output and there is one to one mapping between them. In reversible circuit sequence of discrete time slices and depth is a summation of total time slices. Also it has zero fan-out. The typical model is shown in Fig 1.

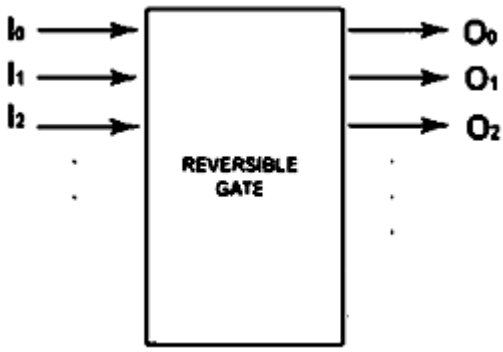


Fig- 1: A n × n Reversible Gate

3.1 Quantum Cost

The quantum cost of a reversible gate is defined by the total number of elementary quantum gates needed to realize the given function. Elementary quantum gate such as 1x1 and 2x2 reversible gates. The quantum costs of all

reversible 1x1 and 2x2 gates are taken as zero and unity respectively. Since every reversible gate is a combination of 1 x 1 or 2 x 2 quantum gate, the quantum cost of a reversible gate can be calculated by counting the numbers of NOT, Controlled-V, Controlled-V+ and CNOT gates used. Quantum cost is very important factor in quantum technology. There are some software tools available which are used to measure quantum cost of design circuit.

3.2 Garbage Output

Every gate output which not used for further processing is called as garbage output. The unused output which needs to maintain reversibility of reversible gate is known as garbage output.

3.3 Fan In

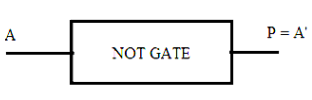
The maximum number of inputs that a logic gate can accept is called as fan-in. If number of input exceeds, the output will be vague or inaccurate

3.4 Fan Out

The fan-out is defined as the maximum number of inputs (load) that can be connected to the output of a gate without degrading the normal operation. Fan Out is calculated from the amount of current available in the output of a gate and the amount of current needed in each input of the connecting gate

NOT GATE:

A NOT gate is the single Reversible Logic gate. It is 1×1 Reversible Logic Gate. The outputs of NOT gate are denoted as P=A' and Quantum cost of a NOT gate is zero.

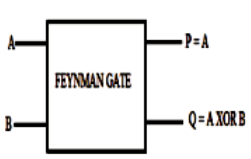


A	P
0	1
1	0

Fig- 2: NOT Gate and its Truth Table

FEYNMAN GATE

Feynman gate is also known as 2X2 reversible gate. The outputs of FEYMAN gate are denoted as P=A, Q=A XOR B and Quantum cost of a Feynman gate is one.

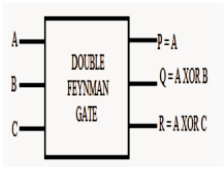


A	B	P	R
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

Fig- 3: Feynman Gate and its Truth Table

DOUBLE FEYNMAN GATE (DFG):

Double Feynman Gate is a 3×3 reversible gate. The outputs of DOUBLE FEYMAN gate are denoted as P=A, Q=A XOR B, R=A XOR C and Quantum cost of a Double Feynman gate is TWO.

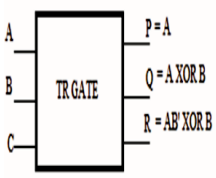


A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	0	0

Fig- 4: Double Feynman Gate and its Truth Table

TR GATE:

TR Gate is a 3×3 reversible gate. The outputs of TR gate are denoted as P=A, Q=A XOR B, R=AB' XOR C and Quantum cost of a TR gate is four.

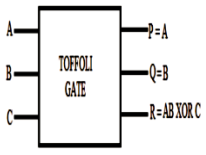


A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	0
1	1	1	1	0	1

Fig- 5: TR Gate and its Truth Table

TOFFOLI GATE

Toffoli Gate is a 3×3 reversible gate. The outputs of Toffoli gate are denoted P=A, Q=B, R=AB⊕ C and Quantum cost is five.

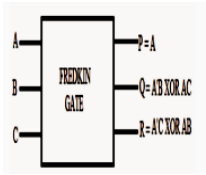


A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

Fig- 6: Toffoli Gate and its Truth Table

FREDKIN GATE

Fredkin Gate is a 3×3 reversible gate. The outputs of Fredkin gate are denoted as P=A, Q=A'B XOR AC, R=A'C XOR AB and Quantum cost of a Fredkin gate is five.

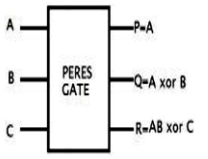


A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

Fig- 7: Fredkin Gate and its Truth Table

PERES GATE

It is also called as 3X3 reversible gate. The output is defined as P = A, Q = A XOR B and R=AB XOR C and the Quantum cost of Peres gate is 4.



A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

Fig- 8: Peres Gate and its Truth Table

4. BASIC GATES USING REVERSIBLE GATES

Considering the circuit requirements we need to design AND gate and OR gate using reversible gates. Here fredkin gate is used to design AND and OR gates as shown in Fig 9. Fredkin gate is preferred because it gives optimistic performance at less Quantum Cost for designing AND and OR gates.

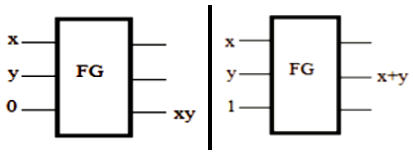


Fig- 9: AND Gate and or gate using Fredkin

5. REVERSIBLE DECODER

Digital decoder converts a set of digital input signals into an equivalent decimal code. It changes a code into a set of signals and does reverse encoding. Decoder means decode coded information from one format into another. It is used for Design of a combinational circuit.

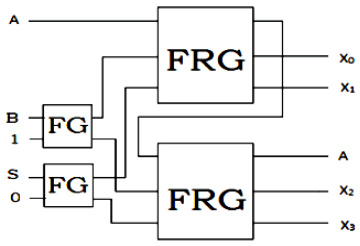


Fig-10: 2×4 Decoder

The previous model of 2×4 decoder is shown in Fig. 10. Replacing Fredkin gates with Peres gate, TR gate, NOT gate and CNOT gate from the design of 2×4 decoder the quantum cost can be reduced. The new design of 4×16 decoder using this new 2×4 decoder is shown in Fig 11.

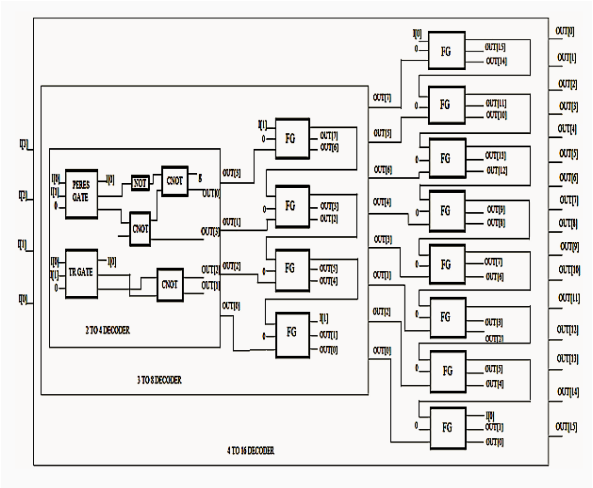


Fig- 11: 4×16 decoder

6. SIMULATION RESULTS

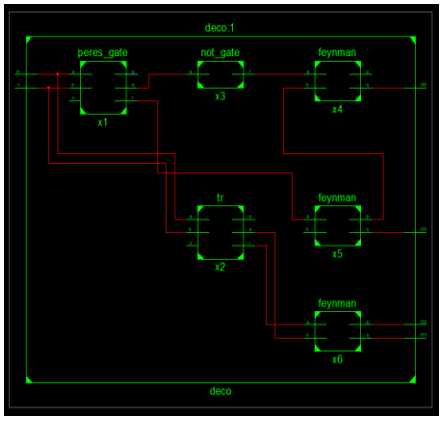


Fig- 12: RTL View of 2 ×4 Decoder

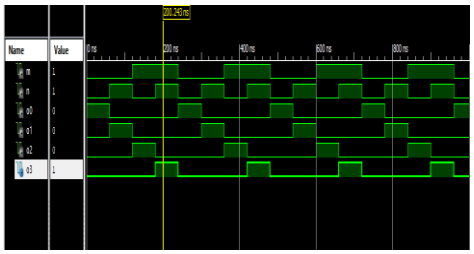


Fig-13: Output Waveform of 2 ×4 Decoder

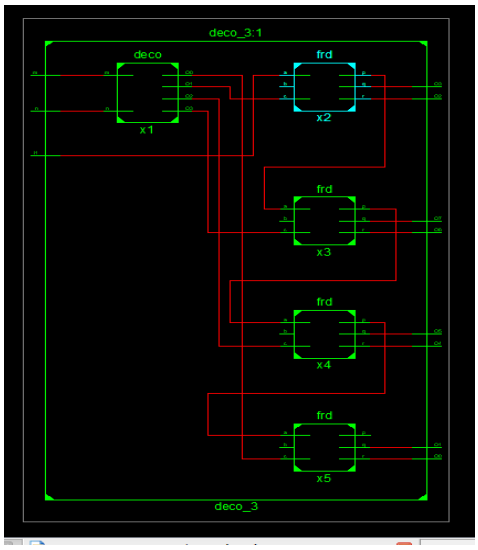


Fig- 14: RTL Viewof 3 × 8 Decoder

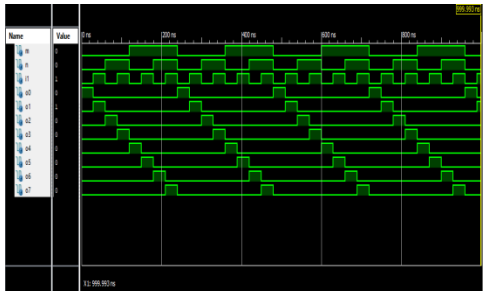


Fig-15: Output Wave form of 3 × 8 Decoder

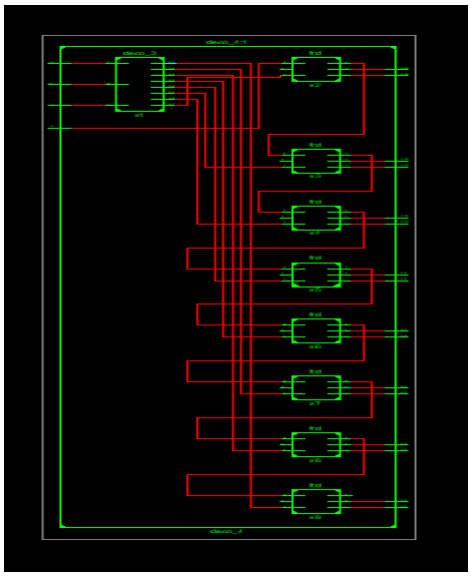


Fig-16: RTL View of 4 ×16 Decoder

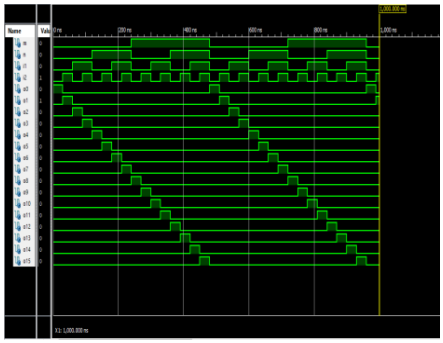


Fig-17: Output Waveform of 4×16 Decoder

7. COMPARATIVE STUDY

Design of reversible decoders are analyzed in terms of Quantum cost and Garbage outputs.

CIRCUIT	QUANTUM COST	GARBAGE OUTPUTS
2 TO 4 DECODER	11	3
3 TO 8 DECODER	31	4
4 TO 16 DECODER	71	5

8. CONCLUSION

Reversible gates can be used to minimize fan-out limitations, garbage outputs and quantum cost. Different combinational circuits like full adder, full subtractor, comparator, multiplexers can be constructed using reversible decoder with better performance.

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