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DESIGN OF SINGLE PHASE TRANSFORMERLESS INVERTER

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Abstract— *The transformerless inverters used in the grid connected photo voltaic (PV) system induce leakage current due to the absence of galvanic isolation and unstable common mode voltage. The leakage current is mainly depending on Common Mode Voltage (CMV).This can be eliminated for all modes of operation. Proper selection of common mode voltage (CMV) depends on selection of inverter topology. To eliminate the leakage current, the common mode voltage must be kept constant during all operation mode. . Even though, the leakage current can be reduced by using the H5 topology, it is still considered high due to the existence of junction capacitance in the switches during the freewheeling mode. The simulation of the proposed topology is carried out in MATLAB and validated experimentally. The results show that the H5 has lower leakage current as compared to the H6 and HERIC*

Key Words: **Transformerless inverter, Common mode voltage, Leakage current , MOSFET .**

1 INTRODUCTION

The PV renewable energy has become a more important electrical energy source within the entire energy market. The growth is mainly due to the reason that these systems have been constantly improving in terms of efficiency, power, reliability. The PV system can be designed in grid connected mode being the last one the most commonly used. The grid connected allows injecting the power generated into the electrical grid; in order to achieve this objective, the PV system is commonly set by using three stages: the PV array, the power converter and the grid filter with galvanic isolation. In the conventional PV systems, the last stage includes an LFT to link the converter with electrical grid to provide galvanic isolation. The main problem with the LFT is that it introduces around 2% of power losses in the system yielding low efficiency. Furthermore, the LFT increases the total cost of the system and the transformer size is big due to the operating frequency that coincides with frequency of the electrical grid which can be 50 or 60Hz. In order to solve the problem of transformer size, an HFT has been proposed as intermediate stage. However, the efficiency in this case is significantly reduced, not only because of the losses in the transformer but also because of the additional power stages that must be added in the power conversion process. Since the efficiency is one of the most important issues in a PV system, transformerless inverters are connected directly to the electrical grid, there is not galvanic isolation between the PV system and the electrical grid dealing in new issue can be solved. A PV solar panel naturally presents a stray capacitance which is formed between the PV cell and the grounded frame. Thus, when the PV generator is connected to the grid by means of a transformerless inverter, a leakage current can flow through the stray capacitance. Then the leakage current can generate additional power losses in the system and high risk of electrical shock for the users in contact with the PV installation. On the other hand, a resonant circuit is formed between the parasitic capacitances, the impedances of the ground path and the passive elements in the output filter of the converter. The resonant peak can reach high values yielding serious problems in the operation of the circuit. Unfortunately, the value of the stray capacitance depends on operational and whether conditions as: humidity, PV panel surface, the material used in the metallic frame and value in the passive elements of the power converter, therefore, it is not possible to precisely determine its value.

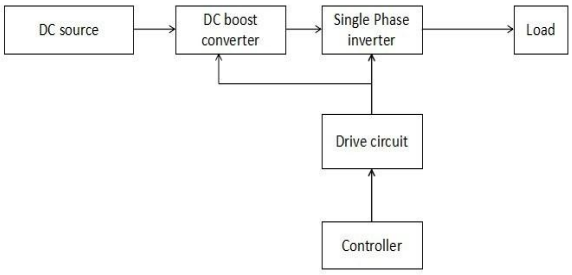

Fig 1: Block diagram

2 H5 TOPOLOGY

There are two outstanding single-phase transformerless inverter topologies in the market, called HERIC (Highly Efficiency and Reliable Inverter Concept) and H5.Compared to these topologies H5 topology is high efficiency, only one auxiliary switch and gating drives are needed. H5 topology has been well received in the PV market due to their very good performance regarding efficiency and CMV. It consists of five switches and four diodes. CPV is the parasitic capacitance between PV array and ground. The capacitance value depends on PV panel frame structure, weather conditions, and humidity and it is generally up to 50-150nF/kW.

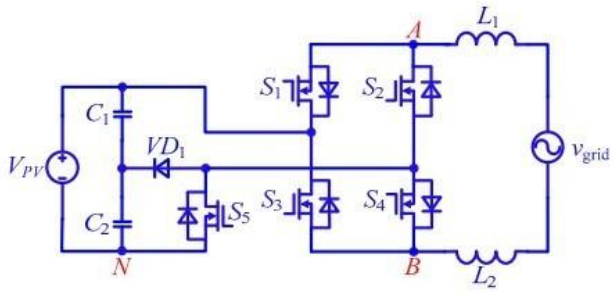

Fig2. Single Phase H5 Transformerless inverter

2.1 COMMON MODE VOLTAGE

Common mode voltage, to understand how the leakage current (also called as Common Mode Current (CMC) is generated through the parasitic capacitances. The project is about how the common mode voltage is directly related to the current generated in the ground path in the case of a transformer PV inverter. Before starting with analysis of a transformerless inverter, it is important to consider the circuit which is corresponds to a PV system with a LFT. In this circuit, the parasitic elements involved in the operation of the circuit are included in order to shown the possible paths for the common mode current. As can be observed in Fig.2.2, a possible path for the CMC between the electrical grid and the generator is through Ct. Ct is a parasitic capacitance located between the primary and the secondary winds in the Low Frequency Transformer. The typical value of these capacitances is in order of hundreds of Pico farads, thus, the impedance of this capacitances is high at the low and medium switching frequency range(<50Hz), therefore, the CMC through the ground path is strongly reduced. Then, if the system is designed with a LFT, the common mode behavior has no significant influence in the selection of the power converter topology and its modulation technique. On the other hand, if the LFT is omitted in the circuit as is depicted in Fig.3, then a path for the CMC exist.

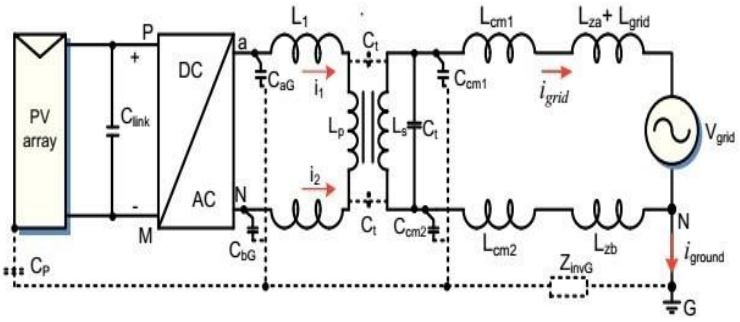

Fig.2.1: PV system with LFT including parasitic elements

A common mode model, of the transformerless converter can be derived from the circuit shown in Fig.4 as it can be observed, there are two main pulse voltage sources named VCMV corresponds to the CMV and Vs1, which represent the influence of the differential mode voltage (VDMV) in the common mode behavior. The total CMV represented by VCMV can be obtained by adding the above mentioned voltage source. According to the model, it can be easily derived that if the VCMV doesn't have high **dv/dt** (ideally constant), then no CMC will flow through the circuit**.**

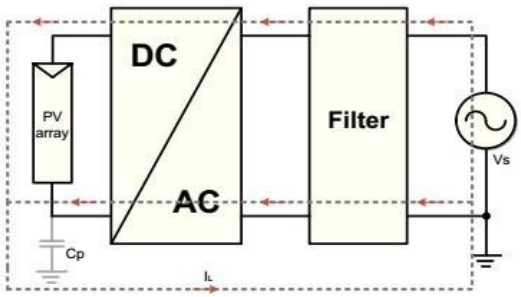

Fig2.2: Leakage ground current path in a transformerless PV inverter

In accordance with the common mode model and specially with the equation for the pulse voltage source Vs1, there is a

remarkable influence in the common mode behavior related to the position of the filter inductance, thus if the inductance is partition in two equal parts located in the line and neutral wires, then Vs1 will be close to zero, otherwise, Vs1 will influence the common voltage of transformerless inverter behavior.

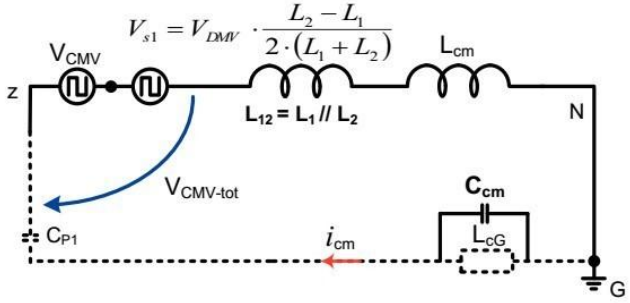

Fig 2.3: Common mode model for single phase transformerless inverter

3 MODE OF OPERATION FOR H5 TOPOLOGY

The operation principle contains four operation modes in each period of utility grid. The immediate common-mode voltage V_{CM} in the H5 topology: **$V_{CM}=0.5(V_{AN}+V_{BN})$**. In order to eliminate the leakage current, the common-mode voltage V_{CM} must be kept constant during all mode of operation

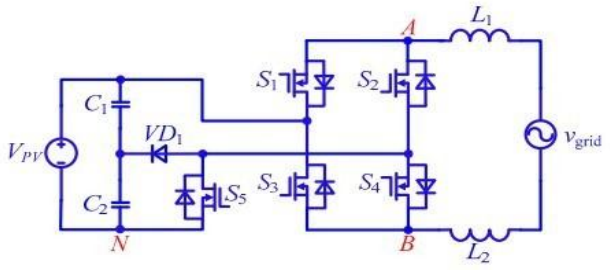

Fig 3: H5 Inverter

3.1MODE 1: CONDUCTION MODE DURING POSITIVE HALF CYCLE

In mode 1, S5, S1 and S4 are ON while S2 and S3 are OFF. Current increases and flow through S5, S1 and S4.$V_{AN}=U_{PV}$ and $V_{BN}=0$, VAB=UPV. Therefore, the V_{CM} and V_{DM} are calculated as

$$V_{CM} = U_{PV}/2$$

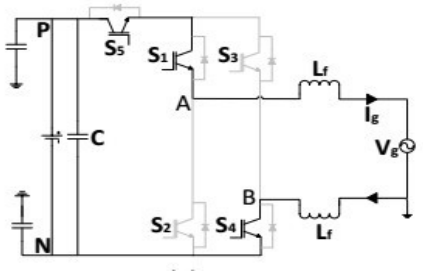

Fig3.1: Mode 1: Conduction mode during positive half cycle

3.2 MODE 2: MODE 2: FREEWHEELING MODE DURING POSITIVE HALF CYCLE

In mode 2, S5 and S4 are OFF while only S1 is ON. Current decreases and freewheels through S1 and anti-parallel diode of S3. V_{AN} decreases and V_{BN} increases until their values reach the common point, U_{PV} /2. The V_{CM} and V_{DM} are calculated as

$$V_{CM} = U_{PV}/2$$

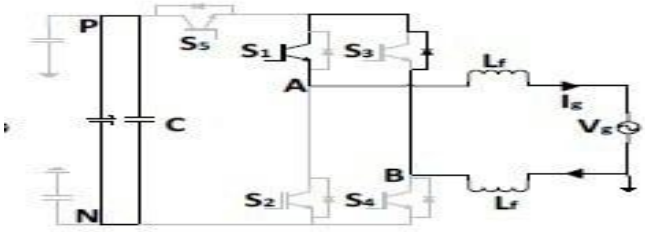

Fig3.2: Mode 2: Freewheeling mode during positive half cycle

3.3 MODE 3: MODE 3: CONDUCTION MODE DURING NEGATIVE HALF CYCLE

In mode 1, S5, S2 and S3 are ON while S1 and S4 are OFF. Current increases and flow through S5, S2 and S3.$V_{AN}=0$ and V_{BN} = U_{PV}, VAB=UPV. Therefore, the V_{CM} and V_{DM} are calculated as

$$V_{CM} = U_{PV}/2$$

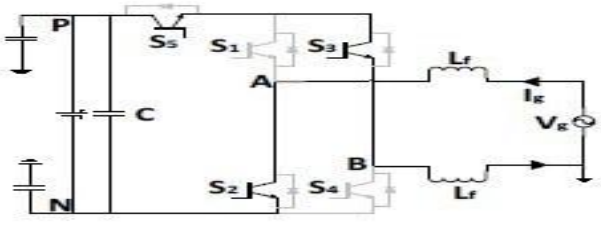

Fig3.3: Mode 3: Conduction mode during negative half cycle

3.4 MODE 4: FREEWHEELING MODE DURING NEGATIVE HALF CYCLE

In mode 2, S5 and S2 are OFF while only S3 is ON. Current decreases and freewheels through S3 and anti-parallel diode of S1. V_{AN} increases and V_{BN} decreases until their values reach the common point, U_{PV} /2. The V_{CM} and V_{DM} are calculated as

$$V_{CM} = U_{PV}/2$$

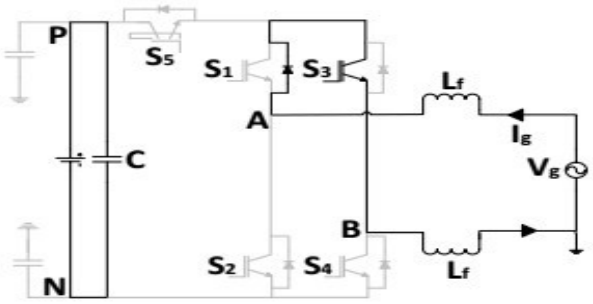

Fig3.4: Mode 4: Freewheeling mode during negative half cycle

For unity power factor operation, it is clear that H5 topology is able to generate unipolar PWM and CMV is constant.

3.5 SIMULATION OF H5 INVERTER

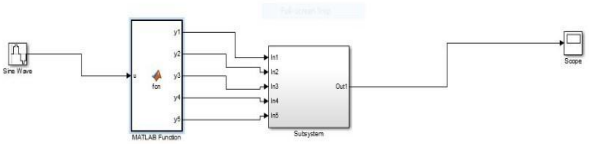

Fig3.5:Simulation of H5 inverter using MATLAB function

The DC input is given to the Matlab function block. The program for positive cycle and negative cycle is dumped in the Matlab function block. It consists of five switches y1, y2, y3, y4 and y5. Each switch has a phase angle and it is given to In1, In2, In3, In4 and In5 respectively in the subsystem. The output AC supply is obtained.

3.5.1 SUBSYSTEM OF H5 INVERTER

The detailed simulation of the H5 topology with all the components and switches is shown in the Fig.12. Temperature, saturation and linear are given as the input to the PV array system. Then the PV array is given as the input to all the five switches to which the inductor is connected. The voltage measurement is connected to the inductor and the scope is obtained.

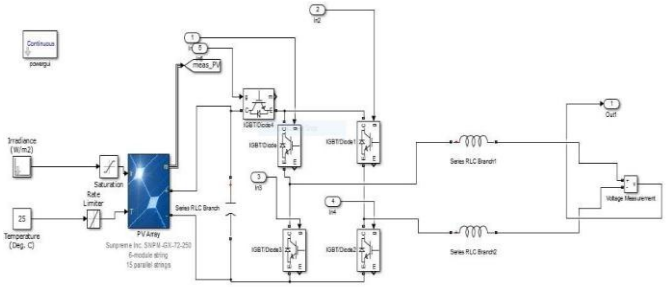

Fig3.6: Subsystem of H5 inverter using MATLAB function

3.5.2 MATLAB Function program

```
function [y1,y2,y3,y4,y5]  = fcn(u)

%Positive Cycle
        if(u>=0 && u<=1)
            y1=0; y2=0;y3=0; y4=0;y5=1;      %Vo=0
        elseif(u>=1 && u<=9)
            y1=1; y2=0;y3=0; y4=1;y5=1;      %Vo=+V1
        elseif(u>=9 && u<=10)
             y1=0; y2=0;y3=0; y4=0;y5=1;      %Vo=0
 %Negative Cycle
        elseif(u<=-0 && u>=-1)
            y1=0; y2=0;y3=0; y4=0;y5=1;      %Vo=0
        elseif(u<=-1 && u>=-9)
            y1=0; y2=1;y3=1; y4=0;y5=1;      %Vo=+V1
        elseif(u<=-9 && u>=-10)
             y1=0; y2=0;y3=0; y4=0;y5=1;      %Vo=0
        else
```

The above program is used to simulate H5 inverter based on switching ON and OFF condition. Simulation is carried out using MATLAB/ Simulink to analyze the theoretical analysis. The dc input and the output voltages are 33.9V and 230/50Hz respectively. The stray capacitance (CPV) is modeled with capacitor of 220nF. The filters are made up of two inductors (Lf), each has a value of 3mH. The switching frequency is 10 kHz. The methods are working properly under unity power factor. However, the conventional modulation methods are not operating correctly for non- unity power factor (lagging and leading power factor).

Current distortions are observed during negative power region. The leakage current is minimized and is kept within the permissible limit even during reactive power operation. With proposed modulation techniques, H5 topology is suitable for transformerless and reactive power applications without any modification on converter structures.

3.5.3 OUTPUT VOLTAGE WAVEFORM OF H5 TOPOLOGY

The output voltage waveform of H5 topology is shown in the Fig.3.6 with time period (ms) along x-axis and voltage (V) along y-axis.

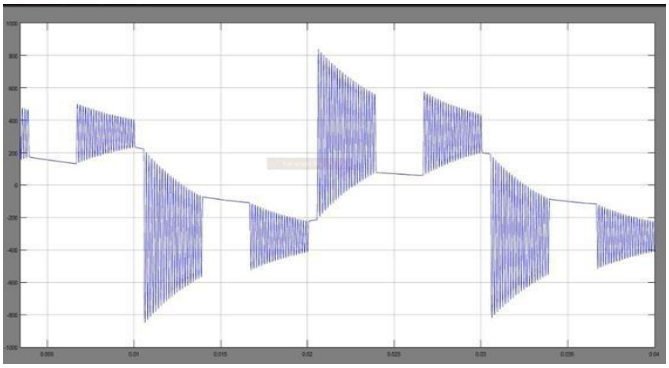

Fig3.7 Output waveform of H5 inverter topology

The output waveform depends on switching function. In all mode of operation, the common mode voltage is fixed as constant. It can be easily reduced leakage current.

3.5.4 LEAKAGE CURRENT OF H5 TOPOLOGY

The leakage current waveform of H5 topology is shown in the Fig.3.7 with time period (ms) along x-axis and current (mA) along y-axis.

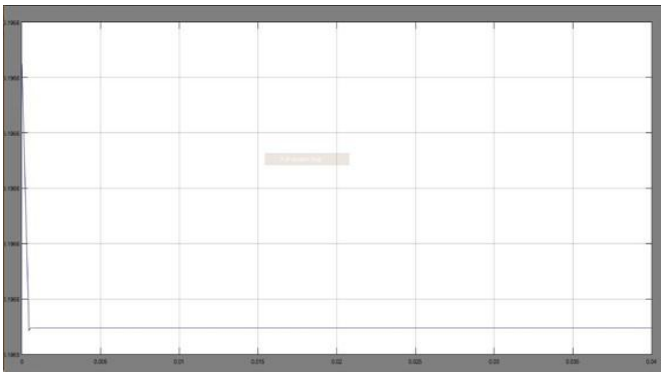

Fig3.8 Output waveform of leakage current

Based on the above waveform analysis, the common-mode voltage VCM of the H5 topology in each operation mode unchanged, and equal to 0.5UPV. Thus, the requirement for eliminating leakage current mentioned is fulfilled.

4. CONCLUSION

The single phase transformerless inverters used in the grid connected photo voltaic (PV) system induce leakage current due to the absence of galvanic isolation and unstable common mode voltage. The leakage current can be mainly depend on common mode voltage(CMV).This can be eliminated for all modes of operation. To eliminate the leakage current, the common mode voltage must be kept constant during all operation mode. The simulation of the proposed topology is carried out in MATLAB and validated experimentally. The results show that the H5 has lower leakage current as compared to the H6 and HERIC. The synchronization of the inverter output voltage with grid voltage shows clearly the target of attaining design was successful. The output current is varying and it depends on the load variation during simulation. The overall hardware circuitry for grid linked inverter can be made which will require very few components and will be cost effective and less in weight and its eliminates leakage current.

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