International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395-0056
Volume: 06 Issue: 02 | Feb 2019 www.irjet.net p-ISSN: 2395-0072

Digital and Implementation of Optimized DDS in FPGA

Satish Gavali[1], Ravichander J [2], Anantha Shayanam G R[3], Dr Shiva Yellampalli [4]

[1]6th Sem, MTech in VLSI Design & Embedded System, VTU regional Centre, UTL Technologies, Bengaluru,-22
[2]Global Head IT IS, Zensar, Technologies, Bengaluru, Karnataka India,
[3] Senior Scientist ISRO Satellite Centre Bengaluru, Karnataka India,
[4]Professor, Department of E&CE, VTU Extension Centre, UTL Technologies Ltd, Bengaluru,-22

Abstract - *This thesis discusses the work carried for the Design and Implementation of the optimized DDS in the FPGA. As compared with conventional analog implantation of frequency synthesizers imposes the lost implanting constraints in terms of frequency tuning and the spectral purity. These very much constrains in the advanced communications system where most of the operations are carried in the digital domain. Generation of Digital waveform using the FPGA based on the Lookup table approach. The requirement of generation of sinusoidal waveform with variable frequency places the major in applications field of digital signal processing.*

The implementation of the signal generation unit is based on the look up table approach. In very much desirable to reduce the hardware requirement. The DDS place the major in the application like software defined radios even its takes the small portion in the design of such applications. The implementation of DDS has lot of constraints in terms of area and speed requirement. There many approaches are available to implement the DDS based on the lookup table, CORDIC algorithm. But in these we used look up table method because of its performance for the high frequency applications by minimize the area usage by just storing the quarter waveform to derive both sine and cosine wave forms.

Computations to prototyping in the FPGA and is targeted to Xilinx xc3s1500-5fg676 FPGA. The computer simulation results obtained from Matlab and Modelsim are compared with the hardware implementations, the same has been illustrated.

Key Words*: *NCO, DDS, FPGA, Chipscope, Simulink, VHDL

1. Introduction

In today's high performance, cost-competitive, small sized package with functionally-integrated products are becoming more and more popular and alternative to conventional analog based synthesizer. Digital processing data such as lookup table techniques are used for direct digital synthesis to generate a tunable frequency as well as phase signal at the output of the circuit with the fixed précised constant frequency clock

source at the input. The précised input clock reference frequency is sampled in DDS system as a programmable binary word. The scaled binary word is 24 bits to 48 bits length typically, that enables greater output frequency with tuning resolution by this DDS Implementation.

The integration of Digital to Analog converter in DDS methodology in a single integrated chip (IC) enables the high speed, high-performance technology product drives many number of mission critical applications & provide an alternate to conventional based PLL synthesizer. (Below points chart down many important distinct advantages of DDS implementation for many applications as compared with the conventional agile analog PLL based frequency synthesizer). In this we implement the DDS algorithm in MATLAB for plotting the desired output and also aim in simulation and realized using VHDL, computations to prototyping is implemented in the FPGA and is targeted to Xilinx xc3s1500-5fg676 F PGA. The computer simulation results obtained from Matlab and Model sim are compared with the hardware implementations, the same has been illustrated.

2. Working Principle and Design

The basic working principle of this optimized DDS is obtained by just storing the quarter wavelength in the lookup table to generate the cosine and sine wave form, normally we split this quarter wave form in to two memory blocks so that the speed can be increased and overlap can be avoided,

By its design architecture, it consists of address counter, PROM, Digital to Analog converter and precision reference clock, basically two PROMs stores the half of the quarter cycle in each of sampled sine wave data in digital form. Because of storing the data in the PROM is placed as major role as a lookup table. The PROM location can be accessed by the address counter and data's can be read and feeds to the D/A converter, the input digital word from the PROM or lookup table will helps the Digital to Analog converter to generate an analog sine and cosine waves accordingly.

By its basic working principle, a DDS has a constant input reference clock, address block counter, PROM and Digital to Analog converter. In this technique PROM stores the quarter cycle of sine wave in the form of digital sampled data. Therefore the PROM is placed in this architecture as a lookup table. The PROM location can be accessed by the address counter and data's can be read and feeds to the D/A converter, the input digital word in the PROM will helps the D/A converter to generate an sinusoidal analog waveforms.

This system should have output analog fidelity, jitter as well as AC purity of this simple design architecture will be very good, and this has a drawback of tuning flexibility. This

system output frequency dependent on the input reference clock or by programming the PROM lookup table size. Neither input reference clock nor PROM size options support high-speed output frequency hopping.

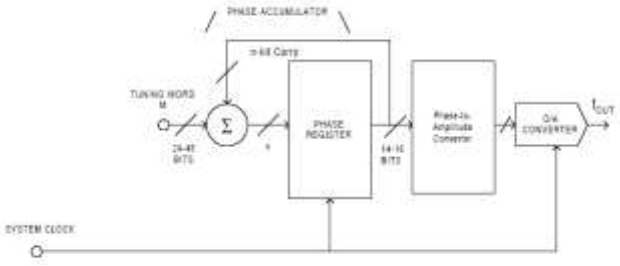

Figure.2.1 frequency tunable DDS system

In this architecture by introducing the function of phase accumulator in the DDS system architecture chain at the input, hence this system called as a numerically-controlled oscillator, this will be the heart of a DDS device. As in above figure 2.1 shows that the input N-bit counter variable and phase accumulator register are implemented in the design at early in the architecture before PROM sine table lookup, as the replacement for register based address counter. The function carry acts as "phase wheel" in the DDS design flow.

3. Matlab Implementation

Matlab is used for high level modeling and simulation to get the complete functionality and also the flow of DDS from Input system to till the end of system.

This figure 3.1 below illustrates the Matlab implementation of DDS it consists of constant (C), Adder (Add), Integer delay, Extract bits, Sine lookup table, Cos lookup table & finally the oscilloscope.

As in above Figure 3.1Accurate required frequencies will not be gained, because of the phase quantization of a signal for a given clock frequency in the system. The DAC accuracy or the number of bits expectable for quantizes at the output sine wave, with greater accuracy in the DACs block producing smoother sinusoidal waveforms.

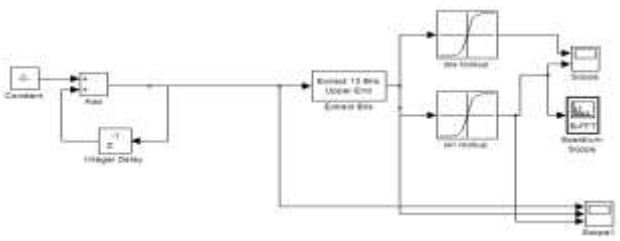

Figure. 3.1Matlab Implementation architecture

In order to design and develop an effective operation flow design from MATLAB to FPGA, which identified algorithm research for MATLAB and system equal language permits effective transition from development of algorithm, this thesis analyzes MATLAB as a development environment for implementing in FPGA.

In digital design communications system, there are two factors which influence the demanding in this generations are Accuracy as well as speed are the development trends. So to succeed these accuracy and speed trends one should gain the controllability, high precision and high carrier frequency signal and more particularly to produce the ideal sinusoidal waveforms which should varies according to the frequencies.

In digital system an output frequency of 10 MHz to generate with an input clock reference frequency signal of 50M Hz, a tuning frequency word 'M' of 51 is stored at the Phase Register block. The value tuning of the frequency word 'M' is calculated by using the frequency tuning equation. The Accumulator is 8-bits length. This 'M' control word is added to the previous value of Phase Accumulator with each input clock pulse.

MATLAB Output:-

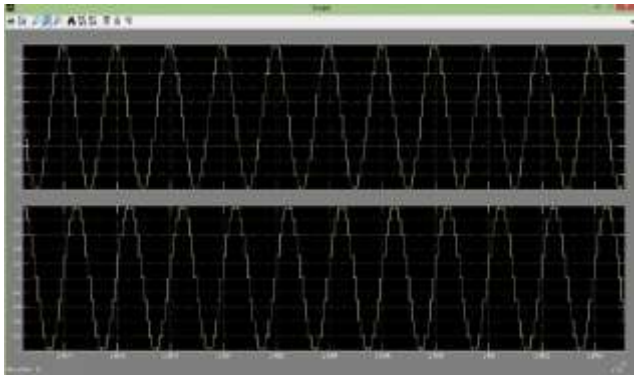

Figure.3.2 Matlab Output

4. FPGA Implementation

The Field programmable Gate Arrays (FPGAs) are electronically burns the memory blocks to get the required digital circuit system. The FPGAs delivers economical solution to the market by comparing with the Application Specific Integrated Circuits (ASIC) these normally required a lot of properties in terms of time and money to obtain first functional device. On the other hand FPGAs take a minute to design and configure also they cost somewhere around a few hundred dollars to a few thousand dollars. Also for changing requirements, any other upcoming developments the final upgraded operations can easily be promoted by just downloading a newly designed code bit stream.

Usually any device of FPGAs consists the following blocks:

• Programmable building logic blocks those are used for implementing logical operations.

• Programmable routing operation that inter-connects these logical blocks.

• Input/output building blocks were connected to logical blocks through routing interconnect and that Makes off-chip connections.

FPGA's and the CPLD's form the basic building blocks for all the programmable logics. The major reason making FPGA's more feasible than the complex programmable logic devices are that they can be configured at the gate level. Hence FPGA's find extensive application in VLSI domain also; these form the important feature of the reconfigurable devices which is the near future of VLSI industries.

5. Simulation & Results

In this chapter we discuss the Simulation of the thesis and their results. MATLAB Simulation is used to gain the DDS function and the way from the input towards output system at High-level. The thesis has also been simulated with the ModelSim simulator and modeled using Verilog. The FPGA kit can be used to synthesize the Verilog code. These simulation& results helps us to increase the working architecture of DDS system under practical design operations and results. Simulations on FPGA board are very important to function as a hardware prototype system before this really built

asreal hardware system. In this practical simulations will be used to comprehend non-ideal features of the structured design of DDS system on this output spectrum. Operation functionality of the DDS system has been illustrated in above chapters.

Table 1:Results comparison table

Sl No.	Parameters	Simple	Memory Optimized
1	Size	700.1	699.5
2	Speed	1300.1	1298.9
3	Power	3500.02	3513

6. Conclusion & Future work

In summary, this thesis Design and Implementation of the optimized DDS in the FPGA placed the necessary path to gain knowledge on designing and implementing any circuit for in FPGA, by considering a DDS as a model. This Design and Implementation of optimized DDS thesis started with few examples of Verilog codes those will be used at the HDL to design the digital circuits and continues in explaining the basic working principle of a DDS architecture. This one surveyed in an in-depth overview of the fundamentals on FPGA design. Above all chapters are very crucial for designing and implementation of any FPGA.

The Computations results and its VHDL implementation for prototyping in the FPGA is presented with experimental results are shown with graphs. This thesis explains through FPGA design flow diagram and an instantaneously showcased with screenshots to help orient the user.

Thus other future additional work on this project might requires executing DAC and LPF on to a single integrated ASIC platform to improve the performance, reduce the size, weight and compare it with an optimized DDS.

REFERENCES

[1] Analog Devices, "A technical tutorial on digital signal synthesis," Application Note, 1999. http://www.analog.com/static/importedfiles/tutorials/450968421DDS_Tutorial_rev12-2-99.pdf

[2] T. M. Comberiate, "Phase noise spur reduction in an array of direct digital synthesizers," M.S. thesis, University of Illinois at Urbana-Champaign, Urbana, IL, 2010.

[3] C. Shan, Z. Chen, H. Yuan and W. Hu, "Design and implementation of a FPGA-based direct digital synthesizer," in Electrical and Control Engineering (ICECE), 2011 International Conference, pp.614-617

[4] H. Omran, K. Sharaf, and M. Ibrahim, "An all-digital direct digital synthesizer fully implemented on FPGA," in Design and Test Workshop (IDT), 2009 4th International, pp.1-6

[5] Paolo Maffezzoni ,"Analysis of VCO Phase Noise in Charge-Pump Phase-Locked Loops "in IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS, VOL. 59, NO. 10, OCTOBER 2012

[6] P. Maffezzoni, D. D'Amore, and M. Santomauro, "Extracting oscillators phase-sensitivity to noise perturbations," in Proc. IEEE Eur. Conf.Circuit Theory Design (ECCTD), Linköping, Sweden, Aug. 29–31,2011, pp. 250–253.

[7] A. Tasic, W. A. Serdijn, and J. R. Long, "Spectral analysis of phase noise in bipolar LC-oscillators: Theory, verification, and design," IEEETrans. Circuits Syst. I: Reg. Papers, vol. 57, no. 4, pp. 737–751, Apr. 2010.