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Design of Energy Efficient 8T SRAM cell at 90nm Technology

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Abstract - *A novel 8-transistor (8T) static random access memory cell with improved data stability in subthreshold operation is designed. The proposed single-ended with dynamic feedback control 8T static RAM (SRAM) cell enhances the static noise margin (SNM) for ultralow power supply. It achieves write SNM of 1.4× and 1.28× as that of iso-area 6T and read-decoupled 8T (RD-8T), respectively, at 300 mV. The standard deviation of write SNM for 8T cell is reduced as that for 6T and RD-8T, respectively. It also possesses another striking feature of high read SNM as that of 5T, 6T, and RD-8T, respectively. The proposed 8T consumes less write power as that of 5T, 6T, and iso-area RD-8T, respectively. The power/energy consumption of 1-kb 8T SRAM array during read and writes operations minimized. These features enable ultralow power applications of 8T*.

Key Words: Single ended, static noise margin (SNM), static RAM (SRAM), sub-threshold, ultralow power.

1. INTRODUCTION

The growing demand of portable battery operated systems has made energy efficient processors a necessity. For applications like wearable computing energy efficiency takes top most priority. These embedded systems need repeated charging of their batteries. The problem is more severe in the wireless sensor networks which are deployed for monitoring the environmental parameters. These systems may not have access for recharging of batteries. We know that on chip memories determine the power dissipation of SoC chips. Hence it is very important to have low power and energy efficient and stable SRAM which is mainly used for on chip memories. There are various approaches that are adopted to reduce power dissipation, like design of circuits with power supply voltage scaling, power gating and drowsy method. Lower power supply voltage reduces the dynamic power in quadratic fashion and leakage power in exponential way. But power supply voltage scaling results in reduced noise margin. Many SRAM arrays are based on minimizing the active capacitance and reducing the swing voltage. In sub-100nm region leakage currents are mainly due to gate leakage and sub threshold leakage current. High dielectric constant gate technology decreases the gate leakage current. Forward body biasing methods and dual VT techniques are used to reduce sub threshold leakage current. In sub threshold SRAMs power supply voltage (VDD) is lower than the transistor threshold voltage (VT) and the sub threshold leakage current is the operating current.
The energy loss during writing is more than the energy loss during reading in conventional SRAM since there is full swing of voltage in bit lines whereas the bit line voltage swing is very less during reading. It is known that the energy stored in the bit lines of the conventional SRAM is lost to ground in each write operation during '1' to '0' transition and this is the main source of energy loss. The power dissipated in bit lines represents about 60% of the total dynamic power consumption during a write operation. The power consumption by bit lines during writing is proportional to the bit line capacitance, square of the bit line voltage and the frequency of writing. Energy loss is reduced by limiting voltage differences across conducting devices. This is accomplished through the use of time-varying voltage waveforms. This is also called Adiabatic charging technique. The SRAM working purely on adiabatic charging principles need multiple phase power clocks. Although there is huge saving in energy during writing as well as reading, the design of the SRAM circuit is complex and not same as the design of conventional SRAM. The latency of operation is more.

No separate pre charging circuit is used before or after reading. No synchronization circuit is needed as only bit lines are concerned. Low power sense amplifier is utilized to sense the data. The design of the conventional SRAM can be retained except the write driver and the pre charge circuit. With this adiabatic driver circuit working in conjunction with conventional 6T SRAM cell other performance characteristics like read stability, write ability, read and write delay etc., have been found by simulation in addition to energy saving under varied conditions of memory operations. The effect of device parameters of the driver on total energy of the SRAM cell has been investigated. Further studies covered proposed SRAM cell arrays.

In addition to recovering the energy from both bit lines the possibility of operating the SRAM cell with single bit line driven by an adiabatic driver is examined to save energy. This effort has resulted in realizing adiabatic 5T SRAM cell which consumes significantly lower energy than adiabatic 6TSRAM cell with reduction in bit line leakage power and with better Static Noise Margin (SNM).Single ended reading is employed and this does not need pre charging, which saves energy. Further the design of adiabatic 5T SRAM is modified to get Feat SRAM which has better speed of operation in addition to other performance parameters remaining almost the same.

All these investigations have been carried out using CADENCE tool with 90nm. The thesis deals with the description of the effort put in to arrive at energy efficient adiabatic 6T and 5TSRAM cells whose other performance characteristics are almost comparable to those of 6Tconventional SRAM cell.

2. LITERATURE REVIEW

2.1 6T and 5T SRAM Cell Topologies

The standard 6T SRAM is built up of two cross-coupled inverters (INV-1 and INV-2) and two access transistors (MA1 and MA2), connecting the cell to the bit lines (BL and BLB), as shown in Fig 1. The pair of cross coupled inverters is formed by a pair of load transistors (MP1 and MP2) and a pair of driver transistors (MN1 and MN2) that are stronger than the access transistors.

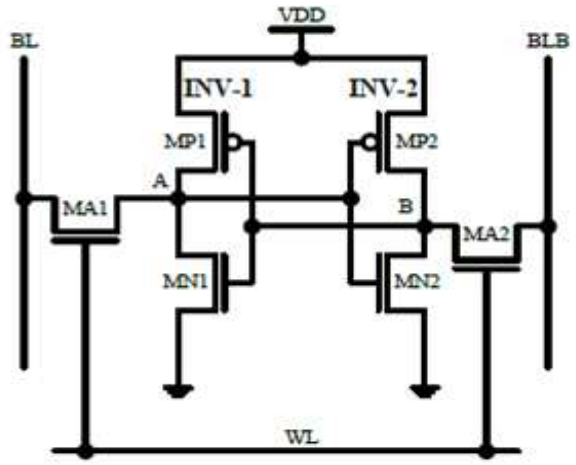

Fig -1: Circuit diagram of standard 6T SRAM cell

More specifically, the cross-coupled inverters of the memory cell have two storage nodes A and B functioning to store either logic '1' or logic '0'. The gates of access transistors are connected to a word line WL, and a rising transition on the word line to assert the access transistors during a read or a write operation.

At the end of the read and write operations, the word line WL is de-asserted to allow the cross-coupled inverters to function normally and hold the logic state of the storage nodes. A concern associated with the read operation is that because of the back-to-back connection of cross-coupled inverters, a regenerative action develops and node A is pulled high resulting in the destruction of contents in the bit cell. Especially, when logic '0' stored initially, the voltage rise in the cell may corrupt the data stored. Therefore, it is desirable to keep the voltage at the storage node which has logic '0' stored from rising above the trip-voltage of the inverter. To provide a non-destructive read operation, the cell ratio (CR) was conventionally varied from 1 to 2.5, where the W/L ratio of the driver transistor to the access transistor is referred to as the cell ratio. Similarly, for a successful write operation, both access transistors must be stronger than the load transistors.

The ratio of the load transistor to the access transistor is referred to as the pull-up ratio (PR). To improve the readability of an SRAM cell, cell ratio can be increased, while a lower pull-up ratio is desirable to improve the cell write ability.

3. PROPOSED SYSTEM

3.1 Introduction

The portable microprocessor controlled devices contain embedded memory, which represents a large portion of the system-on-chip (SoC). These portable systems need ultralow power consuming circuits to utilize battery for longer duration. The power consumption can be minimized using nonconventional device structures, new circuit topologies, and optimizing the architecture. Although, voltage scaling has led to circuit operation in subthreshold regime with minimum power consumption, but there is a disadvantage of exponential reduction in performance. The circuit operation in the subthreshold regime has paved path toward ultralow power embedded memories, mainly static RAMs (SRAMs) . However, in subthreshold regime, the data stability of SRAM cell is a severe problem and worsens with the scaling of MOSFET to sub-nanometer technology.

Due to these limitations it becomes difficult to operate the conventional 6-transistor (6T) cell at ultralow voltage (ULV) power supply. In addition, 6T has a severe problem of read disturb. The basic and an effective way to eliminate this problem is the decoupling of true storing node from the bit lines during the read operation in. This read decoupling approach is utilized by conventional 8-transistor [read decoupled 8-transistor (RD-8T) cell which offers read static noise margin (RSNM) comparable with hold static noise margin (HSNM) . However, RD-8T suffers from leakage introduced in read path. This leakage current increases with the scaling thereby, increasing the probability of failed read/write operations. Similar cells that maintain the cell current without disturbing the storage node are also proposed.

3.2 Proposed 8T SRAM Cell Design

To make a cell stable in all operations, single-ended with dynamic feedback control (SE-DFC) cell is presented in Fig. 2. The single-ended design is used to reduce the differential switching power during read–write operation. The power consumed during switching/toggling of data on single bit line is lesser than that on differential bit-line pair.

The SE-DFC enables writing through single nMOS in 8T. It also separates the read and write path and exhibits read decoupling. The structural change of cell is considered to enhance the immunity against the process–voltage–temperature (PVT) variations. It improves the static noise margin (SNM) of 8T cell in subthreshold/near-threshold region. The proposed 8T has one cross coupled inverter pair, in which each inverter is made up of three cascaded transistors.

These two stacked cross-coupled inverters: M1–M2–M4 and M8–M6–M5 retain the data during hold mode.
The write word line (WWL) controls only one nMOS transistor M7, used to transfer the data from single write bit line (WBL). A separate read bit line (RBL) is used to transfer

the data from cell to the output when read word line (RWL) is activated. Two columns biased feedback control signals: FCS1 and FCS2 lines are used to control the feedback cutting transistors: M6 and M2, respectively.

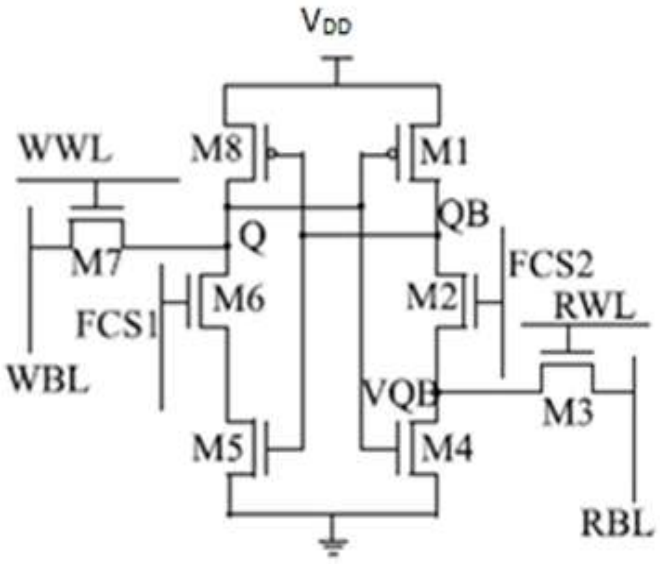

Fig -2: Proposed 8T Design

3.3 Write Operation

The feedback cutting scheme is used to write into 8T. In this scheme, during write 1 operation FCS1 is made low which switches OFF M6. When the RWL is made low and FCS2 high, M2 conducts connecting Complementary Q (QB) to the ground. Now, if the data applied to word bit line (WBL) is 1 and WWL is activated (Table I), then current flows from WBL to Q and creates a voltage hike on Q via M7-writing 1 into the cell. Moreover, when Q changes its state from 0 to 1, the inverter (M1–M2–M4) changes the state of QB from 1 to 0. To write a 0at Q, WWL is made high, FCS2 low and WBL is pulled to the ground. The low going FCS2 leaves QB floating, which can go to a small negative value, and then the current from pull-up MOS M1 charges QB to 1. The WT is measured as the time taken by WWL signal-to-rise to VDD/2 until the storage nodes intersect each other. The simulations for WT were performed at all process corners. The WT (for write 1 and write 0) for 8T increases with the decrease in power supply. The WT is highest for slow nMOS and slow pMOS (SS) worst case corner, as shown in fig. During write 1/0 operation, the power consumption of 8T is highest for fast nMOS and fast pMOS (FF) process corner dominated by the fast switching activities (Fig. 2). As write 0 operations is faster than write 1, the write 0 power consumption during write 0 is more as compared with that of write 1.

3.4 Read Operation

The read operation is performed by pre-charging the RBL and activating RWL. If 1 is stored at node Q then, M4 turns ON and makes a low resistive path for the flow of cell current through RBL to ground. This discharges RBL quickly to ground, which can be sensed by the full swing inverter sense amplifier. Since WWL, FCS1, and FCS2 were made low during the read operation (Table II), therefore, there is no direct disturbance on true storing node QB during reading the cell.

The low going FCS2 leaves QB floating, which goes to a negative value then comes back to its original 0 value after successful read operation. If Q is high then, the size ratio of M3 and M4 will govern the read current and the voltage difference on RBL. During read 0 operations, Q is 0 and RBL holds precharged high value and the inverter sense amplifier gives 0 at output. Since M2 is OFF so virtual QB (VQB) is isolated from QB and this prevents the chance of disturbance in QB node voltage which ultimately reduces the read failure probability and improves the RSNM. During read operation, if FCS1/FCS2 turns 1 before RWL is turned 0 then QB and VQB can share charge. As WWL is 0 no strong path exists between WBL and Q, and any disturbance in QB will not affect respective states (Q = 1 and QB = 0).The read time is measured as the time the RWL signal is activated until the RBL is discharged to 90%.

Table -1: Operation Table of Proposed 8T SRAM Cell

	Write '1'	Write '0'	Row half selected		Column half Selected	
			Write	Read	Write	Read
WWL	1	1	1	0	0	0
RWL	0	0	0	1	0	0
FCS1	0	1	1	1	1	0
FCS2	1	0	1	1	0	0
WBL	1	0	1	1	1	1
RBL	1	1	1	1	1	1

4. RESULTS AND DISCUSSIONS

4.1 Simulation Results

The simulation results for SRAM designs along with conventional were shown in table 2.

Table -2: Simulation analysis of various SRAM cells

Design	6T	5T	RD-8T	Proposed
Area (μm^2)	1.4	1.2	2.1	3.36

The circuit diagram, post layout waveform and layout of proposed SRAM cell were shown in figure 3, 4 and 5 respectively.

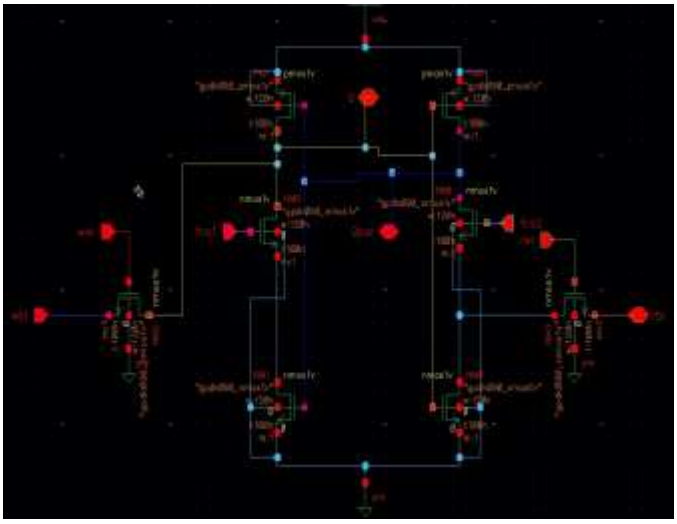

Fig -3: Circuit diagram of proposed SRAM cell.

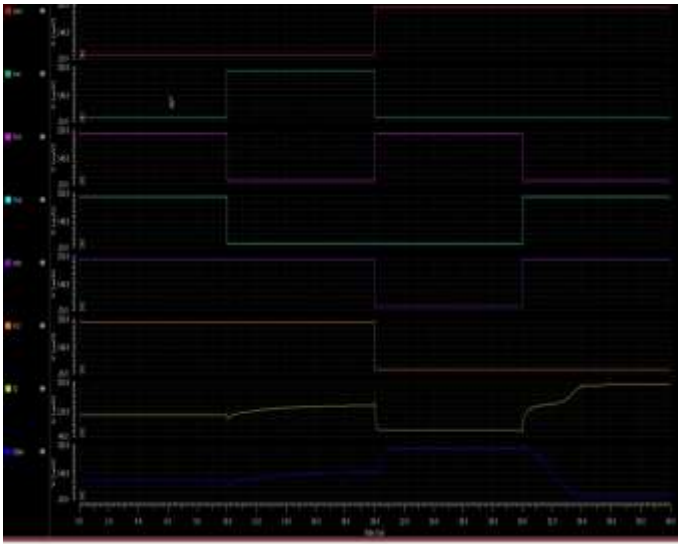

Fig -4: Post layout waveform of proposed SRAM cell

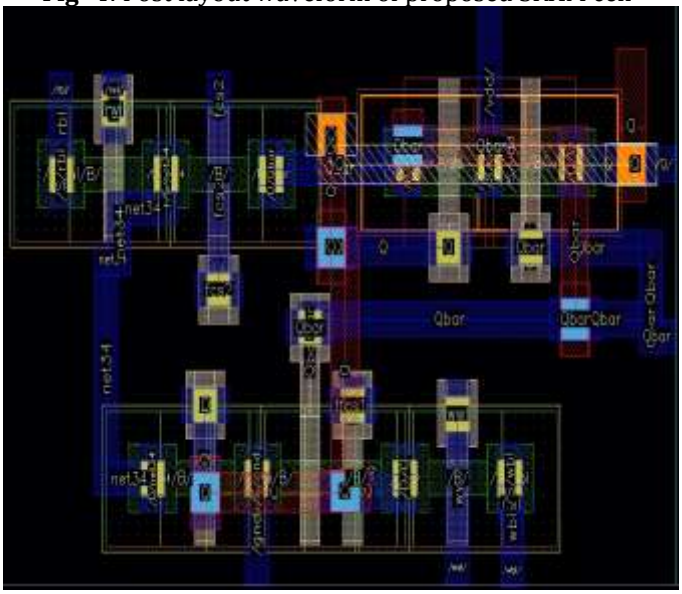

Fig -5: Layout of proposed SRAM cell

4.2 Complete Analysis

The graph shown below gives the complete analysis for the Power, Delay (ns), Energy and Static noise margin of 6T, 5T, RD-8T and the proposed system. The power for 6T is 19nW, for 5T is 21nW, for RD-8T is 24nW and the proposed system power used is 8nW. The delay for 6T is 9ns, for 5T is 8ns, for RD-8T is 21ns and the proposed system is 24ns. The Energy and static noise margin for 6T, for 5T, for RD-8T and the proposed system were depicted in the following Fig 6.

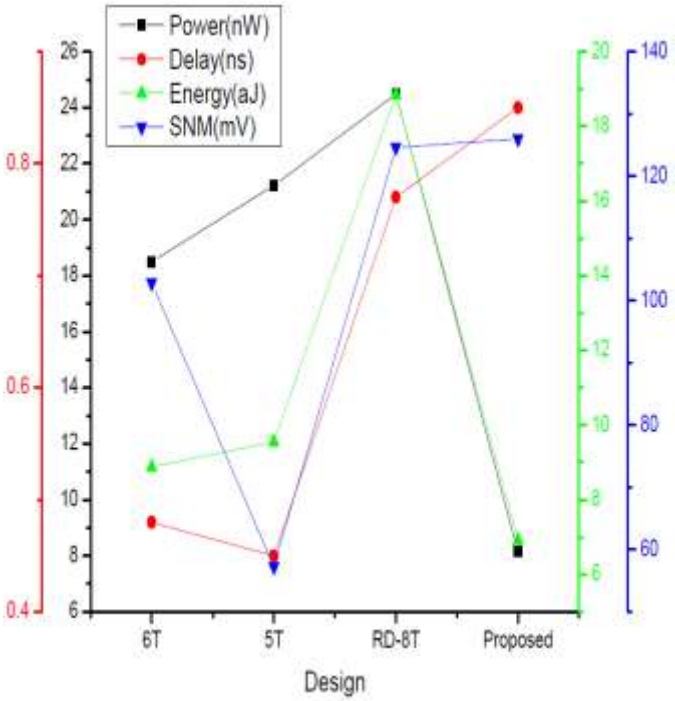

Fig -6: The Complete analysis of proposed SRAM cell

Table 3 shows the different metrics for various SRAM cells.

Table 3. Complete analysis of various SRAM cells

Design	Power (nW)	Delay (ns)	Energy (aj)	SNM (mV)
6T	18.5	0.48	8.88	102.87
5T	21.23	0.45	9.55	57.27
RD-8T	24.48	0.77	18.849	124.6
Proposed	8.15	0.85	6.927	126

5. CONCLUSION

An 8T SRAM cell with high data stability (high μ and low σ) that operates in ULV supplies is presented and attained enhanced SNM in subthreshold regime using SE-DFC and read decoupling schemes. The proposed cell's area is 2.5 times as that of 6T. Still, it's better built-in process tolerance and dynamic voltage applicability enables it to be employed similar to cells (8T, 9T, and 10T). The proposed 8T cell has high stability and can be operated at ULV of 200–300 mV

power supplies. The advantage of reduced power consumption of the proposed 8T cell enables it to be employed for battery operated SoC design.

REFERENCES

1) C.B. Kushwash and S.K. Vishwakarma, "A Single-Ended With Dynamic Feedback Control 8T Subthreshold SRAM Cell" IEEE VLSI Systems vol 24, No 1 January 2017, pp.373-377.

2) K. Roy and S. Prasad, Low-Power CMOS VLSI Circuit Design, 1st ed. New York, NY, USA: Wiley, 2000.

3) N. Verma and A. P. Chandrakasan, "A 256 kb 65 nm 8T subthreshold SRAM employing sense-amplifier redundancy," IEEE J. Solid-State Circuits, vol. 43, no. 1, pp. 141–149, Jan. 2008.

4) C. Kushwah and S. K. Vishvakarma, "Ultra-low power sub-threshold SRAM cell design to improve read static noise margin," in Progress in VLSI Design and Test (Lecture Notes in Computer Science), vol. 7373. Berlin, Germany: Springer-Verlag, 2012, pp. 139–146.

5) B. H. Calhoun and A. P. Chandrakasan, "A 256-kb 65-nm sub-threshold SRAM design for ultra-low-voltage operation," IEEE J. Solid-State Circuits, vol. 42, no. 3, pp. 680–688, Mar. 2007.

6) C. B. Kushwah, D. Dwivedi, and N. Sathisha, "8T based SRAM cell and related method," U.S. Patent IN920 130 218 US1, May 30, 2013.

7) J. P. Kulkarni, K. Kim, and K. Roy, "A 160 mV robust Schmitt trigger based subthreshold SRAM," IEEE J. Solid-State Circuits, vol. 42, no. 10, pp. 2303–2313, Oct. 2007.

8) C.-H. Lo and S.-Y. Huang, "P-P-N based 10T SRAM cell for lowleakage and resilient subthreshold operation," IEEE J. Solid-State Circuits, vol. 46, no. 3, pp. 695–704, Mar. 2011.

9) I. Carlson, S. Andersson, S. Natarajan, and A. Alvandpour, "A high density, low leakage, 5T SRAM for embedded caches," in Proc. 30th Eur. Solid-State Circuits Conf., Sep. 2004, pp. 215–218.

10) B. Zhai, S. Hanson, D. Blaauw, and D. Sylvester, "A variation-tolerant sub-200 mV 6-T subthreshold SRAM," IEEE J. Solid-State Circuits, vol. 43, no. 10, pp. 2338–2348, Oct. 2008.

11) S. A. Tawfik and V. Kursun, "Low power and robust 7T dual-Vt SRAM circuit," in Proc. IEEE Int. Symp. Circuits Syst., May 2008, pp. 1452– 1455.