Design of Power Efficient Johnson Counter

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Abstract - *The main design accent is power minimization in VLSI circuits as chip size is continuously decreasing. In order to design an efficient digital system, you need to reduce power consumption of all its components. As counter is a basic building block to design a digital system. In this paper implementation of 4-bit Johnson counter has been done using BICMOS logic, which is a combination of Bipolar and CMOS transistors. The aim of using BICMOS logic is to combine the advantages of both the logics. This proposed circuit is implemented using Cadence Virtuoso schematic editor and Cadence Virtuoso analog design environment is used for the simulation process. Calculation of power consumption at certain frequencies has been done for the circuit and compared the results with prior implemented research results. After the comparative analysis we came to the conclusion that this proposed counter circuit has low power consumption as compared to other circuits.*

Keywords: BICMOS, Master-Slave D flip flop, Latch up, Cadence, Johnson counter.

1. INTRODUCTION

The main design concern in VLSI circuits with the increase in operating frequency and downscaling of chip size is power minimization. Counter is a basic element to implement any digital system. Johnson counter generates a particular data sequence in response to number of time an event occurred.

Here a 4-bit Johnson counter has been implemented using BICMOS logic and calculation of power consumption at different frequencies for the proposed circuit has done and compare with previously done research results. So, we can get efficient counter circuit in terms of power. To implement this circuit Cadence EDA tool has used, in which Cadence Virtuoso schematic editor provide advanced capabilities of speed and ease the design. BICMOS logic is the combination of Bipolar and CMOS transistor logic. This logic has used to implement fast and low power circuits. Some disadvantages of CMOS logic are high propagation delay because of large interconnect capacitances and latch up condition but importantly the advantage is low power dissipation than BJT logic. Bipolar logic has advantages like high current driving capabilities and high speed compared to CMOS logic. Advantages of both the logics can combine with BICMOS configuration because it is the combination of both BJT & CMOS logics. Problem of latch up can be completely eliminated by using BICMOS logic.[1]

In prior done research work, several circuits of counter have been implemented using different techniques aiming on improving power consumption.

In [1], Divya Bora et.al. used BICMOS technology to design and simulate some of the digital circuits such as logic gates, half adder and full adder on Tanner EDA tool. All of these circuits have certain advantages like fast switching, high gain, large load driving capability, low output impedance and low static power because of using BICMOS logic for designing. Also latch up condition can be completely eliminated.

In [2], Saumya Pandey et.al. Designed 4-bit Johnson Counter on Tanner EDA using 90nm CMOS technology. GDI based clock gated logic and pulse-triggered flip flop has used to implement this circuit. This proposed circuit has power dissipation from 36.68µW (at 600MHz) to 54.69µW(at 1GHz).

In [3], Veena Battula et.al. Implemented a 4-bit Johnson counter using diode-free adiabatic logic(DFAL) on cadence using 90nm technology. Power dissipation for this proposed circuit has been calculated with different frequencies at different load capacitance.

In [4], Chandra shekhar kotikalapudi et.al. Proposed a 4-bit up-down Johnson counter. To reduce the power consumption, this design is embedded with a technique named Dual Dynamic Node Pulsed Flip-flop(DDFF) using logic module(DDFF-ELM) then incorporated with clock gating to reduce more power consumption. This proposed circuit without clock gating produce 344.24 µw power consumption and with clock gating produce 160.56 µw power consumption.

In [5], Abhishek Rai et.al. Proposed a design of 4-bit Johnson ring counter using microwind tool at 90nm technology and negative edge triggered D flip-flop has been used to implement this circuit. The purpose of doing this is to reduce area & power consumption of counter. Here the Auto-generated layout design has power dissipation of 25.095µW and semi-custom layout design has power dissipation of 139µW.

In [6], Ranjana Yadav et. al. proposed a low power Johnson Counter using MTCMOS technique. Comparative analysis of power dissipation at certain frequencies and power delay product has done and results were compared with conventional design.

In [7], M. R.Sangameswari et. al. implemented a 4-bit Johnson up-down counter which embedded low power dual dynamic node hybrid flip-flop (DDFF) & novel dual mode logic (DML). This improves the performance in terms of speed and also reduction in significant energy consumption.

In this paper a Johnson counter has been implemented using BICMOS logic. Section 2 explains the proposed counter circuit. Section 3 showing implemented schematic diagrams of counter and its components using Cadence Virtuoso schematic editor. In Section 4 execution & analysation of simulation results have done and Section 5 concluded the paper.

2. PROPOSED COUNTER

Proposed Johnson counter circuit shown in figure 1. It is the circuit in which inverted output of last flip flop has given to the input of first flip flop. For the implementation of Johnson counter we need to design separate components of the counter individually using BICMOS logic and later use all the components jointly to design the counter.
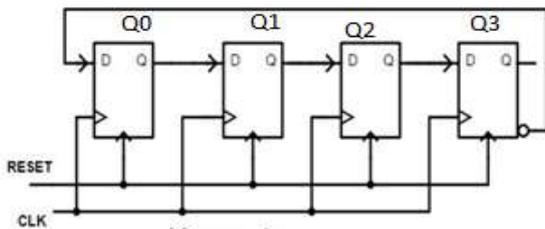
Figure 1: Circuit diagram of Johnson counter

Master-slave D flip flop is shown in figure 2. In this circuit when we need to disable the inputs by using either clock or inverted clock then to hold the output, clock inverter is used. At the input terminal PMOS MP3 has been used at the gate node of device to prevent the glitches. When input is low and clock is high, then there can be possibility of glitches. This completely abolished the need of clock inverter at the input. This phenomenon is useful for reducing delay & area of the circuit. There is a need of controlling the PMOS in feedback switch, which has done by feedback inverter. To steer the NMOS pull down section has used, which is for shunting the BJT. A feedback switch has connected in series with another switch and by making this arrangement pull down network is constructed. Both switches are directed by clock and the input. If in case, there is any occurrence of clock skew then also there is no abasement in this BICMOS circuit. Nevertheless, if the supply voltage is low then also this circuit will always have smaller area and fast output response.
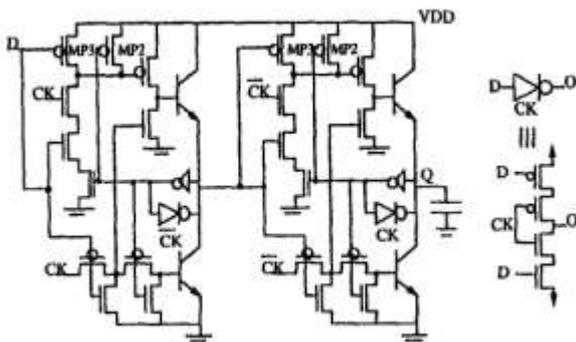

Figure 2: Master- Slave D flip flop implemented with BICMOS logic

3. SCHEMATIC DESIGN

For execution of counter we required to create instances of its components singly and finally use all the components simultaneously. Schematic diagrams of NOT gate, AND gate, XOR gate and Johnson counter have been implemented using Cadence Virtuoso schematic editor of Cadence tool. All these schematic diagrams have shown in following figures. All circuits are designed using BICMOS logic with subsequent specification: Length L=180nm, Width W= 2 μm. Figure 3 represents schematic diagram of inverter which is having 1 PMOS, 3 NMOS and 2 BJT. Figure 4 represents schematic diagram of AND gate which is having 3 PMOS, 5 NMOS and 2 BJT. Figure 4 represents schematic diagram of XOR gate which is having 6 PMOS, 8 NMOS and 2 BJT. Later on use all these components jointly to implement the schematic of counter.
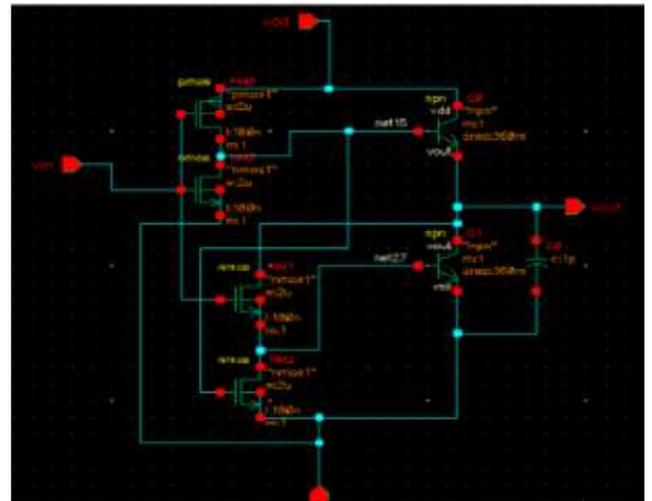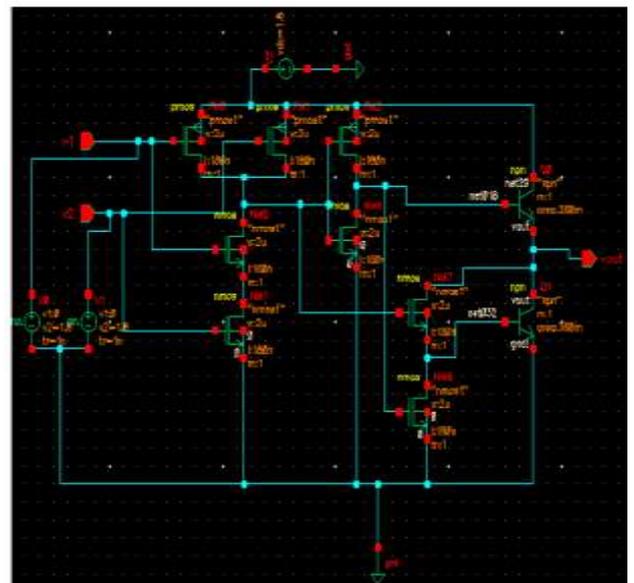

Figure 3: Schematic diagram of Inverter

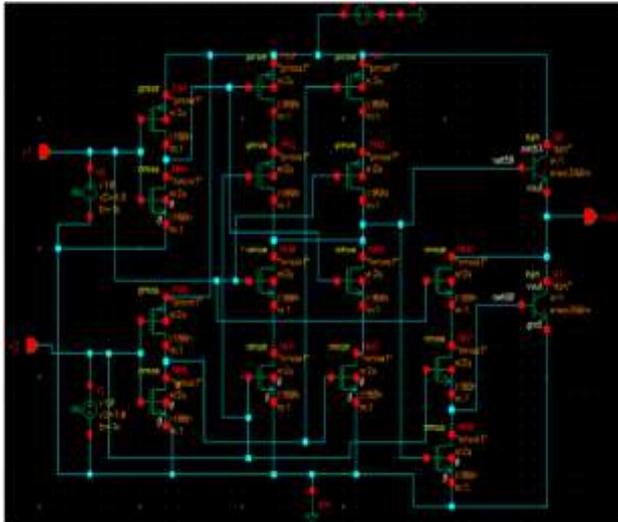**Figure 4:** Schematic diagram of AND gate

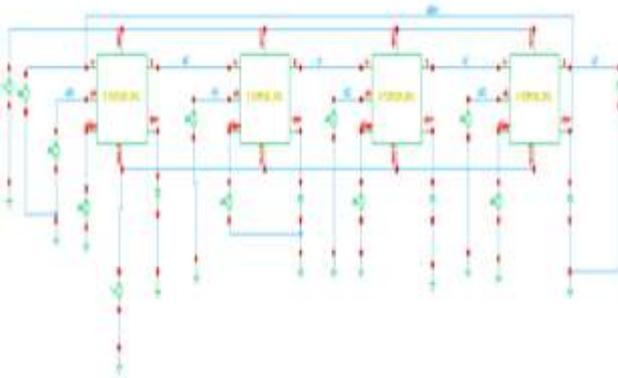**Figure 5:** Schematic diagram of XOR gate

Figure 6: Schematic diagram of Johnson counter

4. SIMULATION RESULTS

To simulate the schematics of Johnson counter along with its design components and for analysation of transient responses, Cadence design environment has been used. Simulation results are important for validating their logic and characteristics. Calculation of estimated power has done after the analysation of simulation results at certain frequencies.
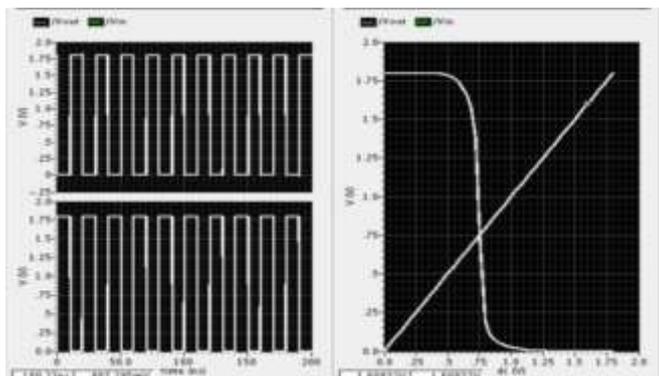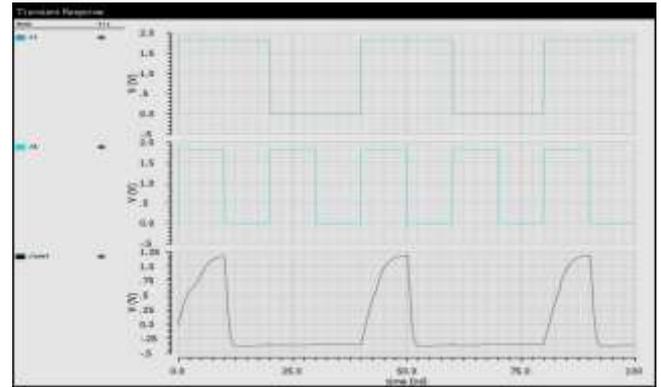

Figure 7: Simulation Result of Inverter

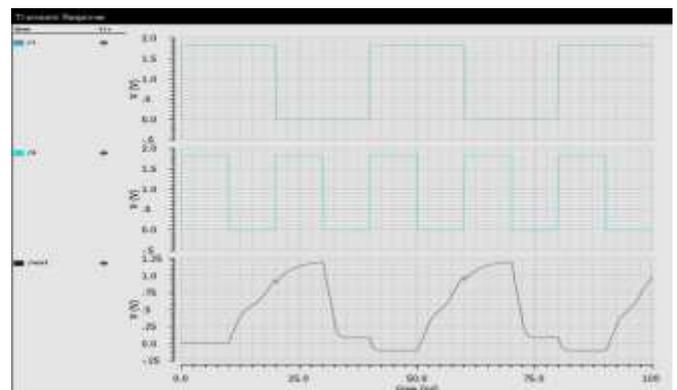**Figure 8:** Simulation Result of AND gate

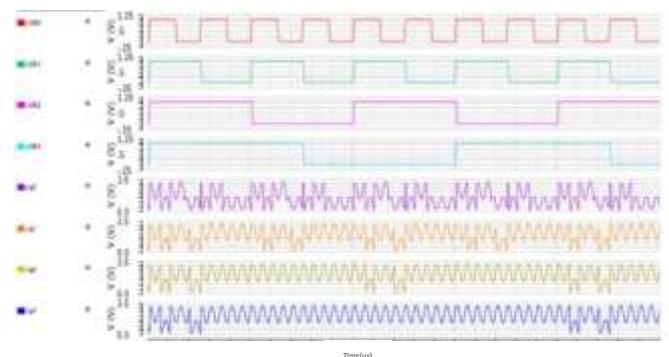**Figure 9:** Simulation result of XOR gate

Figure 10: Simulation Result of Counter

5. CONCLUSION

The main concern in recent VLSI designing is to reduce power consumption and implement a power efficient circuit. As counter is a basic element for any digital circuit, in this paper BICMOS logic is used to design a power efficient Johnson counter. Simulation & analysation of circuit on the basis of its power estimation at different frequencies have done using cadence tool. When results of this proposed counter have been compared with the counter circuit implemented with conventional logic & MTCMOS logic [6], we came to the conclusion that proposed counter circuit has less power consumption. Comparison results for power consumption at certain frequencies have shown in following table.

Table1: Comparison between Proposed counter Results and   Previous Research Results

Frequency (MHZ)	Power Consumption		
	Conventional Johnson Counter (µw)	MTCMOS Johnson Counter (µw)	Proposed Johnson Counter (µw)
600	161	97	85
700	187	112	92
800	218	128	102
900	241	143	110

REFERENCES

[1]   Divya Bora, Dr. U. M. Gokhale, "Design of Different Devices using BICMOS Logic", International Journal of Latest Research in Engineering and Technology (IJLRET),(2016), vol. 2,issue 5, page 69-73.

[2] Saumya Pandey, Sarita Uniyal, Dr. Nidhi Goel, "An Improved Low Power Johnson Counter Design with Clock Gating", International Journal of Electronics & Communication Technology (IJECT), (2015), vol. 6, issue 4, page 9-13.

[3] Veena Battula, Vishal Moyal, "Low Power Dissipation in Johnson Counter using DFAL Technique", International Journal on Recent and Innovation Trends in Computing and Communication, (2017),vol. 5, issue 1, page 244-247.

[4]   Chandra shekhar kotikalapudi, Smt. P. Pushpalatha, "Low Power Design of Johnson Counter Using DDFF Featuring Efficient Embedded Logic and Clock Gating", International Journal of Engineering Research and General Science, (2014), vol. 2, issue 5, page 572-579.

[5] Abhishek Rai, Rajesh Mehra, "Optimized Design and Simulation of 4-Bit Johnson Ring Counter Using 90nm Technology", International Journal of Research in Advent Technology, (2018), vol. 16, no. 6, page 1002-1006.

[6] Ranjana Yadav, Alka Agrawal, "Design and Analysis of Low Power Johnson Counter with Improved Performance using MTCMOS and Clock Gating", International Journal of Science Technology & Engineering (2016),vol. 2, issue 12, page 277-280.

[7]   M. R.Sangameswari, V.Vishnuprasath, "Low power – high speed design of counter using DDff and dual mode logic", International Journal of Science, Engineering and Technology Research (IJSETR), (2015), vol.4,issue 4, page 1203-1210.

[8] Neil H. E. Weste, David Harris and Ayan Banerjee, CMOS VLSI Design , 3rd edition, Dorling Kindersley Pvt. Ltd. 2006.