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EMBEDDED MODELLING AND CONTROL OF ASYMMETRIC CASCADED MULTILEVEL INVERTER

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Abstract - *The multilevel inverter is one of the power electronic converters which are used for medium voltage and high power applications with the additional remuneration of lesser total harmonic distortion and lower switching stress, hence reducing the size of the filter and bypassing the usage of the bulk input transformer. It produces the staircase AC output voltage from the input DC sources. Multilevel inverters can be divided into two classes such as Asymmetric multilevel inverter and Symmetric multilevel inverter. The proposed multilevel inverter is an asymmetrical type. Advanced pulse width modulation design is appropriated. In this paper, a new asymmetrical three-phase multilevel inverter is proposed using trinary DC source cascaded H Bridge. This trinary DC source cascaded H Bridge can provide nine level output voltage and it has experimented with both R and RL load. The simulation of a suggested three-phase multilevel inverter is tested using MATLAB-SIMULINK. This method is predictable to be helpful for higher power and higher voltage applications.*

Key Words: Multilevel inverter, pulse width modulation, total harmonic distortion, cascaded h-bridge multilevel inverter, trinary DC source.

1. INTRODUCTION

The need for a high power converter in the application has developed in modern years. Multilevel inverters have installed as easy replacements of a low power converter in many applications. The multilevel inverter includes a group of power semiconductor devices and a collection of source voltage equipment like capacitors or independent sources. The basic concept of certain inverters depends on the connection of series/parallel of power semiconductor devices and input DC sources to produce a stepped or staircase output voltage waveform. The multilevel inverter performs an extraordinary role in improving the perfection of high power and medium voltage distribution networks, high power conditioning systems, flexible speed drive systems etc [1]. The included system was suggested for eliminating the harmonics of asymmetrical cascade H-bridge multilevel inverter has explained. The suggested included system was combined with two intelligence methods that were fuzzy logic and PSO algorithm. The harmonic elimination concert of the approved system was reviewed with the seventh level asymmetrical cascade multilevel inverter (ACMLI). An automated controller has analyzed for two and a three-level inverter which has modified to work on an asymmetrical nine level active power filter. The controller has now excellent to make all required assignments for the perfect operation of the active power filter, such as current harmonic elimination and removal of larger frequency noise. The below-switching frequency response of nine level inverters was a fundamental benefit in the performance of the automated controller.

The matrix converter is an AC to AC power switching topologies that have installed extensive research concentration as another to conventional AC to DC to AC converter. A matrix converter is able to convert energy from an AC source (Alternating) to an AC load without the necessity of an enormous and short lifetime energy storage system [4]. Shunt interleaved electrical drive arrangements including of various parallel medium voltage back-to-back converters provide power grades of tens of MVA, lesser current distortions, and an accurate smooth air gap torque. To chance unrelenting reliability and approachability goals despite the heavy parts count, the modularity of the drive arrangement essentials to be employed and a meet fault approach design that permits the exclusion and separation of faulted threads is compulsory [5, 6]. The control of four quadrant converters of electric traction vehicles agreed by an AC railway grid has to chance specific conditional limitations with concern to harmonics content and strength. The operation is increased by constantly changing the location dependent grid impedance and voltage harmonics contents earlier limited in the grid voltage. Fault tolerance capacity of the hexagram inverter motor drive modes, due to its single interconnecting nature, the hexagram inverter can permit single leg failure stripped of balancing the power circuit topologies [7, 8]. The trinary DC Source multicarrier based PWM technology is applied to create a nine-level ac output voltage with several PWM scheme. In [9], Phase shift pulse width modulation system is favored as the excellent modulation scheme for a 20MW voltage source converter HVDC with a concern of the total harmonic distortion of the system output voltage. In [10], the study of the switching status of an individual unit division of a cascaded multilevel inverter detects that the operating state of the switching of a chopper arm makes avoidable switching beneath the existing USPWM. Single phase 5level inverter designed by two separate PWM switching schemes and this predicted PWM

switching is planned based on the least switching power loss and smallest harmonic distortion [11].

2. PROPOSED TRINARY DC SOURCE MULTILEVEL INVERTER.

The suggested three-phase trinary DC source cascaded asymmetrical multilevel inverter consists of three single phases multilevel inverter. Every single-phase unit carries two full bridges with irregular DC source. The first full bridge operates the input DC source of 1Vdc and the second full bridge operates the input DC source 3Vdc as exhibited in Fig. 1. Every input DC source is connected in series to construct a suggested three-phase MLI. Every inverter generates a three different (unequal) output voltage levels, such as positive (+Ve), zero (0) and negative (-Ve) levels by separate groupings of the four power semiconductor switches S1, S2, S3, and S4. Whenever switches, S1 and S4 is switched ON, then the inverter output voltage is positive level (+Ve); whenever the switches S2 and S3 is switched ON, then the inverter output voltage is negative level (-Ve); whenever either pair of switches (S1 and S2) or (S3 and S4) is switched ON, then the output voltage will be at zero levels (0).

Then the output voltage of the first bridge can be made equal to the −1Vdc, 0, or 1Vdc, correspondingly the output voltage of the second bridge can be made similar to the −3Vdc, 0, or 3Vdc by switching ON and switching OFF its power semiconductor switches suitably. Consequently, the output voltage of the inverter values for −4Vdc, −3Vdc, −2Vdc, −1Vdc, 0, 4Vdc, 3Vdc, 2Vdc, 1Vdc, can be produced. Table 1 describes the switching sequence of a suggested multilevel inverter.

The lower inverter (HB2) provides a fundamental output voltage with three levels, and then the upper inverter (HB1) adding or subtracting one level from the fundamental output voltage wave to create stepped waves. Here, then the final output voltage levels enhance the summing of every terminal voltage of cascaded Half Bridge, and then the output voltage of the load is given in (1).

Vout=VHB1+VHB2 (Or) *Vout=Vdc+3Vdc* (1)

The output voltage of the first bridge is registered by Vdc and the second full bridge is registered by 3Vdc. In the suggested inverter circuit topologies, if m number of cascaded H bridge section has unbalanced DC sources in order of the power of 3, an expected output voltage levels are provided as,

$Vm = 3^m$, *m=1,2,3.....* (2)

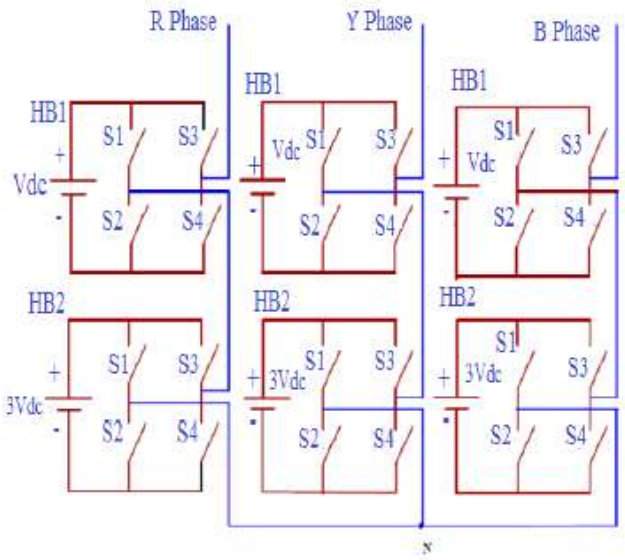


Fig. 1. Proposed trinary DC source multilevel inverter

3. OPERATION OF PROPOSED MULTILEVEL INVERTER.

The lower inverter (HB2) provides a necessary output voltage with three levels, and then the upper inverter (HB1) adding or subtracting one level from the fundamental output voltage wave to produce stepped waves. Following represents the switching sequence of three-phase nine level inverter with R Phase and other two-phase (Y and B Phase) are similar to R Phase. To produce a staircase/ stepped output voltage, the following steps should be observed.

Step 1: For an output voltage level, *Vout* =0Vdc, the power semiconductor switches S2 and S4 are tuned on at both full bridge inverter.

Step2: For an output voltage level, *Vout* = 1Vdc, the power semiconductor switches S1 and S4 are turned on at upper full bridge, S2 and S4 are turned on at lower full bridge inverter.

Step 3: For an output voltage level, *Vout* = 2Vdc, the power semiconductors switches S2 and S3 are turned on at upper full bridge, S1 and S4 are turned on at lower full bridge inverter.

Step 4: For an output voltage level *Vout*=3Vdc, the power semiconductor switches S2 and S4 are turned on at upper full bridge, S1 and S4 are turned on at lower full bridge inverter.

Step 5: For an output voltage level *Vout*= 4Vdc, the power semiconductor switches S1 and S4 are turned on at upper full bridge, S1 and S4 are turned on at lower full bridge inverter.

Step 6: For an output voltage level *Vout* = -1Vdc, the power semiconductor switches S2 and S3 are turned on at upper

full bridge, S2 and S4 are turned on at lower full bridge inverter.

Step 7: For an output voltage level *Vout*= -2 Vdc, the power semiconductor switches S1 and S4 are turned on at upper full bridge, S2 and S3 are turned on at lower full bridge inverter.

Step 8: For an output voltage level *Vout*= -3Vdc, the power semiconductor switches S2 and S4 are turned on at upper full bridge,S2 and S3 are turned on at lower full bridge inverter.

Step 9: For an output voltage level *Vout* = -4Vdc, the power semiconductor switches S2 and S3 are turned on at upper full bridge, S2 and S3 are turned on at lower full bridge inverter.

4. ADVANCED PULSE WIDTH MODULATION TECHNIQUE.

The sinusoidal PWM technique is most widely used PWM technique but it has the drawback of producing the low fundamental RMS output voltage. Due to overcome the drawback, advanced pulse width modulation has been developed. In this work, advanced PWM with multicarrier arrangement is used for generating the triggering pulse for proposed trinary sequence based CHBMLI. For an 'm' level inverters in bipolar multi-carrier techniques, 'm-1' carriers with same frequency fc and same peak to peak amplitude Ac are required [12, 13]. The reference waveform has amplitude of Am and frequency of fm and it is placed at the both cycles. The reference wave is continuously compared with each triangular carrier signals. Whenever the reference wave is greater than carrier signals leads to activate a device corresponding to those carriers otherwise the semiconductor device is switched off. There are many advanced pulse width modulation control techniques has discussed in literature. In this paper, Trapezoidal PWM is discussed which is one of the techniques of it.

The triggering signals are generated by comparing a triangular wave carrier signals with a modulating trapezoidal reference wave. This type of modulation techniques increases the peak fundamental RMS output voltage. The trapezoidal reference wave signal can be achieved from a triangular wave carrier signal by restrictive its magnitude to A_m which is interrelated to the peak value of $A_{r(max)}$ is given by

$$A_r = \alpha\, A_{r(max)} \tag{3}$$

Where α is called as the triangular wave factor.

Because the waveform becomes a triangular wave signal when α=1.Then the modulation indices Ma is given by

$$M_a = \frac{A}{A_c} = \frac{\alpha A_{r(max)}}{A_c} \tag{4}$$

The angle of the flat portion the trapezoidal reference wave is given by

$$2\phi = (1-\alpha)\pi \tag{5}$$

For stable values of $A_{r(max)}$ and A_c, the magnitude and level of output voltage changes with respect to the modulation index. *H*ere, $A_{r(max)}$ is called as peak amplitude value of trapezoidal reference wave. A_c is called as peak amplitude of carrier triangular signals. Here, trapezoidal wave signal is used as a reference signal and triangular wave is used as carrier signal. There are many control techniques are possible, some of those techniques are discussed in this paper which is given below:

4.1. Phase disposition pulse width modulation technique (PD).

4.2. Phase opposition disposition pulse width modulation system (POD).

4.3 Alternate phase opposition disposition pulse width modulation system (APOD).

4.4 Carrier overlapping pulse width modulation system (COP).

4.5 Variable frequency pulse width modulation system (VF).

The formula of Amplitude modulation indices (M_a) for phase disposition PWM, Phase Opposition Disposition PWM, Alternate Phase Opposition Disposition PWM and Variable Frequency PWM is given below

$$M_a = \frac{4A_m}{(m-1)\,A_c} \tag{6}$$

For the carrier overlapping PWM

$$M_a = \frac{A_m}{(2.5)^*\,A_c} \tag{7}$$

Here, A_m- Amplitude of a Modulating signal (Reference Signal), A_c -Amplitude of a carrier signal, m – output level, M_a - Modulation index.

4.1 In Phase Disposition Pulse Width Modulation Technique

For an m-level inverter, (m-1) carriers with the same carrier frequency of (f_c) and the same amplitude of carrier signal is (A_c) are required.

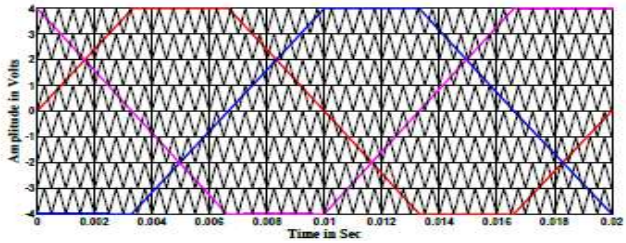


Fig..2. (a) Triangular Carrier and Trapezoidal reference wave arrangement: PD PWM system;

In phase disposition pulse width modulation technique (PD), all carriers are in phase with each other and it has same amplitude. The carrier wave arrangement of three-phase multilevel inverter with trapezoidal reference is shown in Fig. 2(a).

4.2Phase Opposition Disposition Pulse Width Modulation Technique

For an m-level inverter, (m-1) carriers with the same carrier frequency of (fc) and the same amplitude of carrier signal is (Ac) are required. Phase opposition disposition pulse width modulation technique (POD), all carriers are in phase with above and below the modulating signals in zero values. These carriers which below the zero values are 180 degrees out of phase width. The carriers' wave arrangement of three-phase multilevel inverter with trapezoidal reference is shown in Fig. 2 (b).

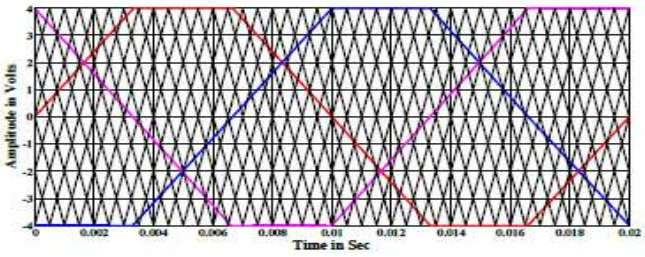


Fig..2. (b) Triangular Carrier and Trapezoidal reference wave arrangement: POD PWM System;

4.3 Alternate Phase Opposition Disposition Pulse Width Modulation Technique

For an m-level inverter, (m-1) carriers with the same carrier frequency of (f_c) and the same amplitude of carrier signal is (A_c) are required. Alternate phase opposition disposition pulse width modulation technique (APOD), the carriers are 180 degree phase displaced with its neighbor carrier. The carrier wave arrangement of a three phase multilevel inverter with trapezoidal references is shown in Fig. 2 (c).

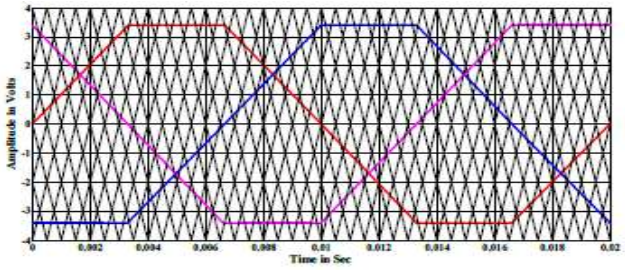


Fig..2. (c) Triangular Carrier and Trapezoidal reference wave arrangement: APOD PWM system;

4.4 Carrier Overlapping Pulse Width Modulation Technique

All carriers have the same frequency fc and same amplitude Ac is disposed such that their bands occupy overlapping with each other carriers. The overlapping vertical distances between each carrier are Ac/2 which is shown in Fig. 2 (d).Amplitude of the reference waveform is A0 and frequency is f0 and it is centered in the middle of the carrier signals.

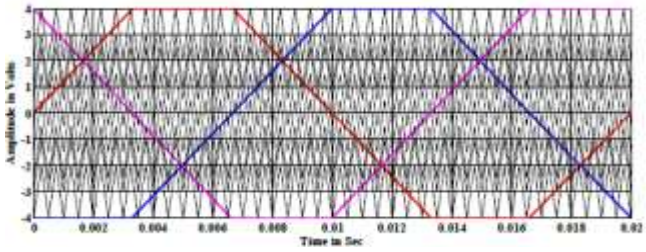


Fig..2. (d) Triangular Carrier and Trapezoidal reference wave arrangement: Carrier arrangement of VF PWM System;

5. SIMULATION RESULTS AND DISCUSSION.

A trinary DC source cascaded asymmetrical three phase multilevel level inverter for generating the nine level output voltage is modeled in MATLABSIMULINK using power systems block set. The proposed multilevel inverter simulation circuit is shown in Fig. 3. Simulations result of %THD is carried out for different values of ma ranges from 0.8 to 1using the FFT plot. Table 1 shows the values of %THD for R and RL load in different carrier arrangement. Table 2 shows the fundamental RMS output voltage of Vrms of proposed MLI in both R and RL load for various carrier arrangements during the modulation indices range of 0.8 to 1.

5.1 R Load

Fig. 4 represents the output voltage created by carrier based PWM control with trapezoidal reference for R Load. For a modulation indices (ma=0.85), it is observed from the Fig. {5 (a), 5(b), 5(c), 5 (d) and 5(e)} the harmonic energy level is governing in: Fig. 5(a) characterizes the harmonic energy

level in PD PWM techniques shows 5thth, 20th, and 40th order of harmonic. Fig. 5(b) characterizes the harmonic energy level in POD PWM techniques shows 5th, 19th, 20th, 29th, 31st and 40th order of harmonic. Fig. 5(c) represents the harmonic energy level in APOD PWM techniques shows 5th, 7th, 29th, 31st, 35th, 37th and 39th order of harmonic. Fig. 5(d) characterizes the harmonic energy level in COP PWM techniques shows 5th and 40th order of harmonic.

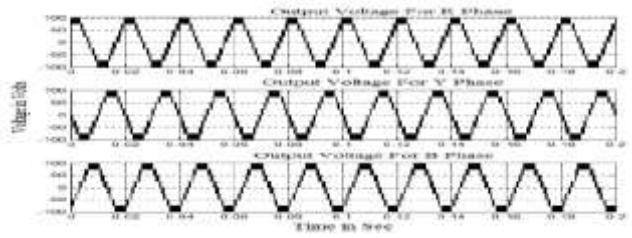


Fig. 4. Output voltages created by All Carrier based PWM control with Trapezoidal reference for R load.

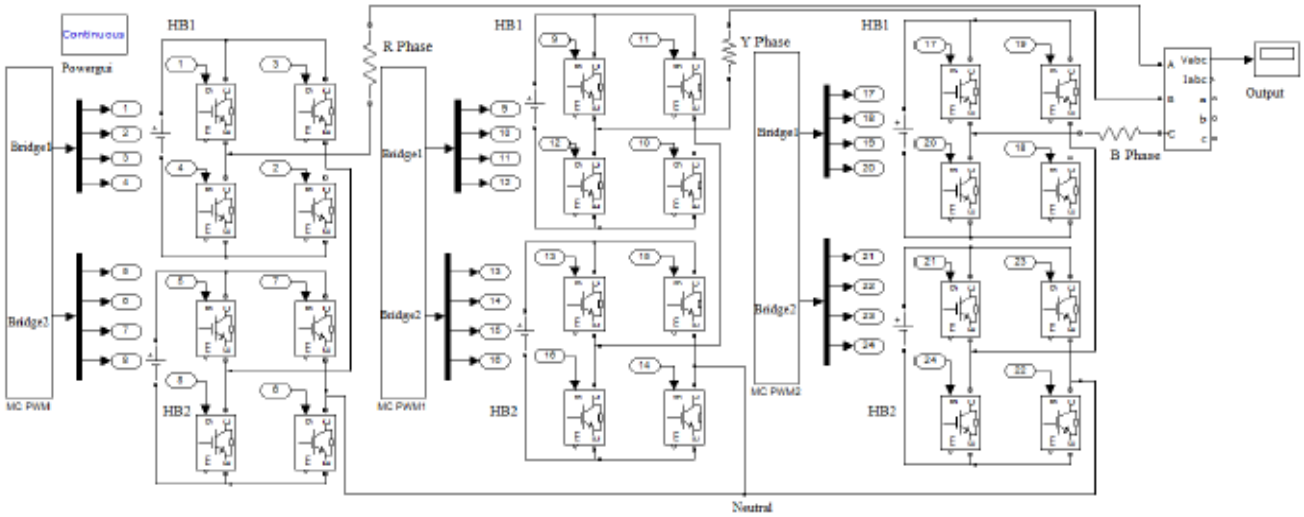
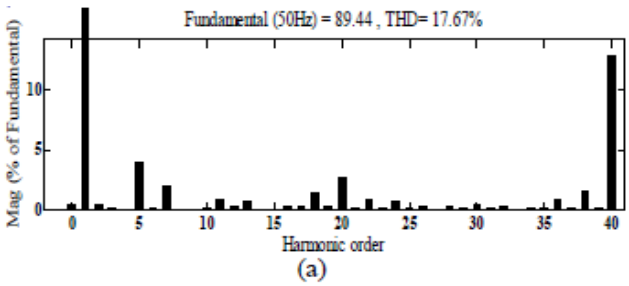
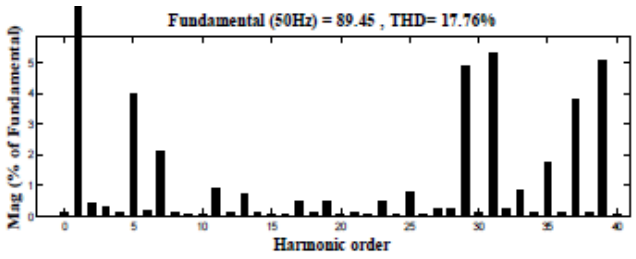
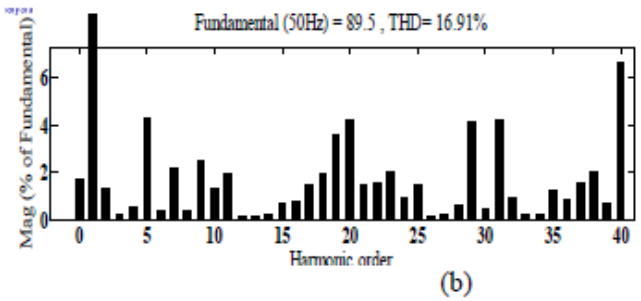


Fig. 3. Simulink model of Trinary DC source asymmetrical three phase cascaded multilevel inverter







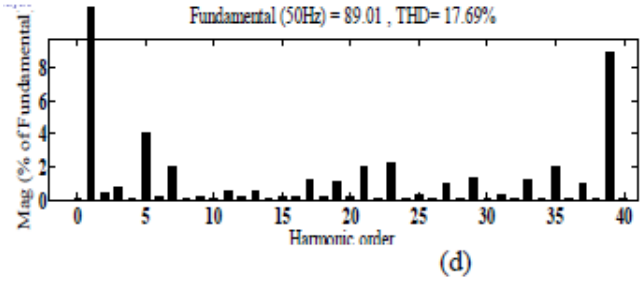


Fig. 5. FFT plot for output voltage of PWM control with Trapezoidal reference with R Load: (a) PD PWM system; (b) POD PWM system; (c) APOD PWM system; (d) COP PWM System;

5.2 RL Load

Fig. 6 represents the output voltage created by carrier based PWM control with trapezoidal reference for RL Load. For a modulation indices (ma=0.85), it is observed from the Fig. 7(a), 7(b), 7(c), and 7(d)} the harmonic energy level is governing in: Fig. 7(a) characterizes the harmonic energy level in PD PWM techniques shows 5thth and 39thorder of harmonic. Fig. 7(b) characterizes the harmonic energy level in POD PWM techniques shows 5th, 20thand 40th order of harmonic. Fig. 7(c) represents the harmonic energy level in APOD PWM techniques shows 5th, 7th, 29th, 31st, 35th, 37th and 39th order of harmonic. Fig. 7(c) characterizes the harmonic energy level in COP PWM techniques shows 5th and 40th order of harmonic. Fig. 7(d) characterizes the harmonic energy level in VF PWM techniques shows 5th, 11th, 19th, 27th, 29th, 39th and 40th order of harmonics.

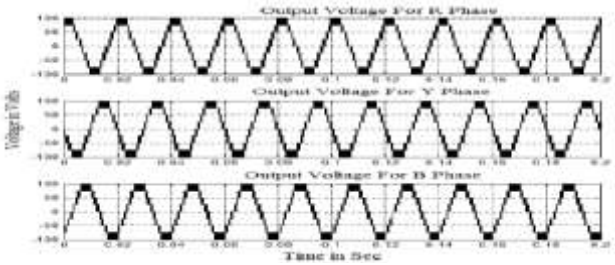
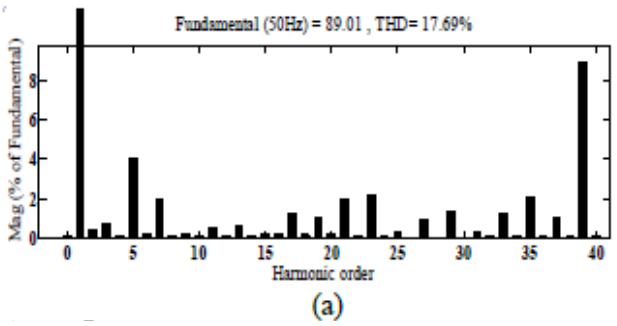


Fig. 6. Output voltages created by All Carrier based PWM control with Trapezoidal reference for RL Load



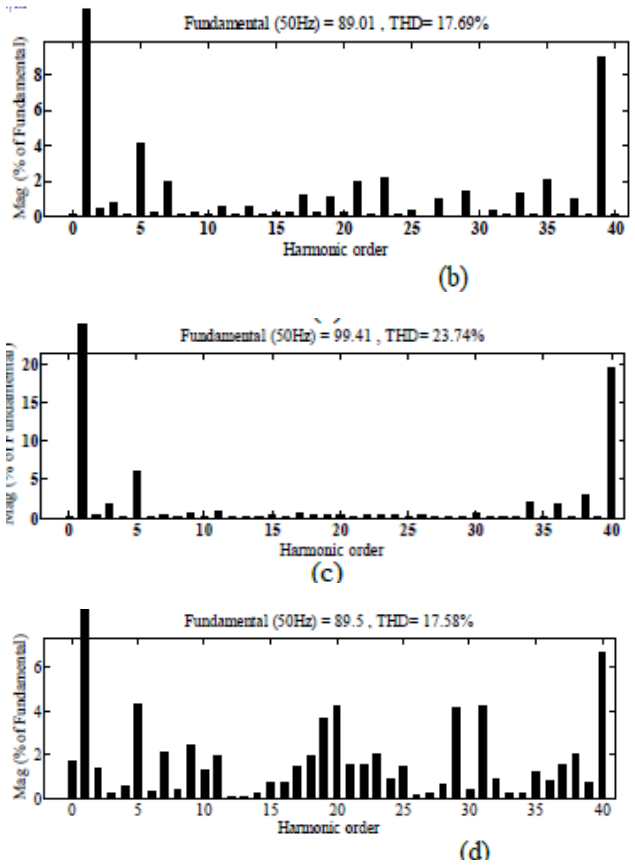


Fig. 7. FFT plot for output voltage of PWM control with Trapezoidal reference with RL Load :(i) IPD PWM system; (ii) POD PWM system; (iii) COP PWM System; (iv) APOD PWM system; (v) VF PWM System.

Table 1and represent the THD contrast of IPD, POD, APOD, COP and VF pulse width modulation techniques with R and RL load no more than one pulse modulation techniques such as POD in R load (Phase Opposition Disposition) it hold minimum quantity of harmonic distortion. Table 2 represent the VRMS contrast of IPD, POD, APOD, COP and VF pulse width modulation techniques with R and RL load no more than one pulse modulation techniques such as COP in R load (Carrier Overlapping) it hold maximum quantity of fundamental RMS output voltage.

Table 1: % THD for Different Modulation Indices

Ma	R Load					R L Load				
	PD	POD	APOD	COP	VF	PD	POD	APOD	COP	VF
1	12.56	11.87	12.40	19.79	12.92	12.08	11.42	12.21	19.31	12.39
0.95	15.25	15.39	15.24	20.98	15.64	15.16	15.02	15.27	20.95	15.46
0.9	17.99	16.81	17.04	22.43	17.01	17.02	16.12	19.78	22.79	17.16

0.85	17.67	16.91	17.76	23.74	17.69	17.69	16.13	17.77	23.74	17.58
0.8	17.48	17.23	17.53	25.31	17.11	17.45	17.03	17.48	25.31	17.19

Table2: Fundamental RMS Voltage for Different Modulation Indices

Ma	R Load					R L Load				
	PD	POD	APOD	COP	VF	PD	POD	APOD	COP	VF
1	74.34	74.29	74.49	77.55	74.51	74.33	70.29	74.34	77.47	74.49
0.95	70.68	70.18	70.65	75.21	70.51	70.67	70.79	70.62	75.13	70.09
0.9	66.97	67.11	66.95	72.08	67.18	66.94	67.05	66.96	72.01	67.18
0.85	63.25	62.94	63.25	70.29	63.29	63.22	62.89	63.26	70.20	67.18
0.8	59.45	59.41	59.53	67.61	59.49	59.49	59.44	59.55	67.01	59.41

6. CONCLUSION

A trinary based asymmetric three phases cascaded H Bridge multilevel inverter with R and RL load has been presented in this paper. It is mentioned that the phase opposition disposition PWM system (RL Load) with trapezoidal reference delivers excellent output waveform with comparatively low total harmonic distortion and carrier overlapping PWM system (RLoad) with trapezoidal reference delivers comparatively greater fundamental RMS output voltage (VRMS). The execution parameters like Total Harmonic Distortion (THD) and Fundamental RMS output voltage (VRMS) are determined and tabulated. The simulation circuit is performed to show the strong point of the suggested new asymmetrical three phase multilevel inverter with trinary DC source cascaded H Bridge. This topology could be analyzed with renewable energy sources like photovoltaic panel or wind energy in future. Also, it could be tested with other pulse width modulation techniques like space vector pulse width modulation or soft computing algorithms.

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