International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395-0056
Volume: 06 Issue: 12 | Dec 2019 www.irjet.net p-ISSN: 2395-0072

IMPLEMENTATION OF LOW POWER FLASH ADC USING ADIABATIC LOGIC BASED DOUBLE TAIL COMPARATOR

Bandreddi Naga Lakshmi[1], Dr. P. Rajesh Kumar[2]

[1]*M.Tech Scholar, Department of Electronics &Communication, Andhra University, A.P, INDIA*
[2]Professor, *Department of Electronics &Communication, Andhra University, A.P, INDIA*

Abstract - *Analog to digital converter has become a very important device in today's digitized world as they have very wide range of applications. Among all the ADC's flash ADC is the fastest one but the main drawback is its power consumption. The performance of Flash ADC is affected due to comparator and encoder design. The dynamic double tail comparator is designed by adding some transistors for low power and fast operation even the circuit operates in low supply voltages. The adiabatic logic is applied to the double tail comparator to reduce the power consumption. The encoder is designed by using fat tree logic. The Flash ADC is designed by combining the resistor ladder network, adiabatic logic based double tail comparator and fat tree encoder. The circuit operates with supply voltage 1.2V. All the circuits are simulated using DSCH and LT SPICE software. The layouts are drawn by using MICROWIND software.*

Key Words: Flash ADC, Comparator, Fat tree encoder, Adiabatic logic, SAR ADC,

1. INTRODUCTION

The development in the digital signal processor field is rapid due to the advancement in the integrated circuit technology over the last decade. Moreover, advantage of digital signal processing is that it is more immune to noise. So analog to digital converter plays an interface role in between analog signal and digital signal processing system. DC which is being designed these days needs an architecture having high speed of operation and less power consumption. One single ADC type cannot cover all applications since the performance parameters like sampling rate, power consumption and resolution of an ADC is basically determined by its architecture.

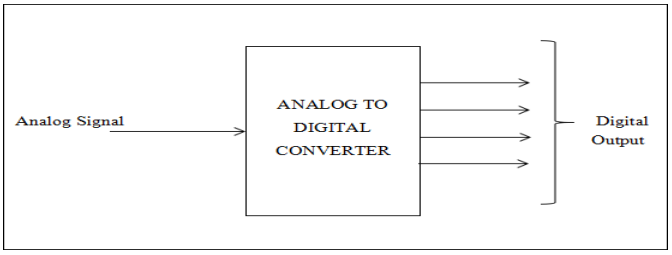

Fig -1: Block Diagram of ADC

Analog to digital converters (ADC's) are the most distinguished signal circuits which interface the world analog signals, the digital signal processing and computing world. ADC's includes three essential parameters which cannot be changed once it has been designed and the parameters are resolution, speed and power consumption. Based up on different applications a variety ADC's with different architectures, resolutions, sampling rates, power consumptions, and temperature ranges have been designed. Since the performance sampling rate, resolution, and power consumption of an ADC is basically determined by its architecture, one single ADC type cannot cover all applications. For instance, Flash (parallel) ADC's can be used in high speed and low resolution applications. Because of its parallel architecture, all conversions are done in one cycle with many comparators.

2. Flash ADC

The flash ADC is mainly consists of three blocks. The three blocks resistor ladder block, comparator and encoder are integrated together to get the functionality of Flash ADC.

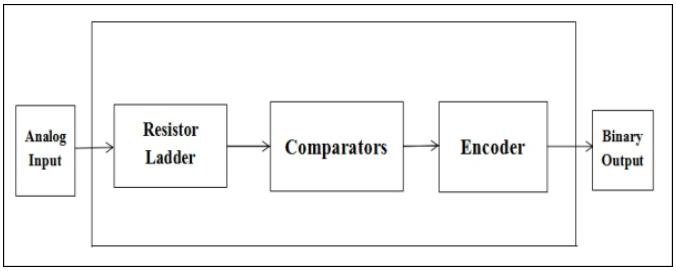

Fig -2: Block Diagram of Flash Adc

3. RESISTOR LADDER NETWORK

The resistor ladder is designed mainly to provide a stable reference voltage to the comparators. The resistor ladder network is formed by 2^N resistors which generates the reference voltage. The reference voltage for all comparator is one least significant bit (LSB) less than the reference voltage for the comparator immediately above it. The ladder divides main reference voltage into 2^N equally spaced voltages.

4. COMPARATOR

The comparator compares the input signal with the reference voltage which is generated by the resistor ladder block. Comparator is the device that compares two analog

voltages or currents and switches it output to indicate which one is larger.

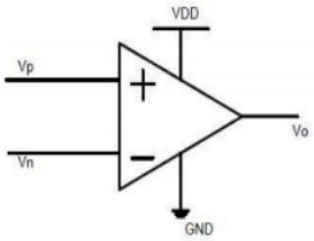

Fig -3: Schematic Diagram of Comparator

If Vp is at a greater potential than Vn, then the output Vo of the comparator is logic 1 and when Vp is at a potential less than Vn, then the output is at logic 0. If we apply a pulse voltage at VP and a DC reference voltage at Vn, the output is logic 1 when the pulse amplitude is greater than the reference voltage.

4.1 SINGLE TAIL COMPARATOR

The operation of Conventional Dynamic Comparator is given in two phases. First one is reset Phase and second one is comparison Phase.

Reset Phase: When clk=0, Mtail transistor goes off and transistors M7-M8 (Reset transistors) goes on which drives both output nodes outp and outn to Vdd. During reset, this defines a start condition with valid logical level.

Comparison Phase: This is the second phase where comparison takes place. When clk=VDD, Mtail goes ON and transistors M7-M8 goes OFF. The output nodes that had already been pre-charged to VDD start to discharge with the different rates of discharging, depending upon two input voltages Vinp and Vinn. Let us assume the case where Vinn>Vinp.

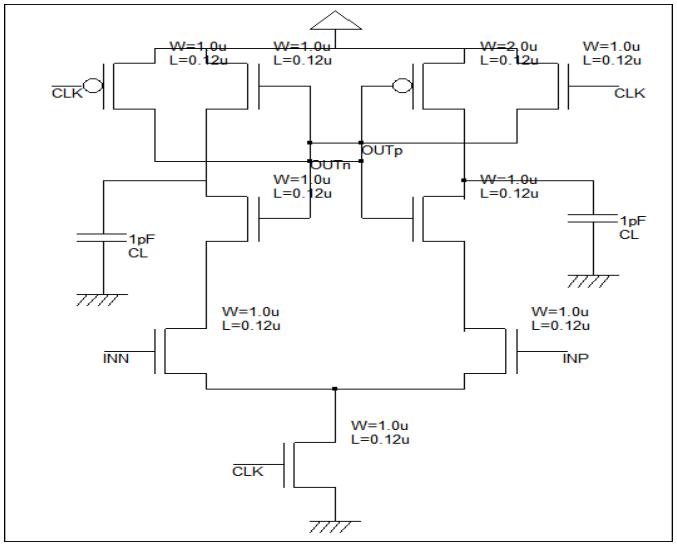

Fig -4: Single Tail Comparator

Due to this voltage difference output node Outn (discharge due to drain current of transistor M1) starts to discharge with faster rate than Outp, falls down to Vdd-[Vthn] before Outp (which is discharges due to drain current of transistor M2), the corresponding Pmos (M6) goes On to initiate latch regeneration which is caused due to cross coupled (back to back) inverters i.e. M3, M5 and M4, M6 transistors. Hence Outp charges to VDD while Outn discharges to ground. Considering another case, if Vinp>Vinn, the whole circuit works vice versa.

4.1 CONVENTIONAL DOUBLE TAIL COMPARATOR

The difference between conventional dynamic comparator and conventional double tail comparator is that the double tail comparator can operate in very low supply voltages when compared to conventional dynamic comparator. Operation of conventional double tail comparator is also divided into two phases as reset phase and comparison phase.

Reset Phase: For reset phase clk=0 hence mtail1 and mtail2 goes off, avoiding static power consumption. Both the nodes fn, fp pulled to Vdd by transistors M3 and M4, hence Mc1 and Mc2 went to cutoff. MR1 and MR2 are the intermediate stage transistors, grounds the both latch output.

Comparison Phase: In comparison phase, clk=VDD hence Mtail1 and Mtail2 are on and transistors M3 and M4 goes off. At the beginning, as both the nodes fp and fn are about VDD hence the control transistors are still OFF. So, in accordance with input voltages applied, both the nodes fp and fn start to fall. Consider the case, if Vinp>Vinn, due to this voltage difference fn starts to drop with a faster rate than fp this happens because M2 transistor drives more current than M1 transistor. Now, during the drop of node fn, corresponding transistor Mc1(control transistor) of pmos gets start to turn ON which pulls fp node again to VDD while other control transistor MC2 remains in off state for allowing node fn to discharge completely. While considering the other case i.e. if Vinn>Vinp, the whole circuit works vice versa.

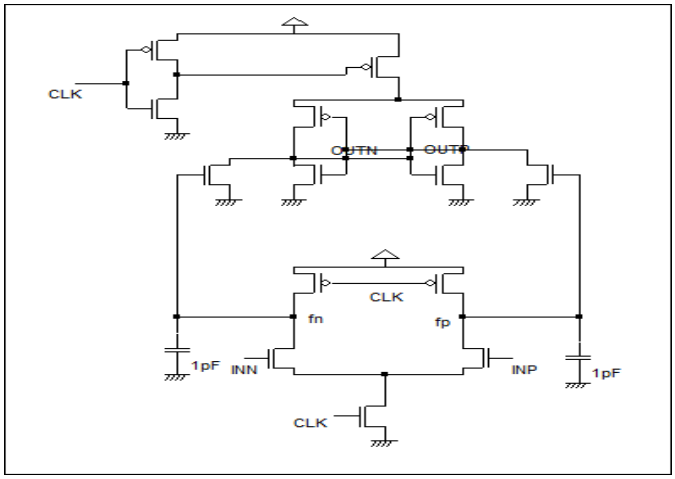

Fig -5: Conventional Double Tail Comparator

4.3 DYNAMIC DOUBLE TAIL COMPARATOR

The basic idea of this comparator is to increase the latch regeneration speed. For this purpose, the two control transistors Mc1 and Mc2 are added to the first stage with are in parallel with M3 and M4 but in cross coupled manner as shown in the figure above. The operation of this comparator is also divided into two phases which are reset and comparison (decision making) phase.

Reset Phase: During this phase, clk=0 so Mtail1 and Mtail2 are Off, both the nodes fp and fn are driven to Vdd by transistors M3 and M4.Hence two control transistors Mc1 and Mc2 are cut off. Both the latch outputs are reset to ground by the intermediate stage transistors MR1 and MR2. **Comparison Phase:** In this phase, clk=Vdd, hence Mtail1 and Mtail2 are On, transistors M3 and M4 are in Off state. At the beginning of this decision making phase, as both the nodes fp and fn are about Vdd so both the control transistors Mc1 and Mc2 are still in Off state. Now both the input nodes fp and fn starts to fall down with different discharging rates in accordance with the input voltages applied. Considering the case, if Vinp>Vinn. Due to this voltage different, node fn starts to drop with faster rate than node fp because current provided by M2 is greater than M1.

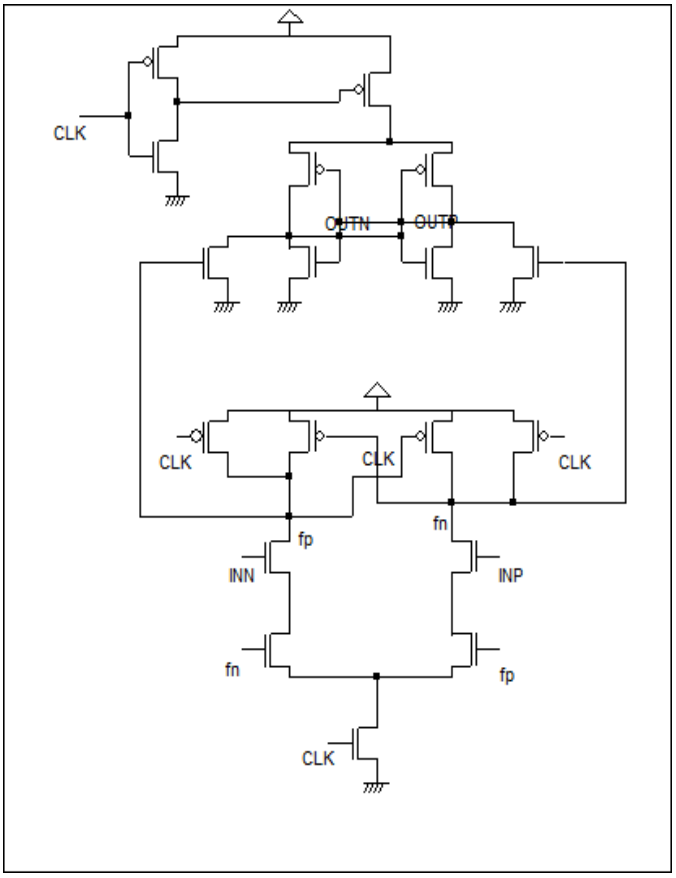

Fig -6: Dynamic Double Tail Comparator

4.4 ADIABATIC LOGIC BASED DOUBLE TAIL COMPARATOR

4.4.1 ADIABATIC LOGIC: Adiabatic logic circuit is a low power circuit which use "reversible logic" to conserve the energy. Adiabatic logic works with the concept of switching activities which results in reduction of the power by giving stored energy back to the supply. There are two key rules associated with it:

1. Never turn on a transistor when there is a voltage potential between the source and drain.

2. Never turn off a transistor when current is flowing through it.

In the principle of operation of adiabatic logic circuit, the power clk plays an important role in the main design. When clk=1 (charge),

When clk=0 (discharge),

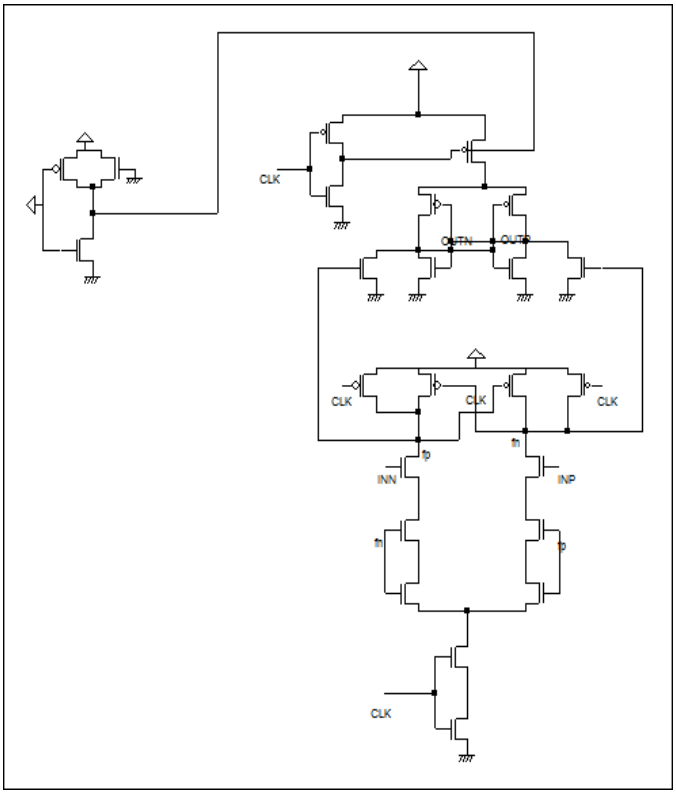

Fig -7 : Adiabatic Logic Based Double Tail Comparator

In this condition the power get reduce in great extent and also improves the speed of the circuit operates on high speed. It is very important to use adiabatic logic circuit as an extra circuitry for the optimization of power in double tail comparator circuit. It is an essential factor for power consumption performance. At the starting condition adiabatic logic is applied to power supply. At the time one transistor is on another one is off and vice versa. It provides the continuous supply to the circuit. This means that at

working period it goes into charging condition and at off stage the circuit discharges according to the supply.

Working of modified dynamic double tail comparator in both reset and comparison phase is similar as the double tail comparator. At the beginning of the decision making phase, both fn and fp nodes are pre charged to VDD. In the reset phase switches are closed fn and fp starts to drop with different discharging rates depends on the input voltages. As soon as comparator detects that one of the fn or fp nodes discharging faster, one of the control transistor will act in a way to increase their voltage difference. If fp is at VDD then fn should be discharged completely, hence switch in the charging path of fp will be opened but the other switch connected to fn will be closed which allow the complete discharge of fn node. The operation of the control transistors with the switches emulates the operation of the latch.

Table -1: Comparision of Power Consumption of Different Comparators.

Design	Power Consumption	Area
Single Tail Comparator	6.683mW	100µm X18µm
Conventional Double Tail Comparator	0.118mW	119µm X18µm
Dynamic Double Tail Comparator	0.108mW	44µm X9µm
Adiabatic Logic Based Dynamic Double Tail Comparator	76.908µW	48µm X13µm

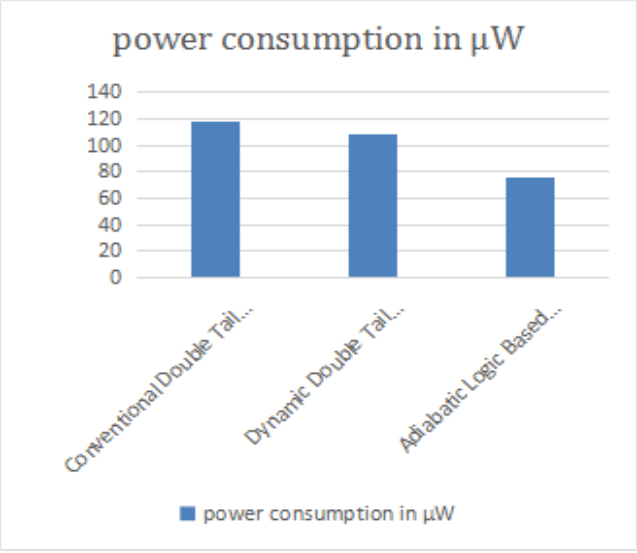

Chart -1 : Comparision Of Different Types Of Comparators

5. ENCODER DESIGN

The encoder is mainly used to convert thermometer code to binary output. There are different ways with which the implementation of thermometer code to binary code conversion can be done. It includes ROM encoder, fat tree encoder, Wallace tree encoder, multiplexer based encoder and logic style based encoder.

Table -2: Truth Table For Encoder

Thermometer Code	B3	B2	B1	B0
000000000000000	0	0	0	0
000000000000001	0	0	0	1
000000000000011	0	0	1	0
000000000000111	0	0	1	1
000000000001111	0	1	0	0
000000000011111	0	1	0	1
000000000111111	0	1	1	0
000000001111111	0	1	1	1
000000011111111	1	0	0	0
000000111111111	1	0	0	1
000001111111111	1	0	1	0
000011111111111	1	0	1	1
000111111111111	1	1	0	0
001111111111111	1	1	0	1
011111111111111	1	1	1	0
111111111111111	1	1	1	1

Fat tree encoder is the popular architecture that is being used in many flash ADC designs. This type of encoder requires intermediate conversion which converts the thermometer code to one out of N code. The one out of N code is then encoded to binary using fat tree encoder, which consists of multiple branches of OR gates. As the number of input bits increases, tree becomes larger. To improve the performance of fat tree encoder, the OR gates are replaced with NAND and NOR logic gates using De-Morgan's theorem.

The flash ADC is mainly consists of three blocks. The three blocks resistor ladder block, comparator and encoder are integrated together to get the functionality of Flash ADC. Flash or parallel converters have the highest speed of any type of ADC's. As seen in fig they use one comparator per quantization level (2^N-1) and 2^N resistors. The reference voltage is divided into 2^N values, each of which is fed into a comparator. The input voltage is compared with the each reference value and generates the thermometer code at the output of the comparators. A thermometer code generates all zeros for each resistor level if the value of the v_{in} less than the value on the resistor string, and ones if the value of v_{in} greater than or equal to the value on the resistor string.

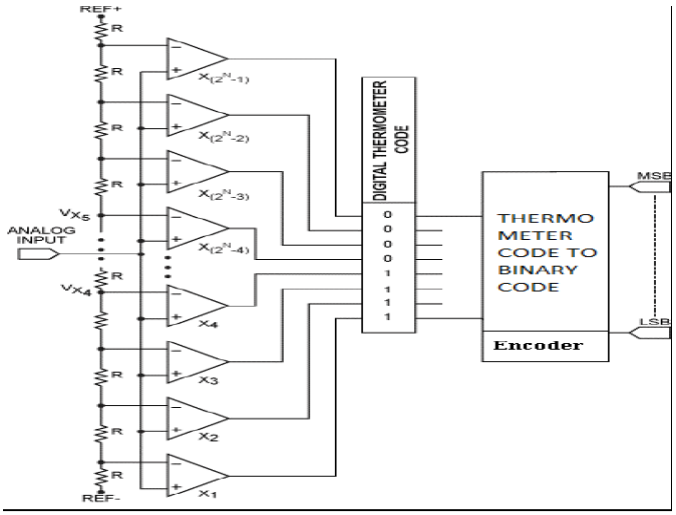

Fig -8: Flash ADC Using Adiabatic Logic Based Double Tail Comparator

6. SIMULATION RESULTS

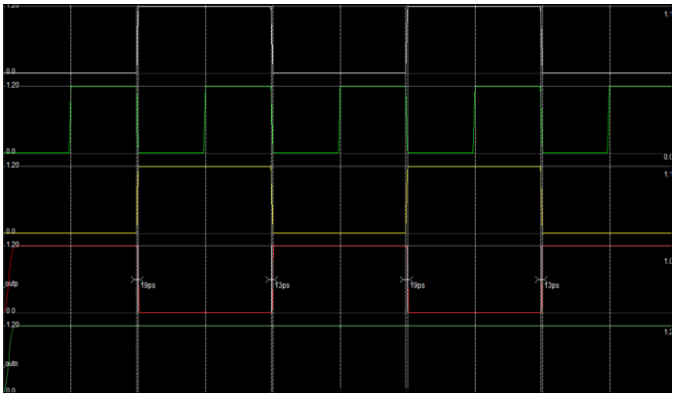

Fig -9: Simulation Results of Single Tail Comparator.

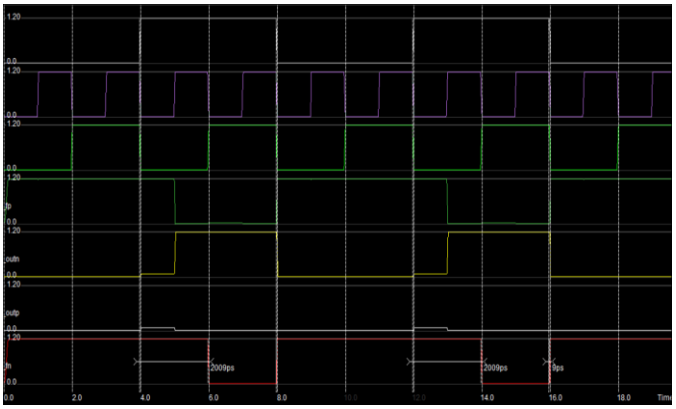

Fig -10: Simulation Results of Conventional Double Tail Comparator.

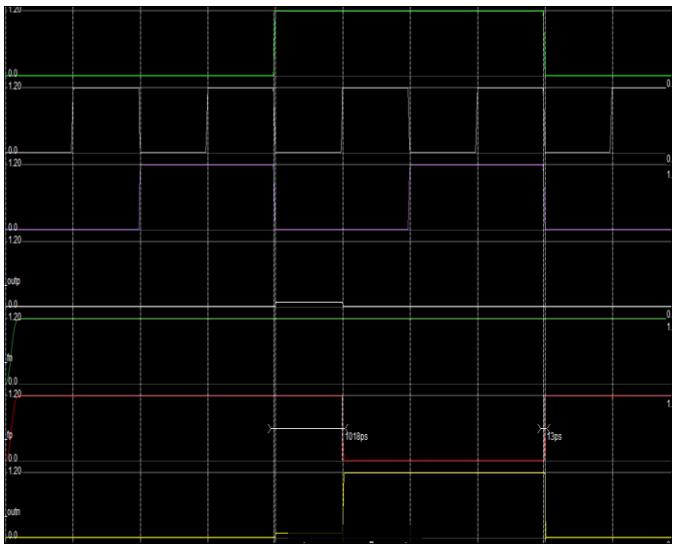

Fig -11: Simulation Result of Dynamic Double Tail Comparator.

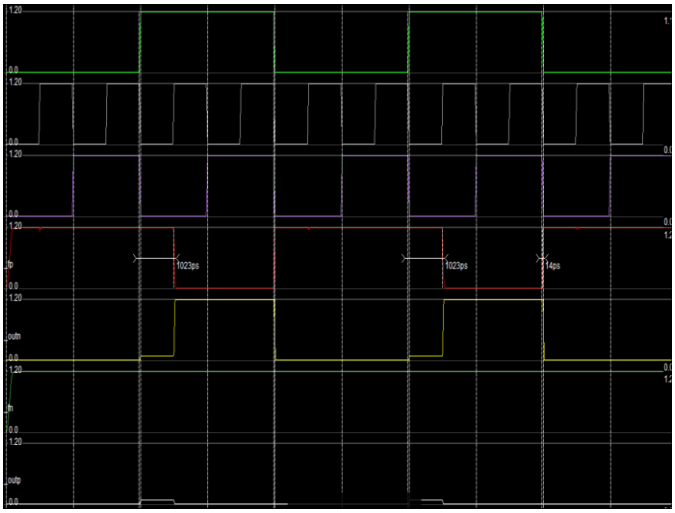

Fig -12: Simulation Result of Adiabatic Logic Based Double Tail Comparator

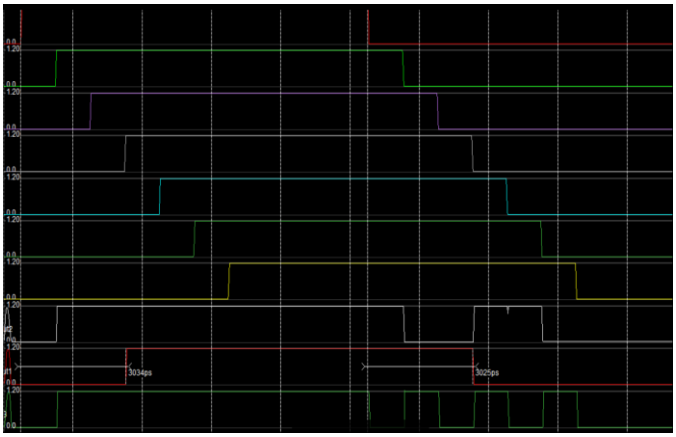

Fig -13: Simulation Result of Adiabatic Logic Based Double Tail Comparator

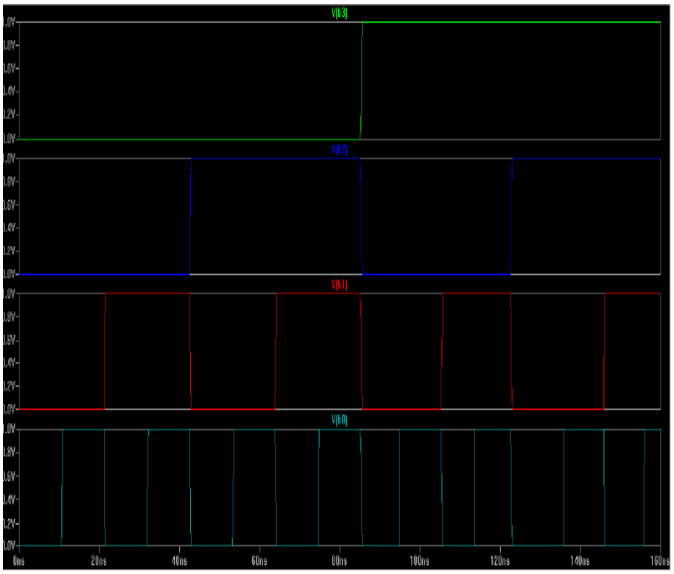

Fig -14: Simulation Result of Flash ADC Using Double Tail Comparator

7. CONCLUSION

Flash ADC is taken as the best architecture for high speed applications. The first step of this project is to design comparator. Analysis of two common structures which conventional dynamic comparator and conventional double tail comparator is done. Based on the analysis, a new structure of double tail comparator with two switches is proposed which is used for low voltage low power capability for improving the performance of the comparator. The proposed comparator has reduced power to a great extent as compared to conventional dynamic comparator and conventional double tail comparator. As compared to conventional double tail comparator and the dynamic double tail comparator, the adiabatic logic based comparator consumes 76.908µW of the power consumption. The layout had been drawn and the layout area of adiabatic logic based double tail comparator obtained is 48µmX13µm. The fat tree logic based encoder is designed with the power dissipation of 8.322µW with 1.2V supply voltage. The layout had been drawn and the layout area of fat tree logic based encoder obtained is 132µmX18µm. finally by combining resistor ladder, comparator blocks and encoder, flash bit ADC is designed and simulated. The average power consumption of designed flash ADC is 5mw the layout had been drawn and the layout area of flash ADC is 83µm X 14µm. All the designs are simulated in DSCH and the layouts are drawn on MICROWIND software.

REFERENCES

[1] S.Akash, A. Anisha, G. Jaswanth Das, "Design Of Low Power And High Speed Double Tail Comparator", International Conference On Circuit, Power And Computing Technologies, Year: 2017.

[2] Hsuan-Yu Chang And Ching-Yuan Yang, "A Reference Voltage Interpolation-Based Calibration Method For Flash ADCs", IEEE Transactions On Very Large Scale Integration (VLSI) Systems, Volume: 24, Pages:1728 - 1738,Year:2016.

[3] Aditi Kar, Moushumi Das, Bipasha Nath, Durba Sarkar, Alak Majumdar, "Comparative Analysis Of Low Power Novel Encoders For Flash ADC In 28nm Low Power Digital Cmos", IEEE Transactions On Microwave Theory And Techniques Volume: 64, Pages: 1143-1152, Year:2016.

[4] Pranati Ghoshal And Sunit Kumar Sen, "A Bit Swap Logic (BSL) Based Bubble Error Correction (BEC) Method For Flash ADC's", 2nd International Conference On Control, Instrumentation, Energy & Communication, Pages: 111 - 115,Year:2016.

[5] Gregor Tretter, Mohammad Mahdi Khafaji, David Fritsche, Corrado Carta, Frank Ellinger, "Design And Characterization Of A 3-Bit 24-GS/S Flash ADC In 28-Nm Low power Digital CMOS", IEEE Transactions On Microwave Theory And Techniques, Volume: 64, Pages: 1143 - 1152,Year:2016.

[6] R. Kasthuri Priya, "Low-Power Low-Voltage High-Speed Performance Improvement

Analysis Of Double Tail Comparator", International Journal on Applications in information and Communication Engineering, vol. 1, no. 6, pp. 5-11, June 2015.

[7] L. Venkateswarlu, MA. Wajeed, M. Basha, "Area efficient low power double tail comparator using switching transistors", International Journal of eminent Engineering Technology, vol. 2, no. 5, June. 2015.

[8] Amol Inamdar, Anubhav Sahu, Jie Ren, Sormeh Setoodeh, Raafat Mansour And Deepnarayan Gupta, "Design And Evaluation Of Flash ADC", IEEE Transactions On Applied Superconductivity,Volume:25,Article: 1400205, Year:2015.

[9] Samaneh Babayan-Mashhadi, Reza Lotfi, "Analysis And Design Of A Low-Voltage Low-Power Double-Tail Comparator", IEEE Trans. On Very Large Scale Integration (VLSI) Systems, Vol. 22, No. 2, Pp. 343-352, Feb. 2014.

[10] Umamaheswari.V.S., Rajaramya.V.G "Low Power High Performance Double Tail Comparator" International Journal Of Scientific Engineering And Technology, Volume No.3 Issue No.5, Pp : 647-650 1 May 2014.

[11] Mr. K. N. Hosur, Mr. Dariyappa, Mr. Shivanand, Mr. Vijay, Mr. Nagesha, Dr. Girish V. Attimarad, Dr. Harish."Design Of 4 Bit Flash ADC Using TMCC & NORROM Encoder In 90nm CMOS Technology", 978-1-4673-6667-0/15/$31.00©2015 IEEE.

[12] Vinayashree Hiremath, Student Member IEEE; Saiyu Ren, Member IEEE, "A Novel Ultra High Speed Reconfigurable Switching Encoder For Flash Adc", 978-1-4577-1041-4/11/$26.00 ©2011 IEEE.