International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395-0056
Volume: 06 Issue: 12 | Dec 2019 www.irjet.net p-ISSN: 2395-0072

Implementation of TPG-LFSR with Reseeding Pattern Value

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ABSTRACT:- In this paper we discuss about Reseeding LFSR based test pattern generation. Traditional testing is not a acceptable quality with the development of integrated circuits and thickness. Testing causes the designer to explore shortcomings and blunder present in created circuit which diminishes time require to test and accordingly diminishes odds of getting fizzled during activity. Reducing the test time of the test pattern generation is one of the most effected solution for the process. Reseeding L_F_S_R is one of the technique to generate test patterns. In this paper, pseudo-random test patterns are generated to test circuit exploitation R_L_F_S_R technique. It helps to scale back the take a look at pattern needed to be hold on for testing. this method is applied by exploitation principals low-power VLSI and low take a look at information volume. Reseeding will primarily be applied for B_I_S_T that targets complete fault coverage and step-down of the take a look at length information .

INTRODUCTION:

Very Large-Scale Integration created a major impact on IC technology it is mainly used to reduce size and cost but increases in complexity. Also it results the performance and cost of the circuits which became boom to the Integrated Circuits industries. Testing of circuits became difficult as the scale of integration is increasing. Normal testing approach is not sufficient with the increase in growth of devices and limited area. In this Traditional testing involves Automatic Testing Equipment becoming more non-suitable due to the growth of Integrated Circuits technology. Linear Feedback Shift Registers are commonly used as pseudo-random test pattern generators in B_I_S_T process, it is a technique that can be used to test itself which has as an effective approach for testing. For absolute checking of errors in test pattern Built-In-Self Test technique gives an optimized response some of the components of BIST are test pattern generation and circuit under test Response In this we mainly use T-P-G for generation of test pattern.

- **Reseeding LFSR :**

Linear feedback shift registers are used to generate pseudo-random test pattern in B_I_S_T schemes. Their structure is simple, they require very small area overhead and it can used for test pattern and response generation. Some of the applications of L_F_S_R are, counters, pseudo random pattern generation, pseudo random sequences resistant faults. In this we use one xor gate

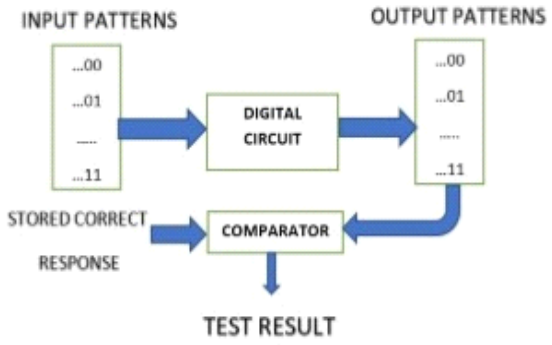

Fig1: Architecture of Test pattern

For any testing methodology, some of the factors has to be considered such as high and easy fault verifiable, speed testing, short testing time. When there is number of circuits in chip then it becomes complex. Then we have to test the chip design with increasing circuit complexity, it becomes difficult to test the chip externally. Thus we use B_I_S_T technique provides a multiple solution to above demands. Another advantage of this methodology is that the test patterns are cannot be applied by external A_T_E.

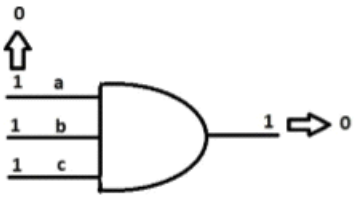

Fig2: ANDgate

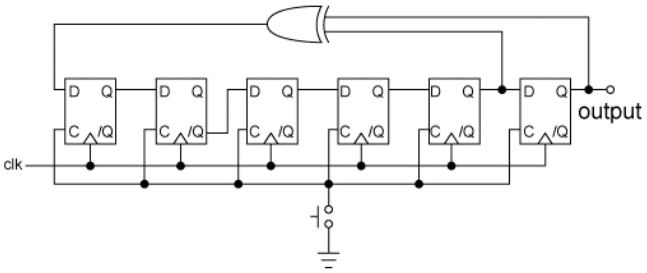

Fig3: Pseudo random pattern generation 8-bit

Maximum length of seed worth given by formula 2n-1, think about AND gate that has n input lines in fig2.The likelihood of obtaining bit one at the output of the AND gate is zero once unbiased random inputs are applied. It becomes not possible to work out the stuck at zero fault if zero applied at input face. It's inconceivable to acknowledge the stuck at zero faults gift within the circuit. So, it's troublesome to discover such form of fault from that take a look at pattern generated. Such a Fig. 3. The implemented design can able to generate the test patterns according to the seed value given to the reseeding LFSR. For N bit number the code can generate the test pattern according to the formula 2n-1. shows the given input values are accountable for the output generation result that is given to the reseeding LFSR.

L_F_S_R can accomplish high flaw inclusion by decreasing connection between the test vectors. Reseeding is an amazing technique for diminishing the test information volume and capacity, Size of the test information can be diminished by L_F_S_R clock which is inert for a few clock cycles after the information seed is given.

- **PROPOSED BLOCK DIAGARAM FOR TEST PATTERN GENERATION**

Counter is used in the system to produce the seed value. The seed value generated should be stable for 2n-1 clock cycle. In this the circuit can be worked up to 256 (8) bits. It can accept the input value up to 256bits.

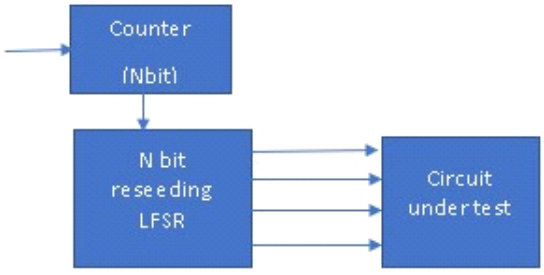

Fig-4: proposed model

Counter one price is given to the reseeding LFSR as a seed price to n bit reseeding LFSR to get Pseudo Random check Patterns for the actual seed value, During this the This check patterns won't be used for testing the CUT, since it's a lock state. LFSR is especially accustomed enhance the fault detectability and shorten the testing method. The reseeding LFSR comprises primitive polynomial which will facilitate to get all the doable combination with relevancy seed price. The seed price that is given to LFSR is taken from the counter one. in line with the given seed price check patterns area unit generated. The received check patterns area unit given to Circuit beneath check for testing the planning. Counter is employed within the system to supply the seed value.

The seed worth generated ought to be stable for 2n-1 clock cycle. within the projected system the circuit will exercise to bits [8]. The system will settle for the input worth up to 256 bits. This take a look at patterns won't be used for testing the CUT, since it's a lock state. The reseeding LFSR include primitive polynomial which will facilitate to get all the attainable combination with reference to seed worth. The seed worth that is given to LFSR is taken from the counter one. consistent with the given seed worth take a look at patterns are generated. That take a look at patterns are given to chop for testing the planning.

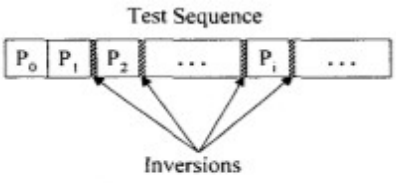

Figure 4. Test sequence

- **Experimental result :**

From the implementation of Reseeding LFSR Test pattern generation we can reduce fault circuit occurrence, increase the efficiency by using this method. In this BIST technique we use TPG by following operation we can generate the result as schematic form.

Fig-5: combinational circuit output

We use counters in this technique, it is used to count the number of cycles to perform the task, In R-LFSR we use one XOR gate to give the inputs and in normal LFSR we use number of XOR gates, in order to reduce complexity we introduce RLFSR technique. We perform write (wr), read (rd) operations and inputs are given, according to inputs, wave forms will change and there is occurrence of shifting operation with one clock pulse delay.

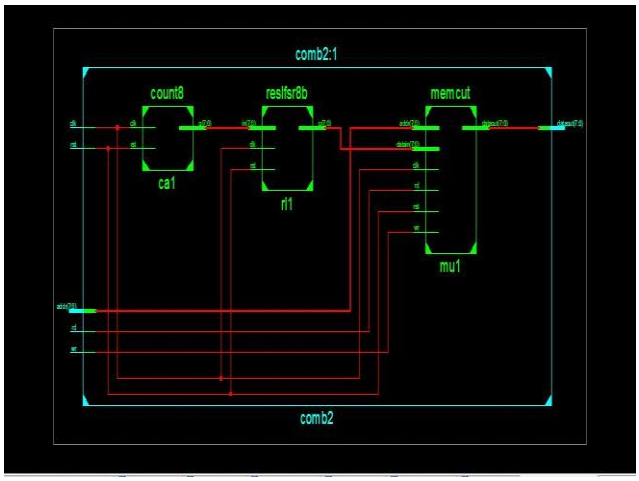

Fig-6: Reseeding LFSR

The architecture shown in Fig. 4 can be used to test the built-in circuits to reduce the storage and time to generate the test patterns.

Counter used to produce the automatic generation of seed continuously which are feed to reseeding L-F-S-R to generate required pseudo-random pattern called as test pattern which will be provided to CUT. Test patterns are generated through reseeding LFSR and are given to CUT. The schematic diagram of the proposed system is shown in Fig6. The proposed method is completed using verilog code.

- **Conclusion and future scope :**

Reseeding has been planned as an efficient technique for testing circuits with random-pattern resistant faults, since it are able to do complete fault coverage with an appropriate range of check vectors. During this paper a brand new reseeding technique for L_F_S_R based check pattern generation, appropriate for test-per-clock B_I_S_T schemes, was planned. The generation of the seeds is performed on- the-fly by the inversion of the logic values of a number of the bits of the L_F_S_R next state. This paper represents a way to come up with check pattern appropriate for circuits with Random Pattern Resistant Fault The technique may be enlarged to satisfy the necessity for low power, low time demand and low volume of check knowledge. Reseeding will primarily be applied for BIST that targets minimization of the check length and complete fault coverage. knowledge time compression for the check pattern needed for testing can indirectly scale back the overall time needed to examine the circuits. On chip testing system may be designed for higher space coverage and reduced memory usage.by using cut back method we can get the fault-free circuit with 100% accuracy.

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