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DESIGN OF ODD-EVEN PARITY GENERATOR USING SIX TRANSISTORS XOR-XNOR MODULE

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Abstract -*In the presented work we have used various XOR-XNOR modules to design the parity generator. Our main aim remains confined to the areas dealing with power, delay and power delay product. We have to design parity generator using various XOR-XNOR modules and compare their performance on the basis of above mentioned factors. The six transistors XOR-XNOR modules involved in the design of parity generator is basic fundamental unit simultaneously giving XOR-XNOR outputs. As we know that power and delay are inversely proportional quantities we will also calculate the power product delay. Simulations have been done on CADENCE VIRTUOSO software on 45nm Technology and all the simulations have been done at 27°C.*

Key Words: *Parity Generator, CMOS Logic Gates, Power Delay Product Etc.*

1. INTRODUCTION

We know that in designing the electronic system today the one factor which is most concerned is that of energy consumption. Low energy consumption is needed for long durability of the energy supplying source such as for space applications where we need constant supply even for months or years.[10] Now as we have advanced various technologies have been evolved using CMOS logic, pass transistor logic, low power gates and many more. Now days to reduce the power consumption the testifying approach is to lower down the power supply but because of supply reduction there are various other anomalies which arise such as increase in delay functionality of the circuit vitiates.[7] So now a day while designing the electronic system our main aim remains to lower down the energy dissipation.

In power reduction there are various factors involved and to reduce the energy consumption in electronic gadgets and devices first we have to understand what are various terms involved which are given below in the equation as [1]

$$p = \sum_i V_{DD} V_{SWING} C_{load\alpha\rightarrow} f + V_{DD} \sum_i I_{isc} V_{DD} I_1 \text{.....1}$$

Above given equation the first term represents scaling element C_{load} represents the output capacitance at a junction I, the given power supply represents by $V_{DD,}$ α is junction changeover movement and the frequency which has been supplied is f. The source supply is equal to the output voltage fluctuation with reference to many cases. The second term signifies the zero resistance current which is rolling from the voltage source to bottom node i.e. ground at this point I_{isc} is held for short circuit power[2][3]. I_1 is seepage current. To reduce the power consumption first stint of equation is done away with and to lower down the junction capacitance the inner meeting point voltage swipe is shirked.

1.1 PARITY GENERATOR:

Parity generator plays an integral part in digital communication for correcting and detecting the error. Whenever we transmit the data from one point to another point then noise gets marred into the data which has been send.[4][] Due to this there is chance of message transformation in bit form which can change from 0 to 1 or 1 to 0. To done away all these miseries we add parity bit at the last of the message signal depending the no. of ones in that message if no. of ones are odd then to make odd parity we add 0 or vice versa and if no. of ones are odd then to make the even parity we add the 1 at the last of the message signal.

1.2 EVEN PARITY GENERATOR:

Even parity generator adds no. of ones in such a manner that it makes no. of ones in the transmitted message signal even depending upon the no. of ones in the message signal is odd or even. If in the transmitted message signal the no. of one is odd then even parity generator adds bit as one and vice versa.

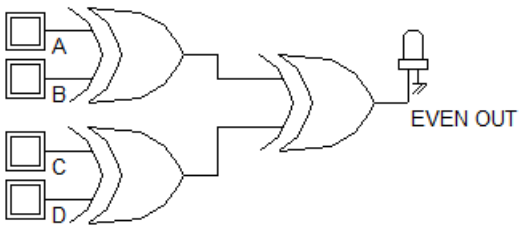

Fig.1: Even parity generator

Depending upon the equations written above we have form

$$P_E = A \oplus B \oplus C \oplus D$$

$$P_E = (\bar{A}B + A\bar{B}) \oplus (\bar{C}D + C\bar{D})$$

$$P_E = (AB + \bar{A}\bar{B})(\bar{C}D + C\bar{D}) + (A\bar{B} + \bar{A}B)(\bar{C}\bar{D} + CD) \text{.....2}$$

the truth table of the even parity generator. From the truth table we can see that in even parity generator when no. of ones is odd then parity bit is one and when no. of ones are even then parity bit is '0'.

Table 1: Even parity generator truth table

Inputs				Even out
A	B	C	D	P_E
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	1
1	1	1	1	0

1.3 ODD PARITY GENERATOR:

In odd parity generator we have incorporated the XNOR gate which is able in detection of odd no. of ones. Whenever in the transmitted message signal there is even no. of ones the odd parity generator add parity bit as one and when no. of ones are odd then it adds parity bit as zero.

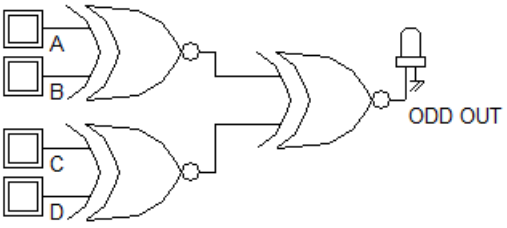

Fig. 2: Conventional Odd Parity Generator

In the truth table given below we can see that whenever there is even no. of ones in the information transmitted the parity bit added by the odd parity generator is one and whenever the input message signal has odd no. of one the parity bit would be one. In the odd parity generator we have XNOR gate employed. In fig 2 we can see the basic connection of the XNOR blocks.

Table 2: Odd parity generator truth table

4 Bit Message				Odd out
A	B	C	D	P_O
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

2. Review of XOR/XNOR design

2.1 Six-transistor XOR-XNOR Gate

To decrease the number of transistor count, we use this six-transistor XOR/XNOR circuit [4]. For the generation of Even and Odd Parity generator, XOR-XNOR gate is used based on pass transistor. This circuit design is based on cross coupled PMOS structure. To create the complement, the complementary cross coupled NMOS structure is too applied. Threshold voltage losses associated with pass transistor XOR circuit can also be eradicated by using feedback topology in this circuit [5][6].

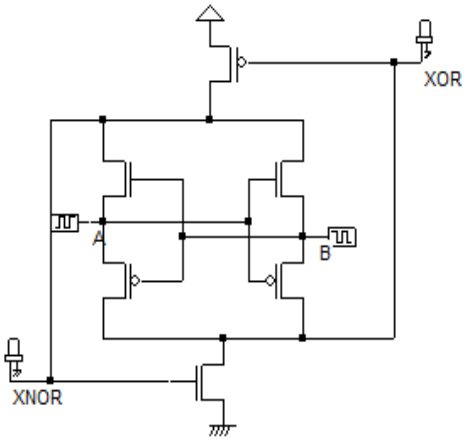

Fig.3: Six-transistor XOR-XNOR gate

2.2 Design of the odd even parity generator using six transistor XOR-XNOR modules:

In parity generator circuit we have used cantankerous attached NMOS and PMOS devices. In the given circuitry to employ the opposite the cantankerous attached NMOS arrangement also incorporated. Minimal supply fatalities accompanying with the CMOS device circuitry can also be reduced by incorporating the reaction methodology in the presented module. [10] In implementing the parity generator we have used the conventional methodology by connecting two gates at non generative level i.e. at the same level and output of both the gates going to the third gate. By implementing this design we can obtain odd and even results simultaneously. In the presented circuitry we have

totally 18 gates employed. We have given total four inputs naming A,B,C,D and responses named as even and odd. Below presented circuitry resembles the conventional parity generator.

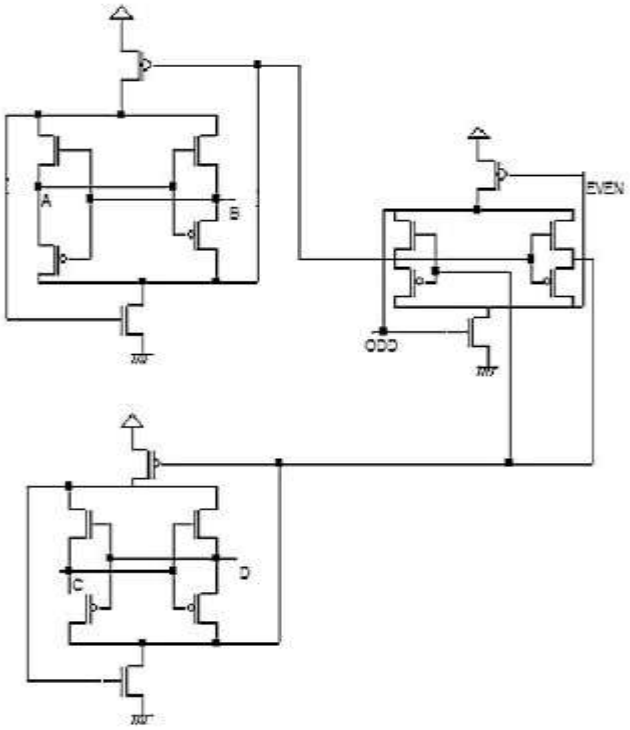

Fig. 4: Odd & Even Parity Generator Using Six Transistor XNOR-XOR Gate

In the above given figure the including four inputs and two outputs whenever there is odd no. of one the even parity would be one and when there is even no. of one there will high signal for odd parity. The truth table of this module will be same like the conventional one parity generator. Now after implementing this design we will investigate the circuit on different measures likewise power, delay, power delay product etc. Now the energy dissipation of this circuitry can be could be fragmented in dual parts one is dynamic power and second one is static part. The static power comprised of the supply power wastage and seepage current and dynamic power dissipation occurs during switching of the circuitry i.e. whenever circuit goes from on to off and vice versa.[8] Here each block is working as a XOR-XNOR simultaneously from the last block we have taken the even and odd outputs simultaneously. Hence it totally depends on the incorporation of the XOR-XNOR gates if we want to improve the efficiency of the circuit. [9] In the above given circuit we simultaneously obtain the even odd output involving four inputs. The connection amongst the XOR-XNOR module is of conventional type.

3. RESULTS AND DISCUSSIONS

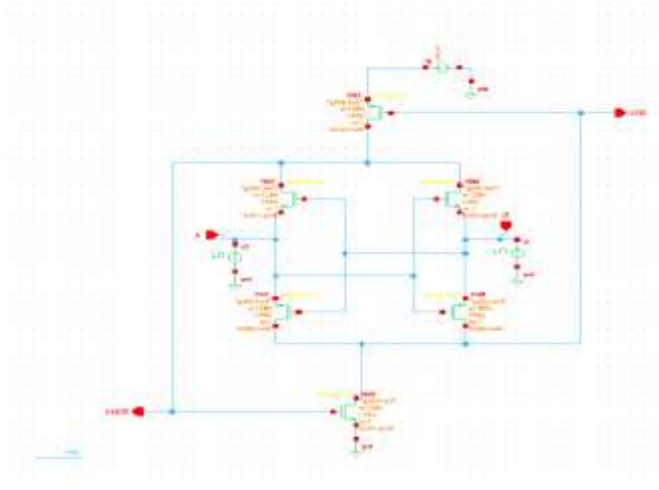

Fig.5: Schematic of six transistor based XOR-XNOR module

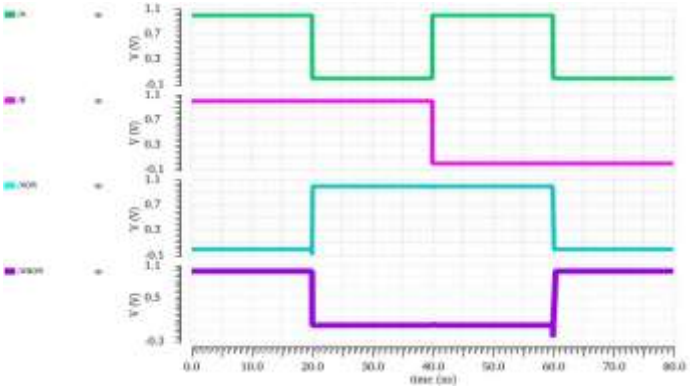

Fig.6: Output wave form six transistor based XOR-XNOR module

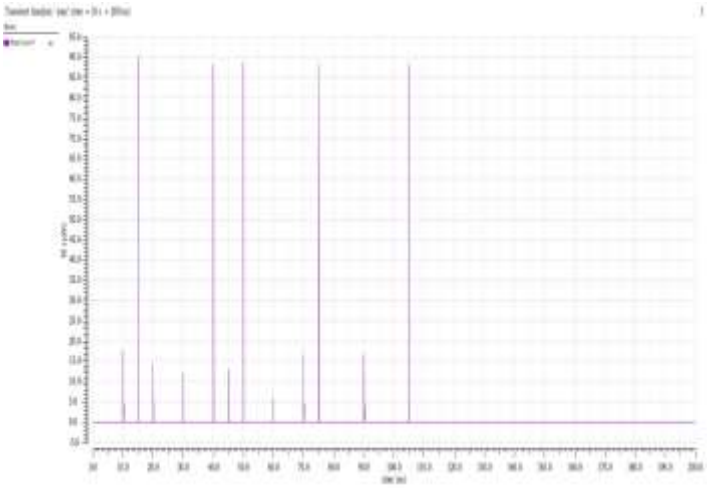

Fig.7: Power Waveform of six transistor based XOR-XNOR module

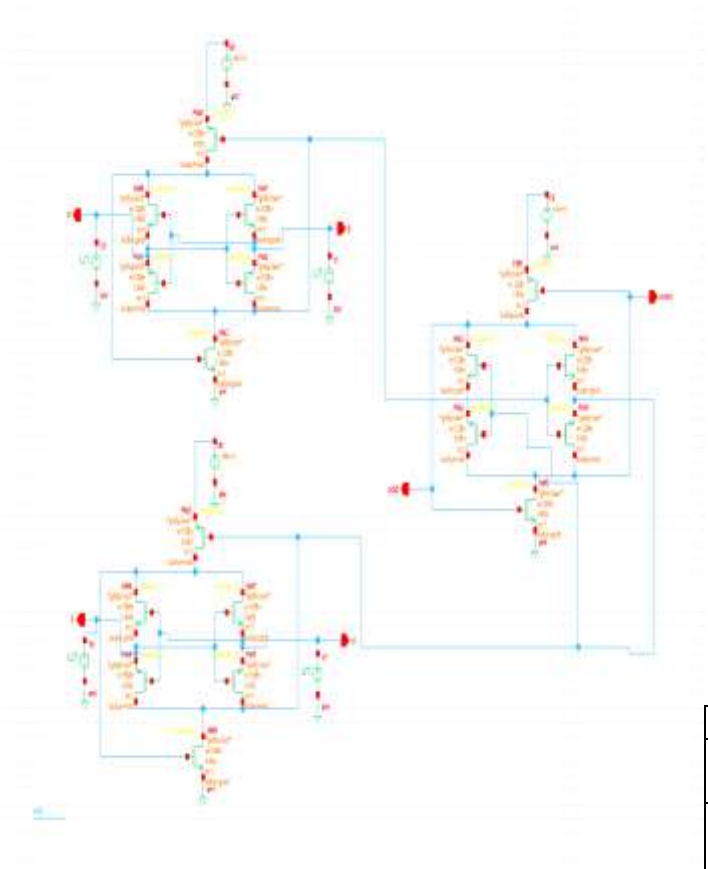

Fig.8: Schematic diagram of parity generator using six transistor based XOR-XNOR module

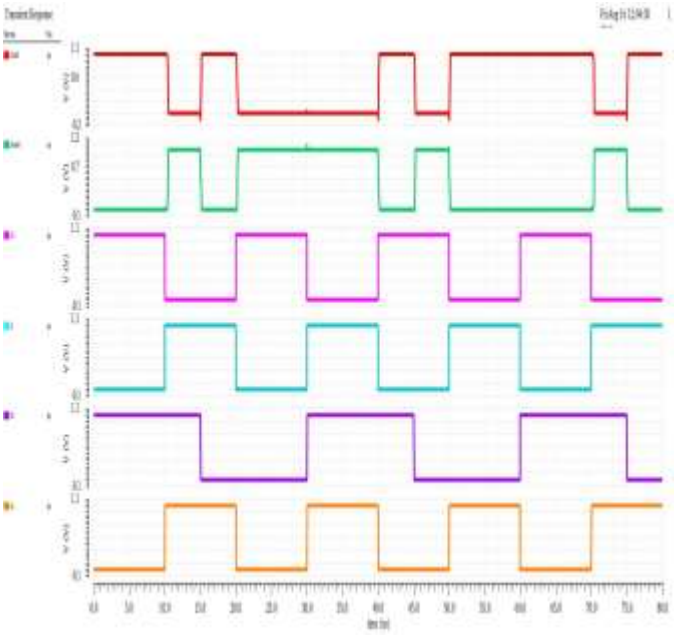

Fig.9: Output waveform of parity generator

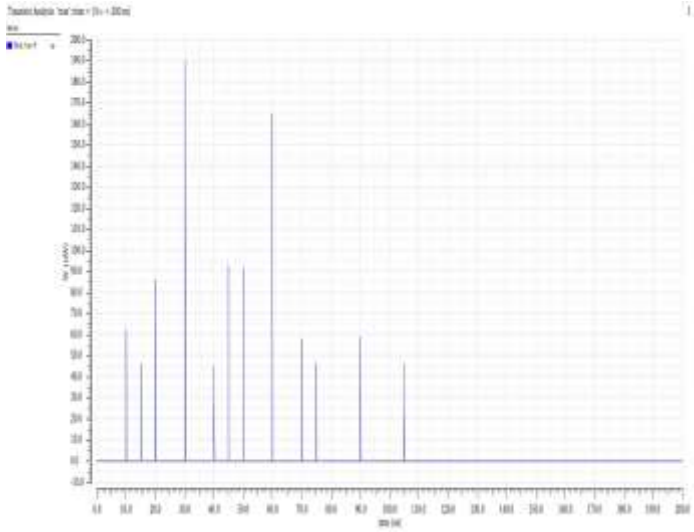

Fig.10: Power waveform of parity generator

Table3: simulation results including various parameters

Design	Power (µw)	Delay(ns)	PDP(pj)
six transistor XOR-XNOR module	92µw	.2533	23.30
Parity generator using six transistor XOR-XNOR module	191	5.18	990

4. CONCLUSION

The above simulations have been done using Cadence Virtuoso at power supply of 1V. The simulations have been performed on 45nm technology. The comparison on different parameters likewise power, delay and power delay product have been performed. As we can see that parity generator consumes more power and hence higher power delay product.

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