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Implementation of Low Power 32-bit Carry-Look ahead Adder using Adiabatic Logic

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Abstract –*Adiabatic logic is low power logic, in this paper an adiabatic logic based 32-bit carry look ahead adder is designed and implemented on the basis of efficient charge recovery logic (ECRL). Power dissipation of the proposed technique is compared with conventional CMOS circuit. The adiabatic (ECRL) shows less average power consumption than the conventional CMOS technique. The adder lies in the critical path of all the arithmetic operations so it plays a crucial role in determining the overall system performance. A schematic and simulation of proposed circuit is implemented in cadence virtuoso 6.1.5 using 45nm technology.*

Key Words: ECRL adiabatic logic, Carry-Lookahead Adder, energy recovery, average power, cadence virtuoso, 45nm technology.

1. INTRODUCTION

In present scenario power dissipation is one of the important parameter while designing any portable devices or embedded devices. The devices are said to be portable if it is minimized in terms of components like transistor, register, capacitor etc, which is one of the prime motto of present generation. According to Moore's law the transistors embedded on IC gets doubled for every 18 months. Most of our customer demand long battery life for portable devices. If the power dissipation is larger in any devices, internally it heats the system. Hence to overcome the above situation it requires heat sink, which further increases the device size, therefore use of heat sink is not an appropriate solution for portable devices [2].

Hence VLSI designers have come up with new technique called adiabatic logic. As compared to conventional logic, adiabatic logic circuits are widely used to reduce power consumption. Depending on the technique used in adiabatic logic i.e. either partially or fully, the energy is stored in load capacitor and can be recaptured back to power supply [5].

1.1 Conventional Logic Switching

In conventional charging power dissipation is mainly during switching activities. The source of the pull-up network is given to the power supply V_{DD} where as the source of pull-down network is given to ground. During steady state depending on the input signal one of the transistors in pull-up or pull-down network is ON. The energy required during discharging is provided by equations (1) to (4).

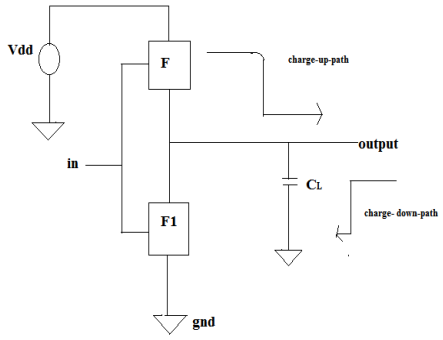


Figure -1: Conventional CMOS logic gate

Consider an example of inverter with conventional charging as shown in figure1 here PMOS transistor turns ON when the input logic gate is low and hence if forms the direct path between V_{DD} to output and load capacitor C_L gets charged.

The total charge Q taken from supply voltage can be given as

$$E = C_L V_{DD}^2 \ldots\ldots\ldots\ldots (1)$$

During charging the energy stored in load capacitance is given by

$$E_{charge} = \frac{1}{2} C_L \cdot V_{DD}^2 \ldots\ldots\ldots (2)$$

The NMOS transistor turns ON when the supply voltage is high. Hence it takes direct path from output to ground and whatever the charge is stored in load capacitance, it

gets discharged through NMOS transistor. The energy required during discharge of a capacitance is given by [2]

$$E_{discharge} = \frac{1}{2} C_L \cdot V_{DD}^2 \ldots\ldots\ldots\ldots (3)$$

Therefore the total energy required for the conventional logic circuit is sum of energy charge and discharge. Therefore

$$E_{total} = E_{charge} + E_{discharge}$$
$$= \frac{1}{2} C_L . V_{DD}^2 + \frac{1}{2} C_L . V_{DD}^2$$
$$E_{total} = C_L . V_{DD}^2 \ldots\ldots\ldots\ldots (4)$$

From the above equation we can say that in conventional logic we can reduce power either by scaling the supply voltage or by varying the size of the capacitance.

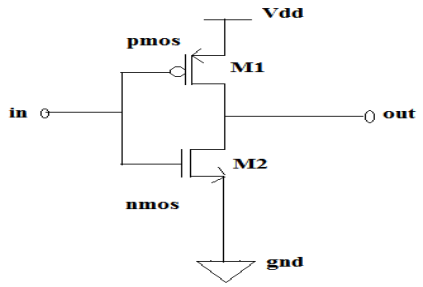


Figure- 2: schematic of a static CMOS inverter

1.2 Adiabatic Logic Switching

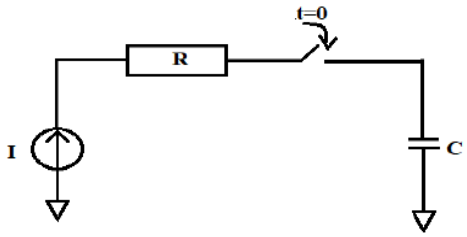


Figure -3: Adiabatic logic energy charging

Figure 3 show the simple RC circuit to demonstrate adiabatic logic charging. In conventional charging we used constant voltage source where as in adiabatic charging varying current source is used to charge the capacitor. Initially at t=0 the load capacitance doesn't contain any charge in it. The voltage across capacitance as a function of time't' is given by,

$$V_C(t) = \frac{1}{C} * I(t) * T \ldots\ldots\ldots\ldots (5)$$

The current at current source can be given as,

$$I(t) = C * \frac{V_C(t)}{T} \ldots\ldots\ldots (6)$$

The energy dissipation in adiabatic circuit can be given as,

$$E_{diss} = R \int_0^T I^2(t) dt \ldots\ldots\ldots\ldots (7)$$

Therefore $$E_{diss} = R I^2(t) T \ldots\ldots\ldots (8)$$

Use equation [6] in equation [8] we get,

$$E_{diss} = \frac{RC^2 V_C^2(t) T}{T * T} \ldots\ldots\ldots (9)$$

$$E_{diss} = \frac{RC}{TCV_C^2(t)}$$

Therefore $$E_{diss} = \frac{RC}{TCV^2(t)} \ldots\ldots\ldots (10)$$

From equation [10] we can clearly observe that,

If T=2RC then $E_{diss} = 0.5CV^2(t) \ldots\ldots\ldots (11)$

If T>2RC then $E_{diss} < 0.5CV^2(t) \ldots\ldots\ldots (12)$

From the above equations we can say that by reducing charge time 'T' or reducing resistance 'R' we can easily reduce the power dissipation.

Basic rules to be followed for designig adibatic logic circuit:

- Replace the PMOS and NMOS tranistor of pull-up and pull-down network by T-gates.
- Use expanded pull-up and pull-down network to drive the true and complimentry output.
- Two networks in the changed circuit, is utilized by both chargeing and dischargeing load capacitor.

2. EFFICIENT CHARGE RECOVERY LOGIC (ECRL)

Moor and Jeong proposed theory of Efficient Charge Recovery Logic (ECRL). The schematic logic block of ECRL is shown in figure 4. The structure of ECRL is similar to that of CVSL (Cascade Voltage Switching Logic). It consist of two cross-coupled PMOS transistor M1 and M2 and two N-Functional blocks. The N-Function block consists of pull-down networks. To recover the energy back to power supply, an AC power supply (CLK) is used. Here two separate outputs, out and out-bar are generated so that clock can always drive capacitance with constant load. Here output flowing due to cross coupled connection of PMOS transistor is opted [5].

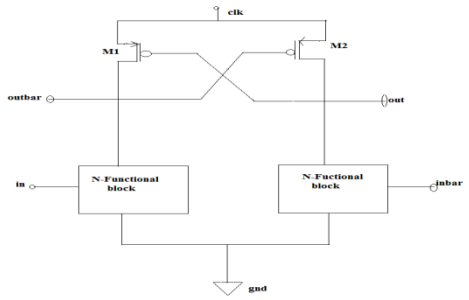


Figure- 4: basic schematic block diagram of ECRL

Some times ECRL faces problems for non-adiabatic loss on pre-charge and recover phase. This problem arises due to threshold voltage of PMOS transistor, i.e. when clock reaches threshold voltage 'V_{tp}' of PMOS transistor, it turns OFF. Hence the path between recovery and clock gets disconnected, which results in incomplete recovery. The loss incurred in ECRL is given by

$$ECRL = C_L \left|V_{tp}\right|^2 / 2 \ldots\ldots\ldots (13)$$

From equation (13) we can say that non-adiabatic energy loss is highly dependent on CL (Load Capacitance) and independent of frequency.

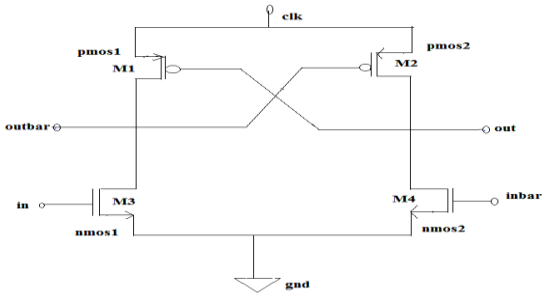


Figure- 5: schematic diagram ECRL inverter

Let us consider ECRL inverter shown in figure 5. Here we observe that, initially 'in' is high and 'in-bar' is at low potential, when CLK rises from ground to V_{DD} output 'out' remains in low state where as output 'out-bar' follows clock. When clock reaches V_{DD} output, out and 'out-bar' holds values V_{DD} and zero. Further it is used as input for next stage, when clock falls from V_{DD} to zero the energy present in 'out-bar' is transformed to CLK. Hence the charge gets recovered back.

3. CARRY-LOOKAHEAD ADDER

The principle behind adders is to perform addition between given bits; there are many numbers of adders to perform addition. Some of them are ripple carry adder, carry look ahead adder, carry skip adder, parallel prefix adder and so on. Ripple carry adder is very simple and cost effective adder where the propagation delay is high, because each time the MSB bit has to wait for computation for carry from LSB bit. To overcome the above problem related to propagation delay, carry look ahead adder is implemented [2].

Carry look ahead adder consists of one bit full adder as shown in figure7. A full adder takes two binary numbers in addition to carry bit. The output is the sum and another carry out. The carry propagation and generation is used in full adder. The output propagation of carry is evaluated by XORing two input Ai and Bi and output of carry generation is taken by ANDing.

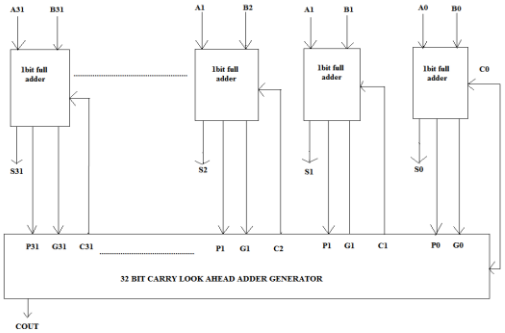


Figure -6: block diagram 32-bit carry look ahead adder

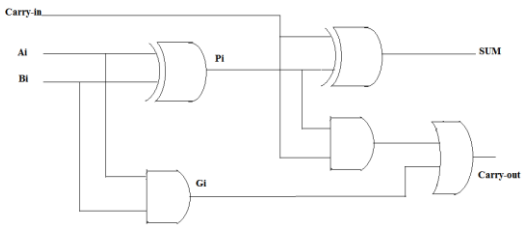


Figure -7: carry propagation and carry generation

The output expression for sum and carry bit can be given as

$$Si = Ai \oplus Bi \ldots\ldots\ldots\ldots\ldots (14)$$

$$Ci+1 = Cin(Ai \oplus Bi) + Ai \cdot Bi \ldots\ldots\ldots\ldots\ldots (15)$$

The intermediate outputs, propagate and generate Pi and Gi can be given as

$$Pi = Ai \oplus Bi \ldots\ldots\ldots\ldots (16)$$

$$Gi = Ai \cdot Bi \ldots\ldots\ldots\ldots (17)$$

Substitute equation (16) in (14)

$$Si = Pi \oplus Cin \ldots\ldots\ldots\ldots\ldots (18)$$

Substitute equation (17) in (15)

$$Ci+1 = Cin \cdot Pi + Gi \ldots\ldots\ldots\ldots (19)$$

4. DESIGN AND SIMULLATION

The implementation of this project work is done using cadence virtuoso 6.1.5 and simulation is done using ADE-L Spectre (Analog Design Environment-L). Here all the implementations are performed using 45nm technology. Adiabatic logic ECRL (Efficient Charge Recovery Logic) are designed and compared with conventional CMOS logic. Inverter, basic gates AND, OR, EX-OR and 32 bit CLA adder are implemented using adiabatic ECRL logic in 45nm technology and the functionality is verified by doing necessary simulations as shown in figures 8 to 21.

4.1 Implementation of Inverter Using CMOS

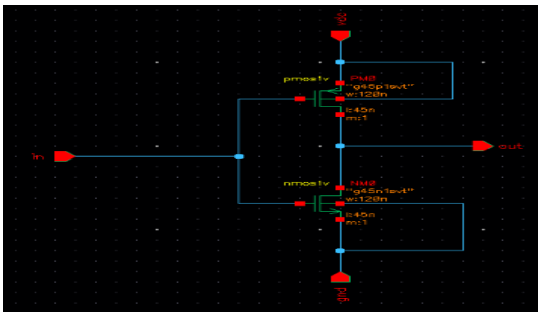


Figure -8: Schematic of CMOS inverter

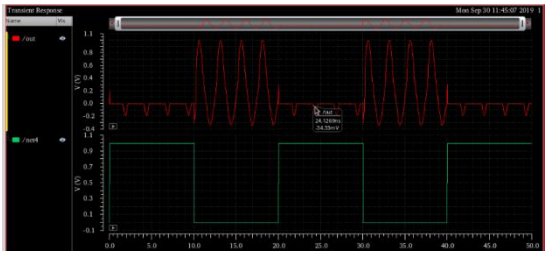


Figure -9: Transient analysis of CMOS inverter

4.2 Implementation of Inverter Using ECRL Adiabatic logic

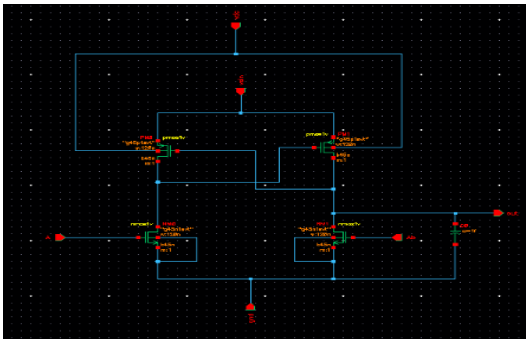


Figure -10: Schematic of ECRL inverter

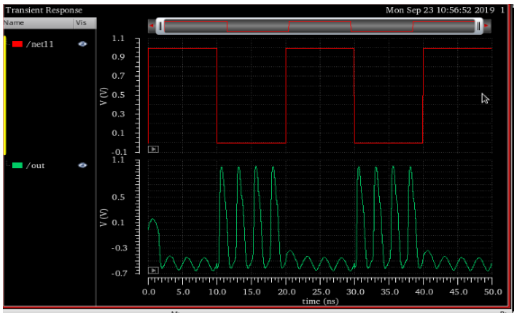


Figure -11: Transient analysis of ECRL inverter

4.3 Implementation of AND gate Using ECRL Adiabatic logic

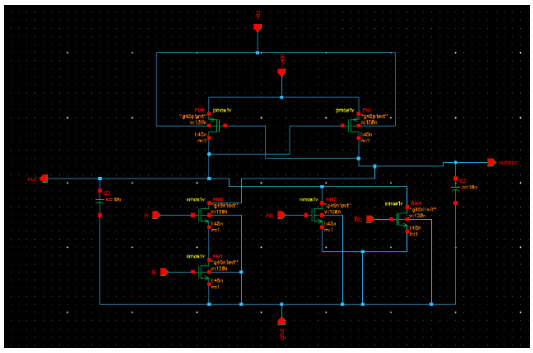


Figure -12: Schematic of ECRL AND gate

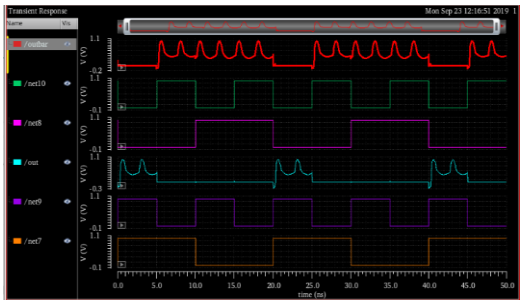


Figure -13: Transient analysis of ECRL AND agte

4.4 Implementation of OR gate Using ECRL Adiabatic logic

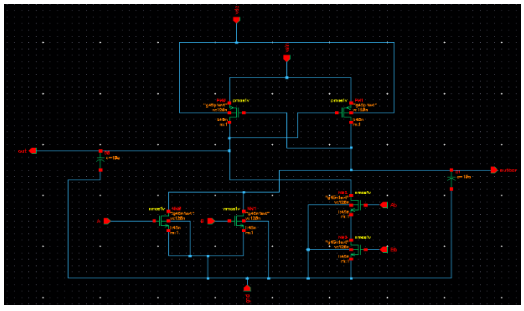


Figure -14: Schematic of ECRL OR gate

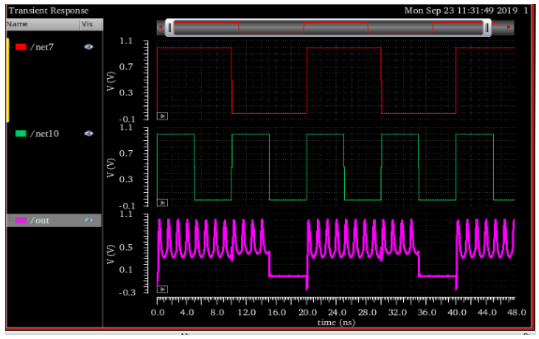


Figure -15: Transient analysis of ECRL OR agte

4.5 Implementation of EX-OR gate Using ECRL Adiabatic logic

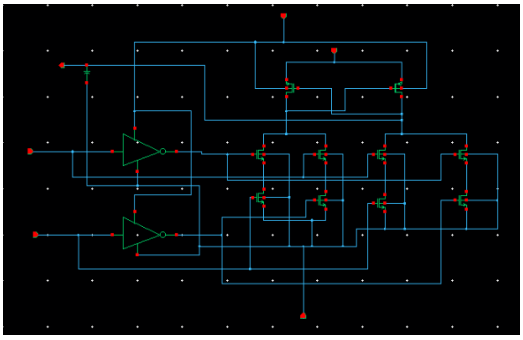


Figure -16: Schematic of ECRL EX- OR gate

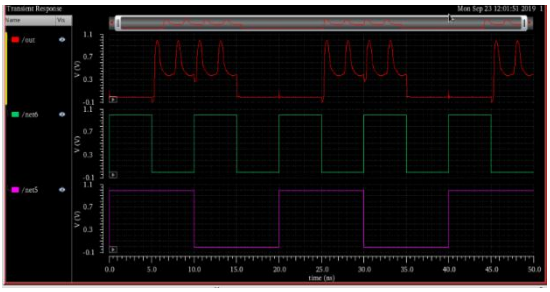


Figure- 17: Transient analysis of ECRL EX-OR gate

4.6 Implementation of 16-Bit CLA Using ECRL Adiabatic Logic

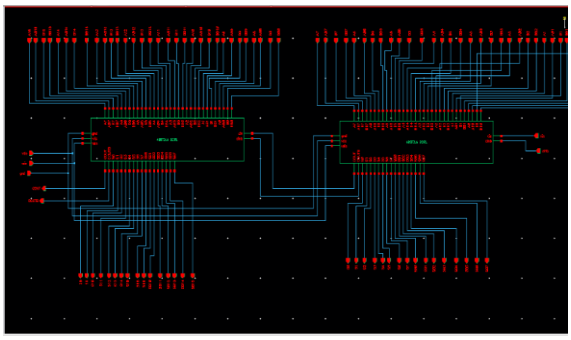


Figure -18: Schematic of ECRL 16-bit CLA.

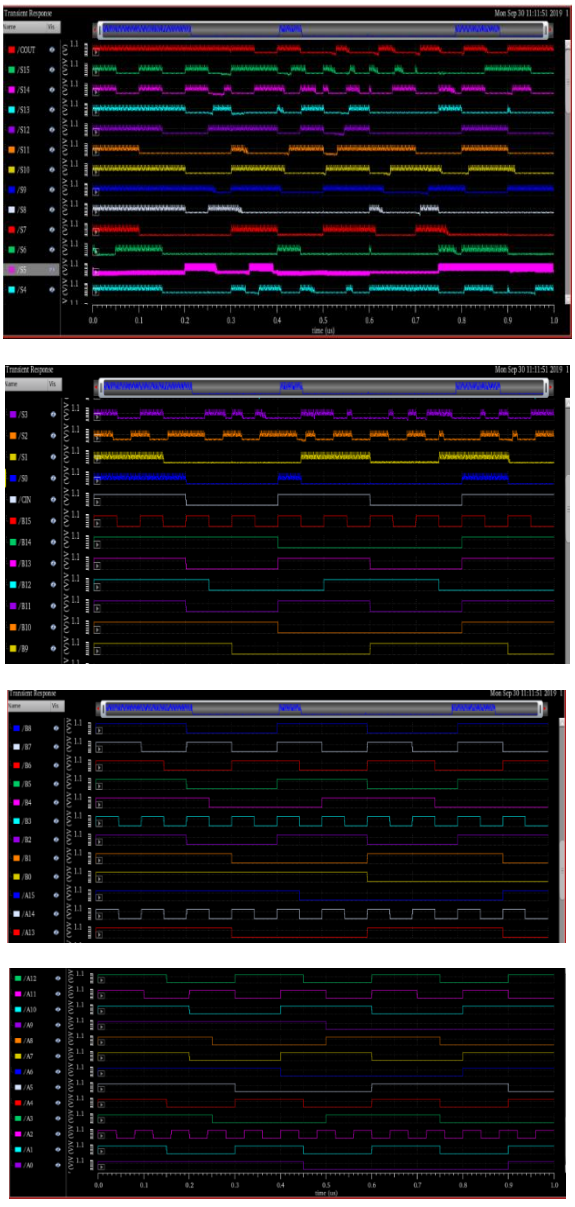


Figure- 19: Transient analysis of ECRL 16-bit CLA

4.7 Implementation of 32-Bit CLA Using ECRL Adiabatic Logic

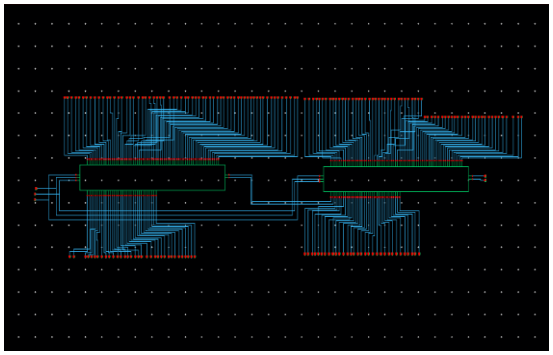
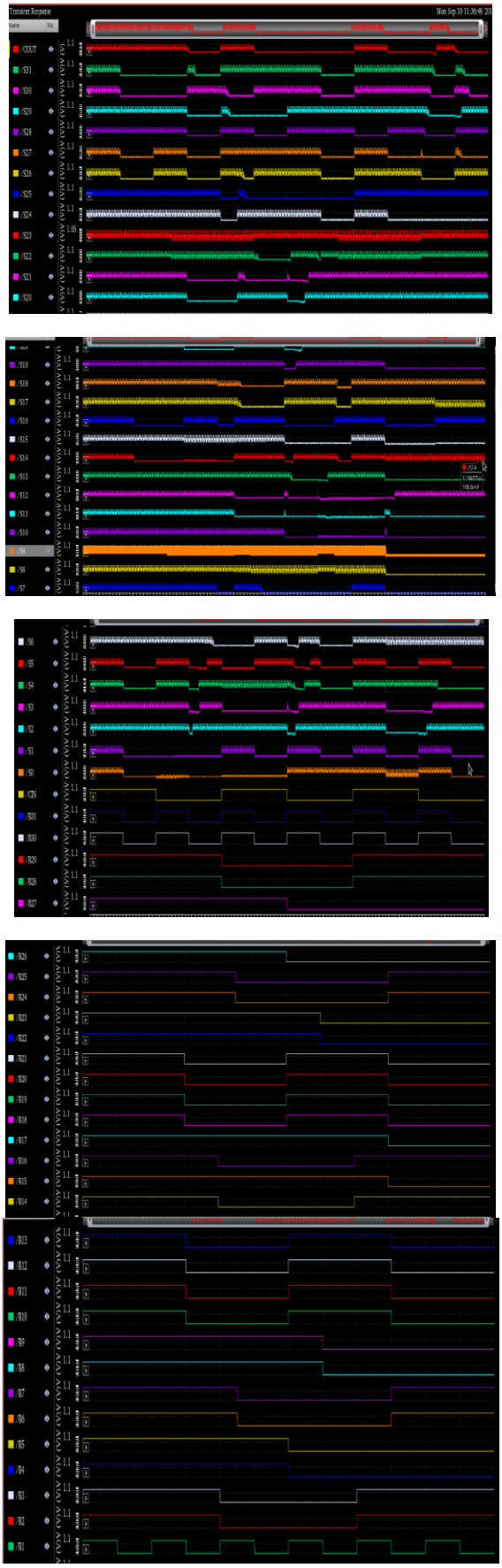


Figure -20: Schematic of ECRL 32-bit CLA.



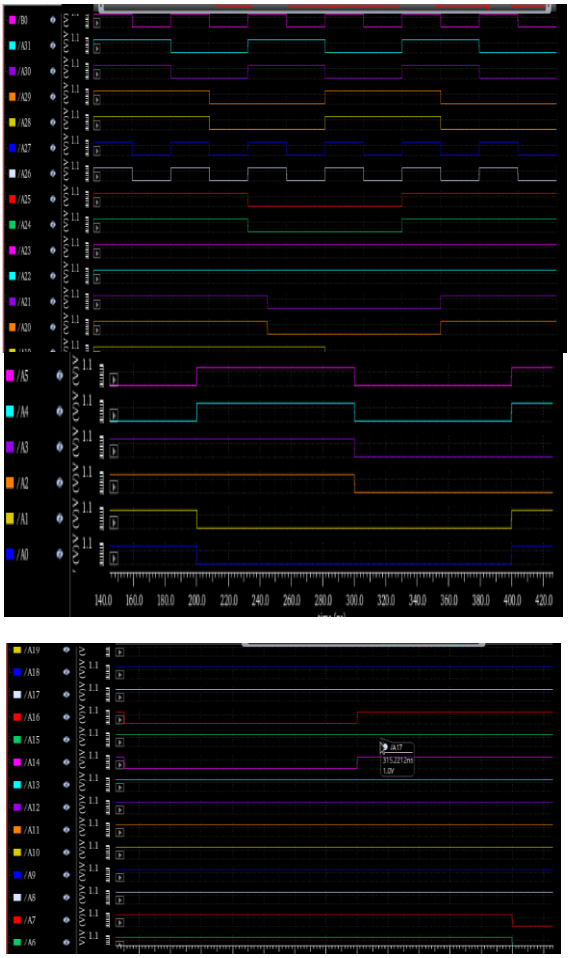


Figure -21: Transient analysis of ECRL 32-bit CLA

5. POWER DISSIPATION ANALYSIS

5.1Power Dissipation Analysis for Basic Gates

The table 1 demonstrates the average power consumed by logic gates namely Inverter, AND, OR and EX-OR under conventional and adiabatic logic (ECRL). From the above observations we can say that adiabatic logic consumes less power than that of conventional logic.

Table-1: comparison between ECRL and CMOS

Technology	ECRL(nw)	CMOS(µw)
Inverter	53.83	3.073
AND	71.06	4.306
OR	63.74	5.854
EX-OR	159.5	6.694

5.2 Power Dissipation Analysis for Adders

The table 2 shows the average power consumption calculated for ECRL and static CMOS for 4bit, 8bit, and 16bit and 32bit carry look ahead adder. From the computation we say that CLA using adiabatic ECRL have low power dissipation than static CMOS logic.

Table-2: comparison between ECRL and CMOS Adders

Technology	4bit (µw)	8-bit (µw)	16-bit (µw)	32-bit (µw)
ECRL	1.966	3.23	10.56	36.76
CMOS	35.2	55.34	100.6	230.03

6. CONCLUSION

The implementation of 32-bit carry look ahead adder is done for both conventional CMOS logic and adiabatic ECRL logic. From all the above observations made and from simulated results, we can conclude that the adiabatic adders consume less power than that of conventional adders. Adiabatic logic circuits consume less power when compared to conventional CMOS logic circuits and also there is less wastage of power, hence there is more demand for adiabatic logic circuits.

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