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Review Paper on Distributed Canny Edge Algorithm Implementation on FPGA

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Abstract - *Image processing is one of the emerging methods in communication. In the image processing edge detection (identifying the edge points in digital image) is the most common preprocessing step in many image processing algorithms such as image enhancement, image segmentation, tracking and image/video processing. Among the existing edge detection algorithms distributed canny edge detector is one of the most widely used edge detection algorithms due to its superior performance, Implementation using FPGA reduces the latency significantly and this allows the block-based canny edge detector to be pipelined very easily with existing block-based codec. FPGA-based hardware architecture of the proposed algorithm will be synthesized on Xilinx virtex-5.*

Key Words: Distributed image processing, Canny edge algorithm, parallel processing, FPGA.

1. INTRODUCTION

In the image processing, edge location (distinguishing the focuses in picture) is the most widely recognized preprocessing venture in many picture handling calculations, for example, image enhancement, image segmentation and picture/video coding. Among the current edge discovery calculations canny edge locator is a standout amongst the most broadly utilized edge identification calculations because of its unrivaled execution. Canny edge recognition is a procedure to extricate helpful auxiliary data from various vision questions and decrease the measure of information, and reduce the amount of data to be processed. Canny edge detection algorithm is more computationally complex as compared to other edge detection algorithms, such as the Roberts and Sobel algorithms. Disadvantage of Canny edge detector is that it consumes a lot of time due to its complex computation, and it is difficult to implement to reach the real-time response. Directly applying the original canny algorithm at the block-level leads to excessive edges in smooth regions and loss of significant edges in high-detailed regions. To solve this problem, a distributed canny edge detection algorithm that adaptively computes the edge detection threshold based on the block type and the local distribution of the gradients in the picture block. To overcome these short comings of traditional canny algorithm, an adaptive threshold selection algorithm [2] has put forward to compute the high and low threshold for each block based on the kind of block and the neighborhood distribution of pixel angles in the block. In order to demonstrate the parallel efficiency of the proposed distributed canny edge detection algorithm, an FPGA based hardware implementation of the proposed algorithm gives a bird eye view of the embedded system for implementing the distributed canny edge detection algorithm based on an FPGA platform. It is composed of several components, including an embedded microcontroller, a system bus, peripherals & peripheral controllers, external Static RAMs (SRAM) and memory controllers, and an intellectual property (IP) design for the proposed distributed Canny detection algorithm. The embedded controller facilitates the exchange of the picture information from the host PC (through the PCIe or USB controller, local bus, and memory controller) to the SRAM, at that point from the SRAM to the nearby memory in the FGPA for handling and finally save back to the SRAM. Xilinx and Altera offer extensive libraries of intellectual property (IP) in the form of embedded micro-controller sand peripherals controller. Therefore in our design focus only on the implementation of the proposed algorithm on the Spartan-6.

2. RELATED WORK

Basic concepts of edge detection edge detection are an image processing technique for finding the boundaries of objects within images. [1]

Divya D et.al [2] used a distributed canny edge detection algorithm to find the edges, in which its yield reduced memory requirements, decreased latency and increased throughput with no loss for simulation using Xilinx Virtex-2 pro platform and tested using ModelSim.

Dhanalakshmi et.al [3] in the image processing the data of edge detection is very large, so the achievement of high speed of image processing is a difficult task. FPGA can overcome this difficult task and it is an effective device to realize real-time parallel processing for vast amounts of image and video data.

Wenhao He et.al [4] explains traditional canny edge detector has two shortcomings. First, the threshold of the algorithm needs to be set by manual. Secondly, the algorithm is very time consuming and cannot be implemented in real time. A new self-adapt threshold canny algorithm is proposed.

Malathy H Lohithaswa [5] the work shows the implementation of Canny Edge detection algorithm on FPGA. When the detection is very large, so the achievement of high speed of image processing is a difficult task. Field Programmable Gate Array (FPGA) can overcome this difficult task and it is an effective device to realize real-time parallel processing for vast amount of image and video data.

Avinash G et.al [6] discuss the accuracy and complexity algorithm. An efficient canny algorithm is designed using Xilinx System Generator which utilizes JTAG Hardware co-simulation approach. Accuracy is compromised in order to make it more efficient.

Bhagesh C. Maheshwari et.al [7] has implemented a re-sizable canny edge detector to increase in size and complexity of a design make it harder and slower to work at a lower level of abstraction.

3. EDGE DETECTION TYPES

There are many methods to detect edge detection. The most well-known strategy for edge detection is to differential the separation of a picture. The first order derivatives in a picture are figured utilizing the slope, and the second request second-order derivatives are obtained utilizing the Laplacian. However the dominant part of various strategies might be gathered into two classes

Gradient: The Gradient technique recognizes the edges by searching for the greatest and least in the principal first order derivatives of the picture.

Laplacian: The Laplacian technique scans for zero crossing in the second differential of the picture to discover edges. An edge has the one-dimensional state of an incline and computing the differential of the picture can feature its area.

3.1 Gradient Method

1. Sobel Edge Detection- The operator consists of a pair of 3×3 convolution kernels. One kernel is simply the other rotated by 90°.

2 Prewitt Edge Detection- Prewitt operators is similar to the Sobel operator and is used for detecting vertical and horizontal edges in images.

3. Roberts Edge Detection- The Roberts Cross operators performs a simple, quick to compute, 2-D spatial gradient measurement on an image.

3.2 Laplacian Method

The Laplacian is a 2-D isotropic proportion of the second spatial subsidiary of a picture. The Laplacian of a picture features districts of fast force change and is in this manner regularly utilized for edge recognition. The Laplacian is regularly connected to a picture that has first been smoothed with something approximating a Gaussian Smoothing channel so as to diminish its responsiveness to noise.

3.3 Canny Edge Detection

Canny built up a way to deal with determine an ideal edge locator dependent on three criteria identified with the discovery execution. The model depended on a stage edge defiled by added substance white Gaussian noise. A block diagram of the canny edge detection algorithm is shown in Fig.1 the original canny algorithm consists of the following steps:

1. Smoothing the input information picture by Gaussian mask. 2. Computing the Gradient (angle) Gx and vertical inclination Gy at every pixel area by convolving with angle.3. Computing the gradient magnitude G and direction θ Gat each pixel location. 4. Applying Non Maximal Suppression to thin edges. 5. Processing high and low limits dependent on the histogram of the slope greatness for the whole picture. 6. Performing hysteresis thresholding. 7. Applying morphological thinning on the resulting edge map.

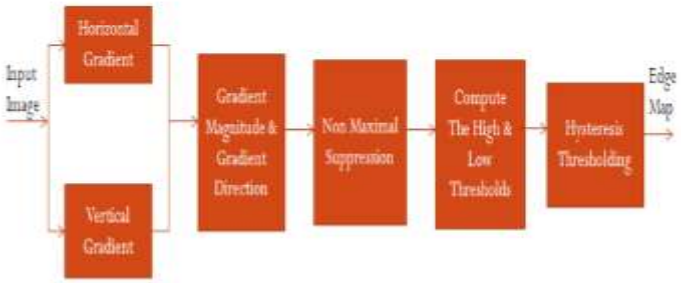

Fig -1: Block Diagram of the Canny Edge Detection Algorithm

Canny edge works on the entire picture and has a latency that is relative to the extent of the picture. While performing the original canny algorithm at the block-level would speed up the operations, it would result in loss of significant edges in high-detailed regions and excessive edges in texture regions. Normal pictures comprise of a blend of smooth areas, surface districts and high detailed by point and such a blend of districts may not be accessible locally in each block of the entire image. In distributed canny edge detection, algorithm is proposed which removes the inherent reliance between the different blocks with the goal that the picture can be separated into blocks and each block can be processed in parallel as shown in fig.2

The input is given to the image block, the uploaded image is converted into gray color image, 2-D to 1-D conversion and resizes. The image and the preprocessing unit output is

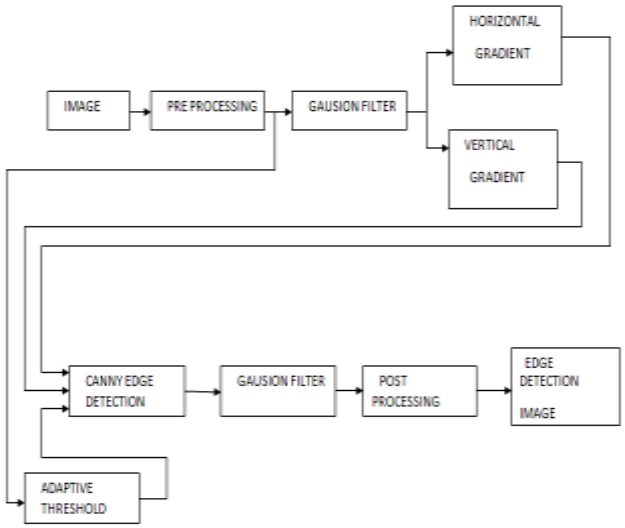

Fig – 2: Block Diagram of the Distributed Canny Edge Detection Algorithm

Passed to Gaussian filter where the image get smoothened. A picture slope is a directional change in the force or color in a picture. The slope of the picture is one of the essential building obstructs in picture handling. For example, the Canny edge detector uses image gradient for edge detection the output is passed through the canny edge detection and again a Gaussian filter, to convert from 1D to 2D the post processing is used and final block is edge detected image, these steps are same for a hardware implementation.

4. DISTRIBUTED CANNY EDGE ALGORITHM USING FPGA

In order to demonstrate the parallel efficiency of the proposed distributed canny edge detection algorithm, an FPGA based hardware implementation of the proposed algorithm gives a bird eye view of the embedded system for implementing the distributed canny edge detection algorithm based on an FPGA platform. It is composed of several components, including an embedded microcontroller, a system bus, peripherals and peripheral controllers, external Static RAMs (SRAM) and memory controllers and a licensed innovation structure for the proposed distributed canny edge algorithm. The embedded controller arranges the exchange of the picture information from the host PC (through the PCIe or USB controller, framework nearby transport, and memory controller) to the SRAM, at that point from the SRAM to the neighborhood memory in the FGPA for handling and finally putting away back to the SRAM. Xilinx and Altera offer broad libraries of licensed innovation IP in the in the form of embedded micro-controller sand peripherals controller. Therefore in our design focused only on the implementation of the proposed algorithm on the Xilinx.

5. CONCLUSION

The original canny's depends on frame level data to predict the maximum and minimum thresholds and consequently has latency relative to the edge measure, so as to minimize the time taken and meet constant necessities, novel canny edge discovery calculation is utilized which can figure edges of numerous block in the meantime. To help this, a versatile limit choice technique is recommended that predicts the maximum and minimum edges of the whole picture while just handling the pixels of an individual block. This result in three benefits: 1) Significant reduction in the latency. 2) Better edge detection performance 3) the possibility of pipelining the canny edge detector with other block-based image codecs, this method is scalable and has high detection performance. It will show that algorithm can detect all visually important edges in the image for various block sizes .Finally, the algorithm will be mapped onto a Xilinx Spartan-6 FPGA.

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