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A Novel Three Phase Asymmetric Multi Level Inverter Fed To Induction Motor Drive

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Abstract - A new three phase asymmetric multi level inverter fed to induction motor is proposed. The proposed topology is based on a cascaded connection of single-phase multilevel converter units and full-bridge converters. In order to generate more number of voltage levels at the output by using different magnitudes of dc voltage sources. This topology is used to generate all positive, negative and zero levels by using a lower number of IGBT's, dc voltage sources and controlling circuit parameters that leads to lower THD, reduction in installation space, cost of inverter is low, reduced electromagnetic interference (EMI) and increasing the life of inverter also. It reduces not only switching devices such as power electronic components, and also reduces the blocked voltages at each IGBT. An Asymmetric cascaded multi level inverter uses different magnitudes of voltages that leads to the more number of levels at the output as compared to that of the Symmetric cascaded multi level inverter. The performance of a new three phase asymmetric cascaded multi level inverter fed to induction motor drive have been verified by using MATLAB/SIMULINK.

Key Terms- Three phase asymmetric, multilevel inverter, h-bridge basic units, induction motor.

1. INTODUCTION

Over many years, Induction motor drives have been popularly used for variable speed control applications in industries. In recent years, Multi Level Inverters (MLI's) are more popular because of their huge advantages over than the conventional inverters. The main advantages of MLI's are lower voltage changing rate, lower total harmonic distortion (THD), lower amount of switching loss and better power quality.

The cascaded MLI's (CMLI's) are gaining popularity because of easy control, easily identification of error circuits and modularity of the devices. Cascaded MLI's are categorized based upon their using dc sources are as follows,

1) Symmetric CMLI's and

2) Asymmetric CMLI's

Symmetric CMLI's are having same magnitude of applied voltages on both sides of the inverter. Asymmetric CMLI's are having different magnitudes of applied voltages on both sides of inverter. Asymmetric CMLI's are generate more number of levels at the output than the symmetric CMLI's. Symmetric CMLI's are having bidirectional switches includes driver circuit, two number of IGBT's and power diodes if that may leads the increasing of total cost of an inverter and installation space also be increased. Different symmetric CMLI's are on [5]. Asymmetric CMLI's are having unidirectional switches from voltage point of view and bidirectional switches from the current point of view. Unidirectional switches include of an IGBT with an antiparallel diode. Different Asymmetric CMLI's are on [6].

The proposed one is developed by using a new single-phase H-bridge basic units[1].

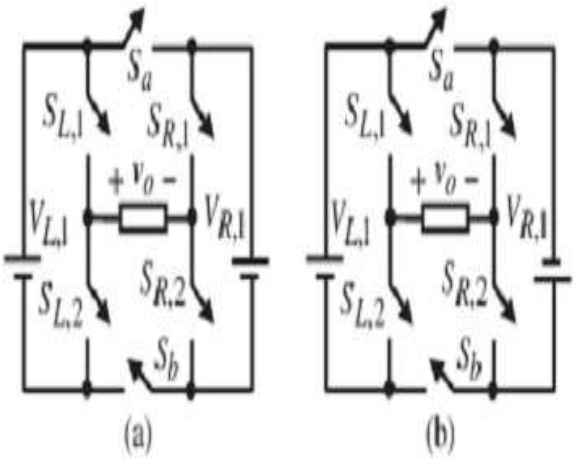

Fig 1: Seven Level Inverters. (a) First Proposed Topology (b) Second Proposed Topology.

Table 1:OUTPUT SEQUENCE VOLTAGES OF A H-BRIDGE

STATE	$S_{L,1}$	$S_{L,2}$	$S_{R,1}$	$S_{R,2}$	S_a	S_b	Vo
1	0	1	1	0	0	1	$V_{R,1}$
2	1	0	0	1	0	1	$V_{L,1}$
3	1	0	1	0	0	1	$V_{R,1}+V_{L,1}$
4	1	0	1	0	1	0	0
	0	1	0	1	0	1	
5	1	0	0	1	1	0	$-V_{R,1}$
6	0	1	1	0	1	0	$-V_{L,1}$
7	0	1	0	1	1	0	$-(V_{R,1}+V_{L,1})$

Considering Table I, to generate all voltage levels (odd and even) in the proposed topology. From the table I, we observes the three positive levels, three negative levels and one zero level are generate by using single h-bridge. By cascading the two h-bridges, we are generate 49 levels with a maximum amplitude of output voltage.

II. PROPOSED TOPOLOGY

The basic novel h-bridge is shown in Fig 1,it consists of six unidirectional power switches named as SL,1,SL,2,SA,SB,SR,1 and SR,2. These power switches are able to generate seven levels, in the similar way the proposed one consists two h-bridges. The two h-bridges consists totally twelve IGBT's and four insulated dc voltage sources. The twelve IGBT 's named as SL,11, SL,12, SL,21, SL,22, SR,11, SR,12, SR,21, SR,22, SA,1, SA,2, SB,1 and SB,2.

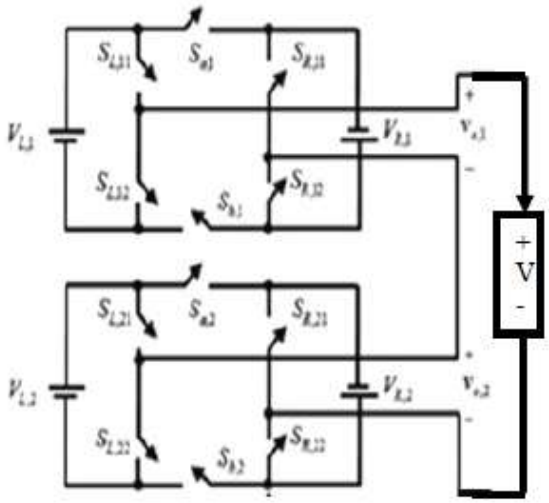

Fig 2: Asymmetric 49-Level Inverter

The proposed topology for single-phase Asymmetric 49-level inverter is shown in Fig 2.

The power switches of each leg is activated simultaneously that means for each and every switching pattern, the switches SL,1 or SL,2, SR,1 or SR,2, SA or SB of a single h-bridge.

Magnitudes of dc voltage sources for a single h-bridge is

VR,1=Vdc (1)

VL,1=2Vdc (2)

The total output voltage is determined by the equation,

Vo(t)= Vo,1(t)+ Vo,2(t) (3)

Vo,1(t) is the maximum voltage at the output of first h-bridge,

Vo,1(t)=VR,1+VL,1=3Vdc (4)

Vo,2(t) is the maximum voltage at the output of second h-bridge,

Vo,2(t)=7VR,1+7VL,1=21Vdc (5)

Hence the total output voltage of proposed system is

Vo(t)= Vo,1(t)+ Vo,2(t)=24Vdc (6)

Then the output voltage from peak to peak is

Vp-p=2 Vo(t) (7)

The blocked voltages by all IGBT's in the first bridge is

Vblock,1=4(VR,1+VL,1) (8)

The maximum amount of blocked voltages in the proposed system is

Vblock=4(VR,1+VL,1+VR,2+VL,2) (9)

III. PERFORMANCE OF A THREE-PHASE ASYMMETRIC INVERTER FED INDUCTION MOTOR

Asymmetric inverter has four dc voltage sources having ranges are VR,1=10V, VL,1=20V, VR,2=70V and VL,2=140V.

An electric motor convert's electrical power to mechanical power in its rotor. Induction motors are widely used, especially poly phase induction motors, which are frequently used in industrial drives. When induction motors are given supply, Motor draws a very high current initially, due to which voltage dip will forms, which show the effect on the power system network. In order to avoid voltage dip, we employ new controller to generate more levels at ouput voltage.

IV. SIMULINK MODELS AND RESULTS

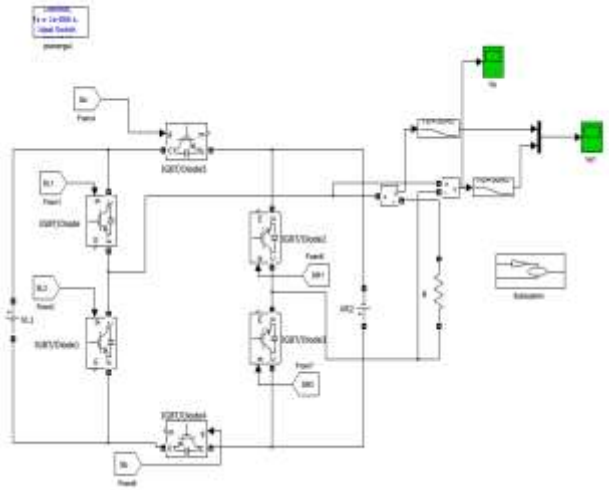

Fig 3: Seven Level Inverter

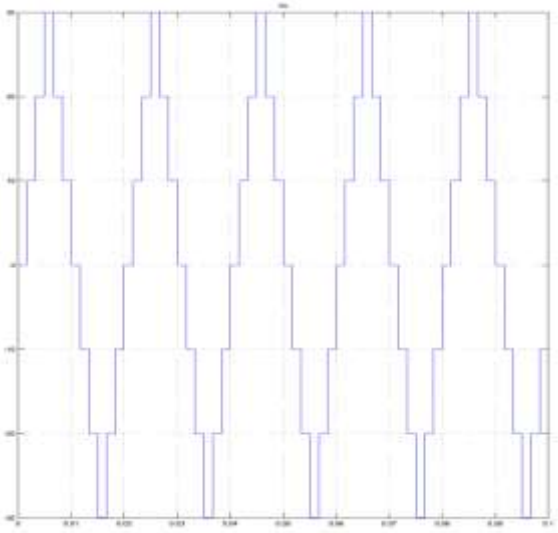

Fig 4: Seven Level Inverter Simulink Results

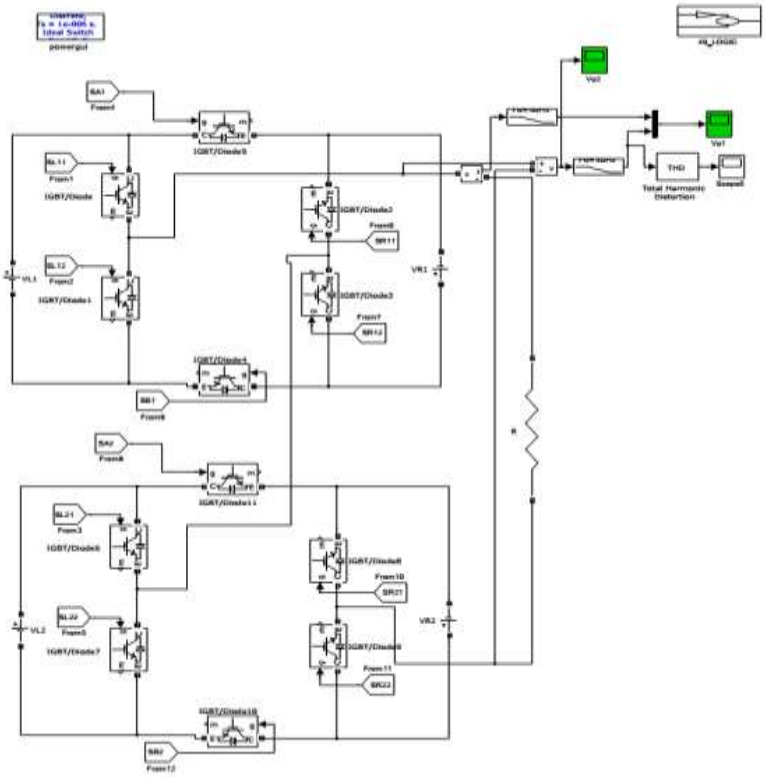

Fig 5: Asymmetric 49-Level Inverter

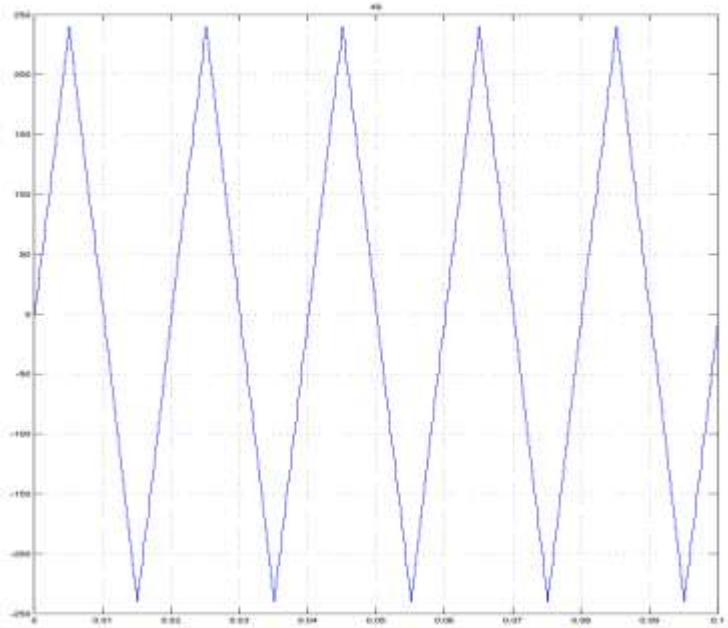

Fig 6: Output Voltage

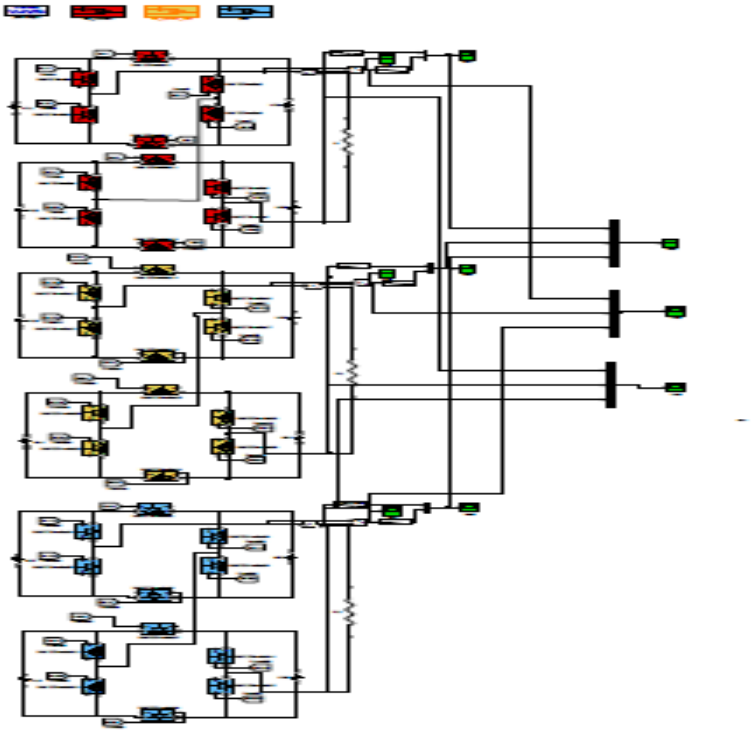

Fig 7: Three-Phase Asymmetric Inverter

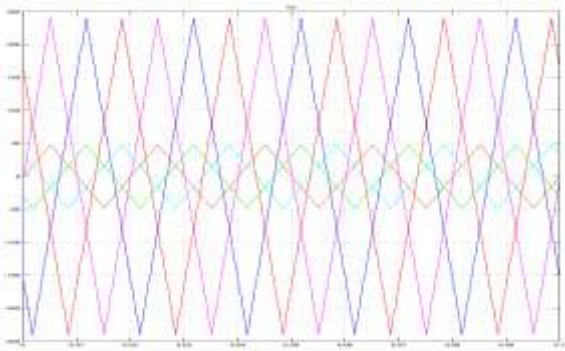

Fig 8: Three-Phase Current and Voltage

Fig 9: Three-Phase Filtered Current and Voltage

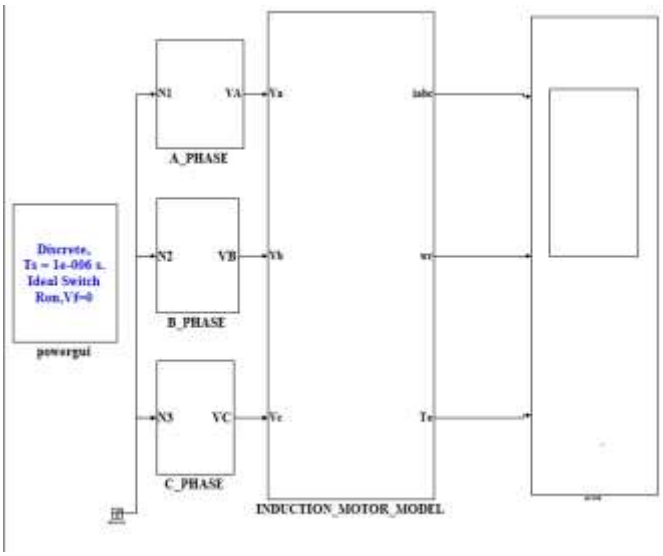

Fig 10: Three-Phase Mli Fed to Induction Motor Drive

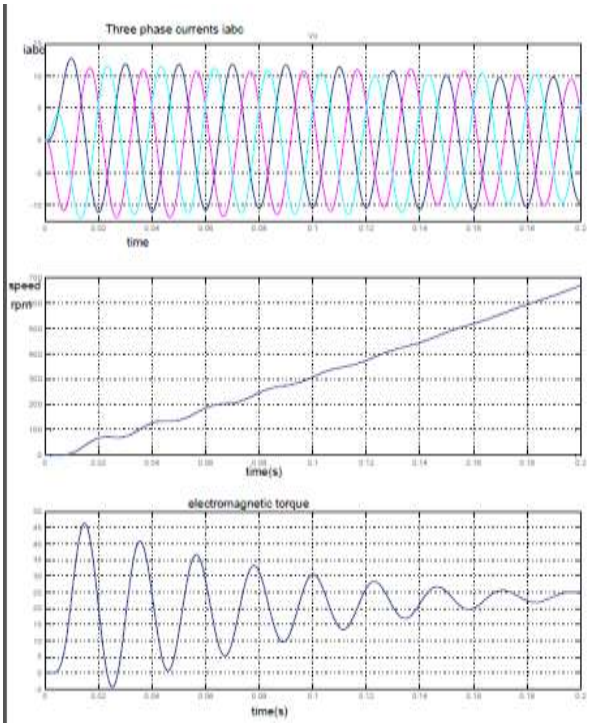

Fig 11: Induction Motor characteristics, (a)Iabc , (b)Rated speed and (c) Electomagnetic Torque

V. CONCLUSION

In this paper, two basic topologies have been proposed for multilevel inverters to generate seven voltage levels at the output. The basic topologies can be developed to any number of levels at the output where the 49-level and general topologies are consequently presented. In addition, a new algorithm to determine the magnitude of the dc voltage sources has-been proposed. The proposed general topology was compared with the different kinds of presented topologies in literature from different points of view. According to the comparison results, the proposed topology requires a lesser

number of IGBTs, power diodes, driver circuits, and dc voltage sources. Moreover, the magnitude of the blocking voltage of the switches is lower than that of conventional topologies. However, the proposed topology has a higher number of varieties of dc voltage sources in comparison with the others. The proposed topology was verified through the matlab/Simulink platform through 49-level inverter.

V. REFERENCES

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