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32nm FinFET Based Comparator for Flash ADC

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Abstract - *Power consumption is a major problem in all electronic circuits. In order to achieve the power consumption, circuit scaling is important. In CMOS based circuits scaling should be possible up to constrained range after that it will present short channel impacts. To defeat above disadvantage FINFET has been presented. Comparator is one of the components most importantly required in analog to digital converter. Op-Amps are the major constituent of analog and mixed-signal systems. Speed interest for rapid applications, for example, ADC and DAC lead to expanded interest for amplifiers with high gain and speed. FinFET is a standout amongst the most encouraging advancements to structure underneath 50nm. FinFET transistors in simple circuit configuration presents noteworthy enhancement contrasted with conventional one entryway CMOS structure. In this paper, we present a FINFET based comparators for high speed Flash ADC. The main parameters considered in the performance analysis are delay, frequency and power consumption. LT-Spice simulation software is used for design and analysis of the comparator circuits in the above specified 32nm scaling range.*

***Key Words*: Flash ADC, FinFET, Comparator, Low Power**

1. INTRODUCTION

Analog-to-digital converters are used to convert real world analog signals into digital representations of those signals. As we know that the digital signal processing can then efficiently extract information from the signals. ADCs find use in communications, audio, sensors, video and many other applications [1]. High-speed, low-resolution ADCs are used in oscilloscopes, digital high-speed wire line and wireless communications and radar. Flash and time-interleaved ADCs architectures are typically used for high-speed applications. There are various types ADC architecture in which first is pipeline ADC [2]. Its operating speed is high but below flash with medium resolution. Second ADC architecture is SAR ADC [3]. It is appropriate for low power and medium-to-high goals applications with moderate speed. Third ADC design is Sigma-delta ADC [4]. It is reasonable for high goals and low speed applications. Forth ADC architecture is Flash ADC [5]. It can work at fast and low goals. So we can say that Flash ADC is the quickest ADC in correlation with other ADC models. The flash ADC is the best choice in high speed low resolution applications. It is highly used in high data rate links, high speed instrumentation, radar, digital oscilloscopes and optical communications. Since flash ADC is working in parallel change technique, most extreme working recurrence in the scope of gigahertz is conceivable. Comparator design is also a challenge for design of Flash ADCs.

2. FLASH ADC

The General block diagram for a 3 bit Flash ADC is given in below Fig -1. A Flash ADC is framed of mostly three blocks- Resistor ladder, Comparator array and Thermometer to Binary code encoder. Resistor ladder is utilized for producing different reference voltages. The incoming analog signal is compared with these generated reference voltages using the comparator array and the corresponding thermometer code will be generated [6]. These thermometer codes are given to the advanced encoder which will change over them to the relating binary codes.

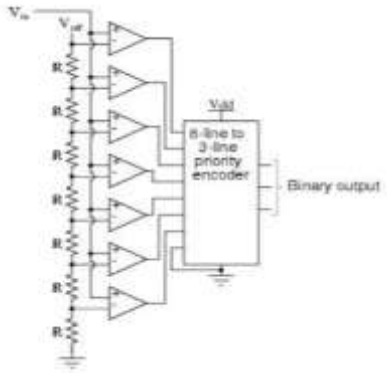


Fig -1: Block Diagram of 3-Bit Flash ADC

3. FINFET TECHNOLOGY

Multi-gate FETs are an option in contrast to planar MOSFETs, which enhanced the drain potential screening out of the channel because of quality of extra gates. In all multi-gate devices, the two gate FETs or tri-gate FETs are increasingly attractive because of littler parasitic capacitances and hearty conduct against irregular dopant conduct. The Trigate FETs are having decreased fringing capacitances yet at the expense of complex creation process. The FinFETs are the rising gadgets in this mechanical time which are having negligible power utilization, insusceptible to short channel effects, littler area necessity and higher speed of activity [7]. The FinFETs are grouped in fundamental two classes: (a) Independent Gate FinFET (IGF) (b) Short Gate FinFET (SGF). IG FinFETs are having four terminals while SGF are otherwise called three terminal FinFETs. The entryways are disconnected in IGF structures while the front and the back doors are shorted to one another in SGF structures as

appeared in Fig -2. SGF structures are having higher ON current when contrasted with IGF structure on the grounds that SGF structure mutually utilizes both the entryways for electrostatic control of the channel. Be that as it may, an IGF structure offers the adaptability to apply distinctive signals on the diverse gates however at the expense of bigger chip territory.

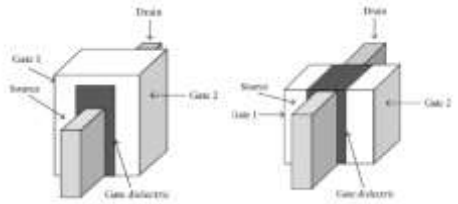


Fig -2: Comparison between SGF and IGF

4. COMPARATOR

Block diagram of an amplifier with a differential input and a single-ended output is shown in Fig -3. Two-stage amplifier is made of four principle parts. This include a differential amplifier in the input, second gain circuit, bias circuit and compensation circuit [8]. Given that the circuit load is capacitive, the buffer stage isn't required in the enhancer. Differential amplifier at the input obtains a larger share of the total amplifier gain to improve noise performance and offset. To have most extreme swing in the yield, the second stage is generally utilized as a straightforward common source. Compensation circuit is additionally used to balance out and the inclination circuit has the errand of giving the predisposition voltages of the amplifier circuit.

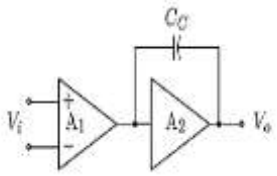


Fig -3: Block Diagram of Two-Stage Op-Amp

4.1 Conventional Two Stage Op-Amp

A customary two phase operational amplifier with compensation capacitor Cc is exhibited in Fig -4. The amplifier incorporates the course phases of voltage to current and current to voltage converters. The primary stage comprises of a differential amplifier that change over the differential information voltages to differential currents. The differential currents are connected to the present current mirror stack that recovers the differential voltage. This is obviously only a differential voltage amplifier. The second stage incorporates a MOSFET regular source that changes over the input voltage of the second stage to the current [9].

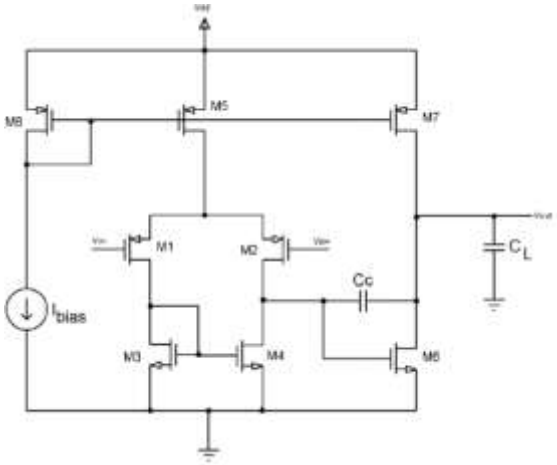


Fig -4: Conventional Two-Stage CMOS Op-Amp

This operation amp is so much utilized that is called conventional two phase operation amp. Capacitor CC is utilized for Miller pay to expand the phase margin.

1.2 Proposed Two Stage Op-Amp

Here, another two-stage single-ended differential amplifier with FinFET innovation is presented. The past circuit executed with MOSFET is supplanted by FinFET transistors [10]. Fig -5 demonstrates the general structure of the amplifier utilized for planning.

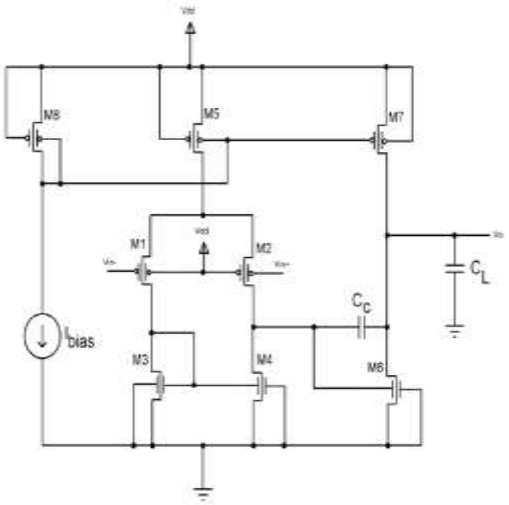


Fig -5: Proposed Two-Stage FinFET Op-Amp

All transistors are FinFET and as appeared in the figure the second gate of every n-FinFET transistors are associated with GND and the back door of p-FinFET transistors is associated with Vdd. Here M1, M2, M3, M4 and M5 frame the main phase of amplifier. M1 and M2 is differential pair and M3 and M4 are utilized as the load for the differential combine transistors. M6 and M7 together assume the job of common source and frame the second phase of amplifier. M5 assumes the job of current source to the amplifier. M8 together with Ibias assumes the job of bias circuit for the

amplifier. Cc is utilized for Miller pay in the amplifier structure.

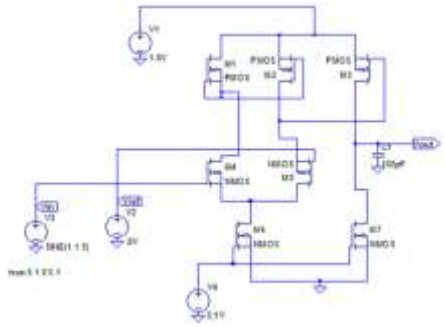
The amplifier open loop gain can be communicated as the increase of two phases:

$Av=(2*gm2*gm6)\ (I5*I6*(\lambda 2+\lambda 3)*(\lambda 6+\lambda 7))$ (1)

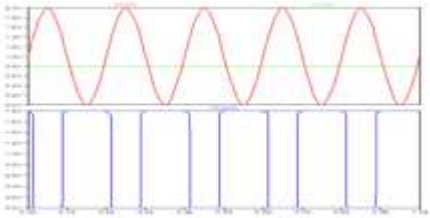
Along these lines, the gain depends to transconductance gm and the channel length modulation parameter λ. FinFET compelling portability is higher than mass transistors due to non-doping channels and subsequently builds gm. Channel length modulation parameter (λ) in FinFET is impressively limited because of better control of short channel impacts in double gate structure. Thus, the gain can be expanded by FinFET.

5. RESULTS AND SIMULATION

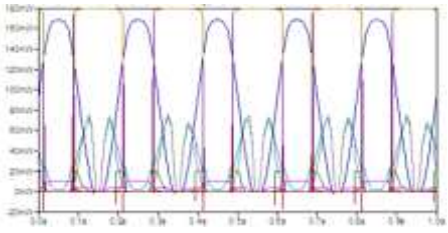
5.1 Schematic of Two Stage CMOS Op-Amp



5.2 Transient Analysis of Two Stage CMOS Op-Amp



5.3 Power Analysis of Two Stage CMOS Op-Amp



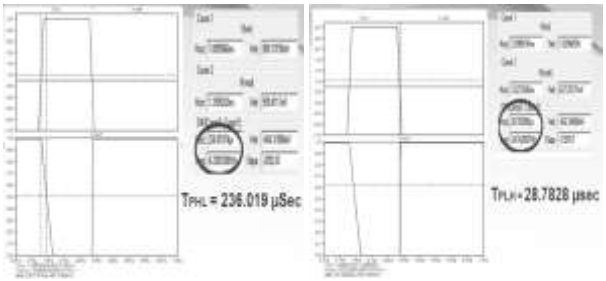
Fclk = 1/T = 1/0.3 sec = 3.33 Hz

Dynamic Power Dissipation = Fclk * Vdd² * CL

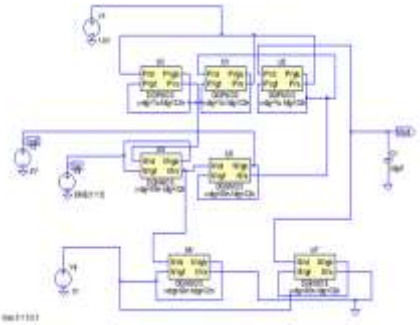
= 3.33 * 1.8² * 100pF = 1.08 nW

Static Power Dissipation = 1.1952 µW

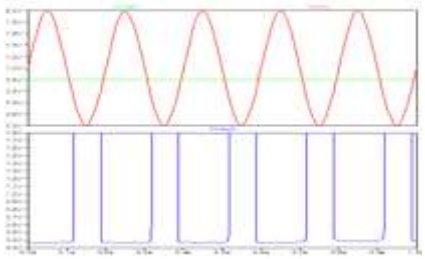
5.4 Propagation Delay of Two Stage CMOS Op-Amp



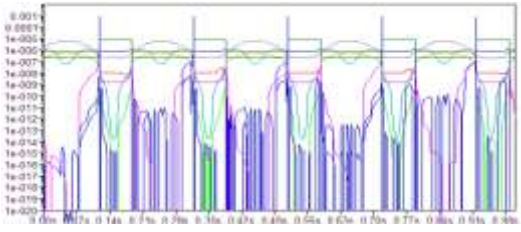
5.5 Schematic of Two Stage FinFET Op-Amp



5.6 Transient Analysis of Two Stage FinFET Op-Amp



5.7 Power Analysis of Two Stage FinFET Op-Amp



Fclk = 1/T = 1/0.3 sec = 3.33 Hz

Dynamic Power Dissipation = Fclk * Vdd² * CL

= 3.33 * 0.8² * 30pF = 0.6393 pW

Static Power Dissipation = 0.268 µW

5.8 Propagation Delay of Two Stage FinFET Op-Amp

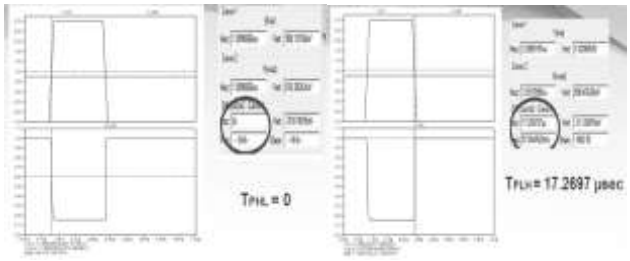


Table -1: Comparison between CMOS Comparator and FinFET Comparator

Parameter	Two Stage Op-Amp using CMOS	Two Stage Op-Amp using FinFET
Technology	180 nm	32 nm
Vdd	1.8V	0.8V
CL	100pF	30pF
Static Power Dissipation	1.1952µW	0.268µW
Dynamic Power Dissipation	1.08nW	0.6393pW
Propagation Delay	TPHL = 236.019µs TPLH = 28.78 µs	TPHL = 0 TPLH = 17.269 µs

5. CONCLUSION

The prerequisite of low power circuits for correspondence applications is expanding because of fast enhancement in frameworks requiring framework on chips (SoC) for example, remote handheld gadgets like tablet PC, advanced cells and Satellite Phones. The flash ADCs are profoundly worthwhile in these respects. Be that as it may, the traditional CMOS based flash ADCs are confined by territory prerequisites and activity delay. The correspondence transfer speeds that are utilized at present for SoC applications require low power ADCs with programmable reference voltage for simple to advanced transformation. The speed of a Flash ADC relies upon the speed of the comparators. FinFET based comparators turned out to be of low power dispersal and engendering delay than MOSFET based comparators.

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