International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395-0056
Volume: 06 Issue: 01 | Jan 2019 www.irjet.net p-ISSN: 2395-0072

FinFET based 3-Bit Flash ADC on 32nm Technology

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Abstract - *Power utilization is a noteworthy issue in every single electronic circuit. So as to accomplish the power utilization, circuit scaling is essential. In CMOS based circuits scaling ought to be conceivable up to oblige extend after that it will show short channel impacts. To overcome this disadvantage FINFET has been introduced. Comparator is one of the segments above all required in simple to advanced converter. Operational Amplifiers are the real constituent of analog and mixed-signal systems. Speed requirement for fast applications, for instance, ADC and DAC lead to extended enthusiasm for amplifiers with high gain and speed. FinFET is a champion among the most reassuring progressions to structure underneath 50nm. FinFET transistors in basic circuit setup presents vital upgrade appeared differently in relation to ordinary single gate CMOS structure. In this paper, we present a FINFET based Flash ADC. The fundamental parameters considered in the execution investigation are delay and power utilization. LT-Spice simulation software is utilized for design and investigation of the circuits in the above determined 32nm scaling range.*

Key Words: **Flash ADC, FinFET, Comparator, Encoder**

1. INTRODUCTION

Analog-to-digital converters are used to convert real world analog signals into digital representations of those signals. As we know that the digital signal processing can then efficiently extract information from the signals. ADCs find use in communications, audio, sensors, video and many other applications [1]. High-speed, low-resolution ADCs are used in oscilloscopes, digital high-speed wire line and wireless communications and radar. Flash and time-interleaved ADCs architectures are typically used for high-speed applications. There are various types ADC architecture in which first is pipeline ADC [2]. Its operating speed is high but below flash with medium resolution. Second ADC architecture is SAR ADC [3]. It is appropriate for low power and medium-to-high goals applications with moderate speed. Third ADC design is Sigma-delta ADC [4]. It is reasonable for high goals and low speed applications. Forth ADC architecture is Flash ADC [5]. It can work at fast and low goals. So we can say that Flash ADC is the quickest ADC in correlation with other ADC models. The flash ADC is the best choice in high speed low resolution applications. It is highly used in high data rate links, high speed instrumentation, radar, digital oscilloscopes and optical communications. Since flash ADC is working in parallel change technique, most extreme working recurrence in the scope of gigahertz is conceivable. Comparator design is also a challenge for design of Flash ADCs.

2. FLASH ADC

The General block diagram for a 3 bit Flash ADC is given in below Fig -1. A Flash ADC is framed of mostly three blocks- Resistor ladder, Comparator array and Thermometer to Binary code encoder. Resistor ladder is utilized for producing different reference voltages. The incoming analog signal is compared with these generated reference voltages using the comparator array and the corresponding thermometer code will be generated [6]. These thermometer codes are given to the advanced encoder which will change over them to the relating binary codes.

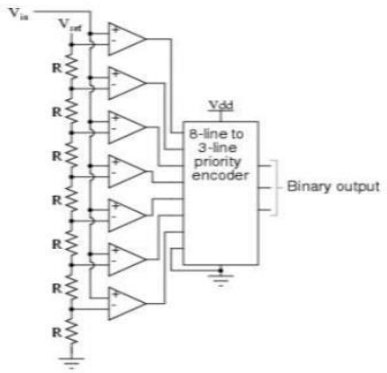


Fig -1: Block Diagram of 3-Bit Flash ADC

3. FINFET TECHNOLOGY

Multi-gate FETs are an option in contrast to planar MOSFETs, which enhanced the drain potential screening out of the channel because of quality of extra gates. In all multi-gate devices, the two gate FETs or tri-gate FETs are increasingly attractive because of littler parasitic capacitances and hearty conduct against irregular dopant conduct. The Trigate FETs are having decreased fringing capacitances yet at the expense of complex creation process. The FinFETs are the rising gadgets in this mechanical time which are having negligible power utilization, insusceptible to short channel effects, littler area necessity and higher speed of activity [7]. The FinFETs are grouped in fundamental two classes: (a) Independent Gate FinFET (IGF) (b) Short Gate FinFET (SGF). IG FinFETs are having four terminals while SGF are otherwise called three terminal FinFETs. The entryways are disconnected in IGF structures while the front and the back doors are shorted to one another in SGF structures as appeared in Fig -2. SGF structures are having higher ON current when contrasted with IGF structure on the grounds

that SGF structure mutually utilizes both the entryways for electrostatic control of the channel. Be that as it may, an IGF structure offers the adaptability to apply distinctive signals on the diverse gates however at the expense of bigger chip territory.

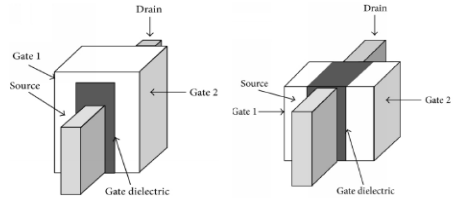


Fig -2: Comparison between SGF and IGF

4. RESISTOR LADDER

The resistor ladder is designed mainly to provide a stable reference voltage to the comparators [8]. The resistor ladder network is formed by 2N resistors which generates the reference voltage. The reference voltage for all comparator is one least significant bit (LSB) less than the reference voltage for the comparator immediately above it. The ladder divides main reference voltage into 2N equally spaced voltages.

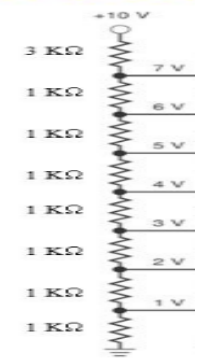


Fig -3: Resistor Ladder for 3-bit flash ADC

5. COMPARATOR

Block diagram of an amplifier with a differential input and a single-ended output is shown in Fig -4. Two-stage amplifier is made of four principle parts. This include a differential amplifier in the input, second gain circuit, bias circuit and compensation circuit [8]. Given that the circuit load is capacitive, the buffer stage isn't required in the enhancer. Differential amplifier at the input obtains a larger share of the total amplifier gain to improve noise performance and offset. To have most extreme swing in the yield, the second stage is generally utilized as a straightforward common source. Compensation circuit is additionally used to balance out and the inclination circuit has the errand of giving the predisposition voltages of the amplifier circuit.

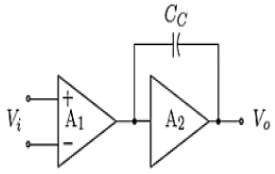


Fig -4: Block Diagram of Two-Stage Op-Amp

4.1 Conventional Two Stage Op-Amp

A customary two phase operational amplifier with compensation capacitor Cc is exhibited in Fig -5. The amplifier incorporates the course phases of voltage to current and current to voltage converters. The primary stage comprises of a differential amplifier that change over the differential information voltages to differential currents. The differential currents are connected to the present current mirror stack that recovers the differential voltage. This is obviously only a differential voltage amplifier. The second stage incorporates a MOSFET regular source that changes over the input voltage of the second stage to the current [9].

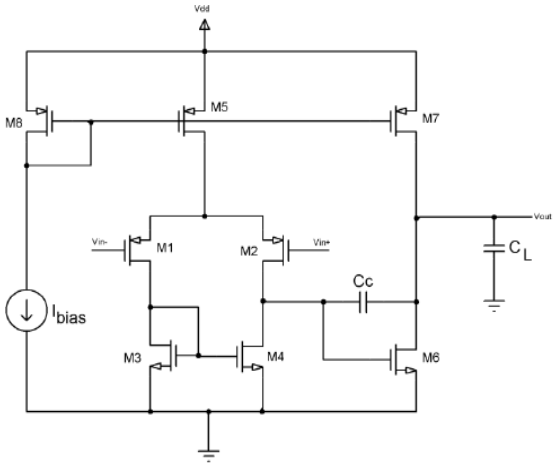


Fig -5: Conventional Two-Stage CMOS Op-Amp

This operation amp is so much utilized that is called conventional two phase operation amp. Capacitor CC is utilized for Miller pay to expand the phase margin.

1.2 Proposed Two Stage Op-Amp

Here, another two-stage single-ended differential amplifier with FinFET innovation is presented. The past circuit executed with MOSFET is supplanted by FinFET transistors [10]. Fig -6 demonstrates the general structure of the amplifier utilized for planning.

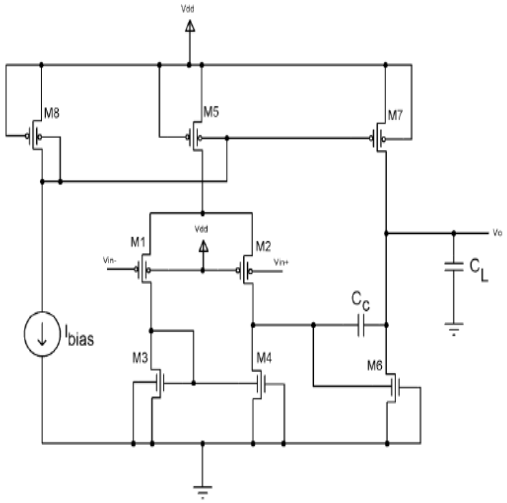


Fig -6: Proposed Two-Stage FinFET Op-Amp

All transistors are FinFET and as appeared in the figure the second gate of every n-FinFET transistors are associated with GND and the back door of p-FinFET transistors is associated with Vdd. Here M1, M2, M3, M4 and M5 frame the main phase of amplifier. M1 and M2 is differential pair and M3 and M4 are utilized as the load for the differential combine transistors. M6 and M7 together assume the job of common source and frame the second phase of amplifier. M5 assumes the job of current source to the amplifier. M8 together with Ibias assumes the job of bias circuit for the amplifier. Cc is utilized for Miller pay in the amplifier structure.

The amplifier open loop gain can be communicated as the increase of two phases:

$$Av=(2*gm2*gm6)\ (I5*I6*(\boldsymbol{\lambda 2}+\boldsymbol{\lambda}\ 3)*(\boldsymbol{\lambda}\ 6+\boldsymbol{\lambda}\ 7)) \quad (1)$$

Along these lines, the gain depends to transconductance gm and the channel length modulation parameter λ. FinFET compelling portability is higher than mass transistors due to non-doping channels and subsequently builds gm. Channel length modulation parameter (λ) in FinFET is impressively limited because of better control of short channel impacts in double gate structure. Thus, the gain can be expanded by FinFET.

6. PRIORITY ENCODER

A priority encoder is one of the types of encoders in which an ordering is imposed to the inputs that means compared with the standard encoder, it includes the priority function. However, this priority is based on the relative magnitudes of the inputs. Hence, the input with larger magnitude is the one that is encoded first. Priority encoders can select the inputs with highest priority in many practical applications. This process of selection is called arbitration. One of the most common examples of arbitration is that, there is numerous input devices in computer system and several of which devices attempt to supply the data to the computer simultaneously. In those cases, a priority encoder enables the input device having the highest priority among those devices trying to access the computer at the same time.

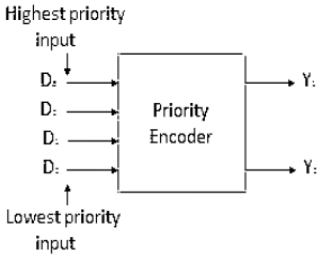


Fig -7: Block Diagram of 4:2 Priority Encoders

6.1 8:3 Priority Encoder Using Logic Gates

The truth table of a thermometer – to – binary priority encoder is shown below. This type of encoder has 8 inputs and three outputs that generate corresponding binary code. A priority is assigned to each input so that when two or more inputs are 1 at a time, the input with highest priority is represented in the output.

Table -1: Truth Table of Priority Encoder

Inputs								Outputs		
T0	T1	T2	T3	T4	T5	T6	T7	O1	O2	O3
1	0	0	0	0	0	0	0	0	0	0
X	1	0	0	0	0	0	0	0	0	1
X	X	1	0	0	0	0	0	0	1	0
X	X	X	1	0	0	0	0	0	1	1
X	X	X	X	1	0	0	0	1	0	0
X	X	X	X	X	1	0	0	1	0	1
X	X	X	X	X	X	1	0	1	1	0
X	X	X	X	X	X	X	1	1	1	1

Suppose if the input lines T2, T4 and T7 are logic 1 simultaneously irrespective of the other inputs, only T7 will be encoded and the output will be 111. Similarly, if T3 = 1, the state of T2, T1 and T0 is irrelevant or don't care and the output is equal to 011.

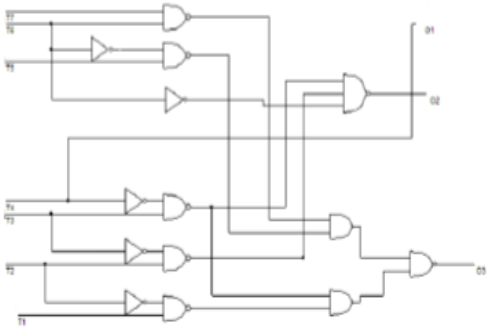


Fig -8: Priority Encoder using Logic Gates

6.2 8:3 Priority Encoder Using MUX

MUX based encoders operate at high speed and covers the small chip area compared to the dynamic logic encoding technique. This encoder is implemented by grouping the results of smaller length MUX based encoder to develop a high bit resolution encoder to convert thermometer code into binary output. It gives better result than previous encoders in terms of power consumption, speed and space.

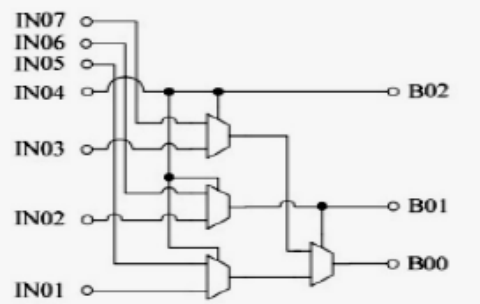


Fig -9: Priority Encoder using MUX

6.3 8:3 Priority Encoder Using TG

We have designed our proposed encoder using four 2:1 multiplexers. These MUXs are implemented by transmission gates. The block diagram of the proposed encoder is illustrated by the given Fig -10. We have designed a 2:1 MUX using two transmission gates(TG).This design requires less number of transistor compared to others as well as less average power consumption. A 2:1 MUX using TG is shown below.

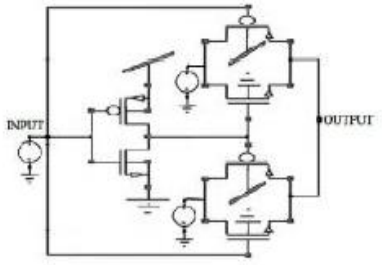


Fig -10: Circuit of a 2:1 MUX using TG

Our proposed architecture is shown in below.

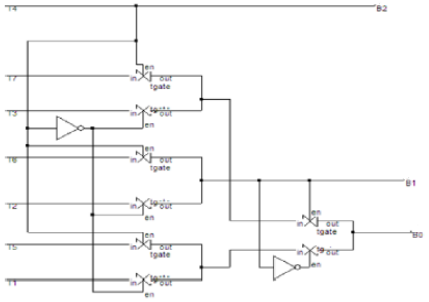
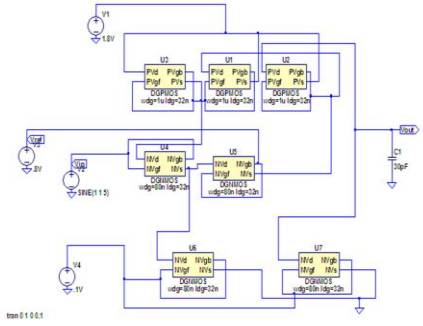


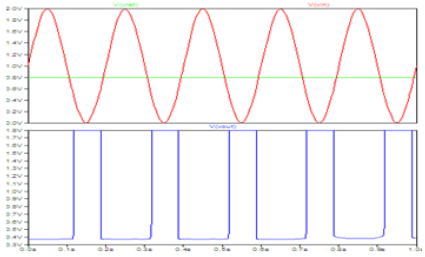
Fig -11: Priority Encoder using TG

7. RESULTS AND SIMULATION

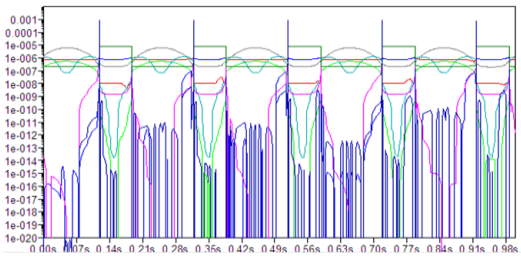
7.1 Schematic of Two Stage FinFET Op-Amp



7.2 Transient Analysis of Two Stage FinFET Op-Amp



7.3 Power Analysis of Two Stage FinFET Op-Amp



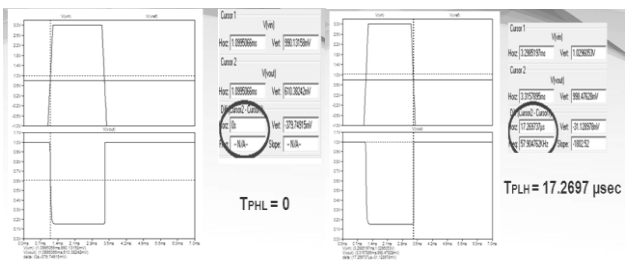
Fclk = 1/T = 1/0.3 sec = 3.33 Hz

Dynamic Power Dissipation = Fclk * Vdd² * CL

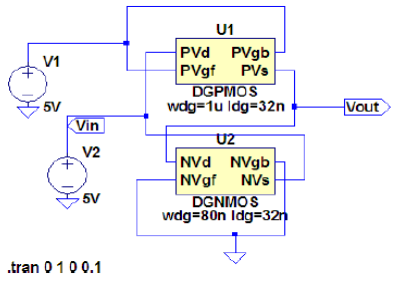
= 3.33 * 0.8² * 30pF = 0.6393 pW

Static Power Dissipation = 0.268 µW

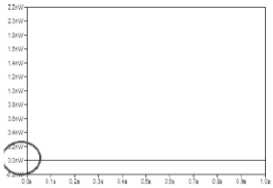
7.4 Propagation Delay of Two Stage FinFET Op-Amp



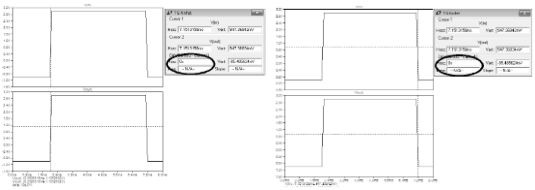
7.5 Analysis of FinFET Transmission Gate



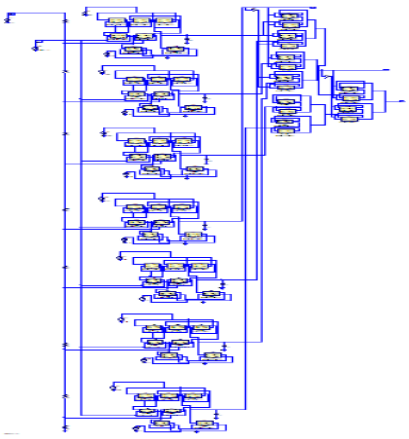
7.6 Power Dissipation of FinFET TG



7.7 Propagation Delay of FinFET TG



7.8 Schematic of FinFET Based 3-bit Flash ADC



7.9 Transient Analysis of 3-bit Flash ADC

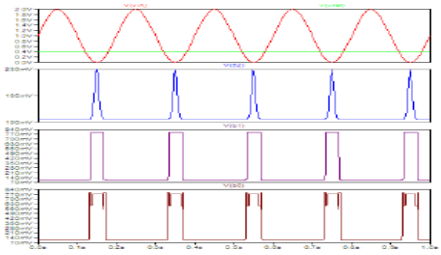


Table -2: Comparison between 3-Bit Flash ADC using CMOS and FinFET Technology

Parameter	CMOS 3-Bit Flash ADC	FinFET 3-Bit Flash ADC
Technology	180nm	32nm
Vdd	1.8 V	0.8 V
CL	100 pF	30 pF
Static Power Dissipation	8.3664 µW	1.876 µW
Dynamic Power Dissipation	7.56 nW	4.4751 pW
Propagation Delay	TPHL = 1.652 ns TPLH = 0.201 ns	TPHL = 0 TPLH = 0.1208 ns

8. CONCLUSION

The requirement of low power circuits for communication applications is increasing as a result of rapid improvement in systems requiring system on chips (SoC) such as wireless handheld devices like tablet PC, smart Phones and Satellite Phones. The flash ADCs are highly advantageous in this regards. However, the conventional CMOS based flash ADCs are restricted by area requirements and operation delay. The communication bandwidths that are used currently for SoC applications require low power ADCs with programmable reference voltage for analog to digital conversion. The speed of a Flash ADC depends on the speed of the comparators. FinFET based comparators and priority encoders proved to be of low power dissipation and propagation delay than MOSFET based comparators and priority encoders. So in order to use a high speed and low power flash ADC, it is better to implement it using FinFET technology.

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