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Glitch Reduction in Combinational Logic Circuits By Using NAND Gates

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Abstract - *The Combinational circuit which we designed was NAND-based digitally controlled delay-lines (DCDL) present a glitching problem which may limit their employ in many applications. This paper presents a glitch-free NAND-based DCDL which overcame this limitation by opening the employ of NAND-based DCDLs in a wide range of applications. The proposed NAND-based DCDL maintains the same resolution and minimum delay of previously proposed NAND-based DCDL. The theoretical demonstration of the glitch-free operation of proposed DCDL is also derived in the paper. Following this analysis, three driving circuits for the delay control-bits are also proposed. Proposed DCDLs have been designed in a 90-nm CMOS technology and compared, in this technology, to the state-of-the-art. Simulation results show that novel circuits result in the lowest resolution, with a little worsening of the minimum delay with respect to the previously proposed DCDL with the lowest delay. Simulations also confirm the correctness of developed glitching model and sizing strategy. As example application, proposed DCDL is used to realize an All-digital spread-spectrum clock generator (SSCG). The employ of proposed DCDL in this circuit allows to reduce the peak-to-peak absolute output jitter of more than the 40% with respect to a SSCG using three-state inverter based DCDLs*

Key Words: *All-digital delay-locked loop (ADDLL), all-digital phase-locked loop (ADPLL), delay-line, digitally controlled oscillator (DCO), flip-flops, sense amplifier, spread-spectrum clock generator (SSCG)*.

1. INTRODUCTION

In recent deep-sub micrometer CMOS processes, time-domain resolution of a digital signal is becoming higher than voltage resolution of analog signals. This claim is nowadays pushing toward a new circuit design paradigm in which the traditional analog signal processing is expected to be progressively substituted by the processing of times in the digital domain. Within this novel paradigm, digitally controlled delay lines (DCDL) should play the role of digital-to- analog converters in traditional, analog -intensive, circuits. From a more practical point of view, nowadays, DCDLs are a key block in a number of applications, like all-digital PLL (ADPLL), all-digital DLL (ADDLL), all- dig-ital spread - spectrum clock generators (SSCGs), and ultra-wide band (UWB) receivers with ranging feature.

a delay-cells chain and a MUX to select the desired cell output. In this mux- based DCDLs, the MUX delay in-creases with the increase of the number of cells. This results in a tradeoff between the delay range and minimum delay (t_{min}) of the DCDL. It is worth to note that t_{min} is a critical design parameter in much application. As an example in ADPLL/ADDLL, t_{min} determines the maximum output frequency of the circuit.

This property remains true also for the All- digital SSCG of where a correct DCDL synchronization is obtained only by imposing that t_{min} is lower than one half input clock period. The large t_{min} of MUX-based DCDLs can be reduced by using a tree-based multiplexer topology. This however results in an irregular structure which complicates layout design and, consequently, also increases the nonlinearity of the DCDL.

1.1 Glitches /Hazards

Hazards/glitches: Undesired output switching

Occurs when different pathways have different delays
Wastes power; causes circuit noise
Dangerous if logic makes a decision while output is unstable

Solutions

Difficult when logic is multilevel
Design hazard-free circuits

1.2 Types of Hazards

Static 0 –hazard

Output should stay logic 0
Gate delays cause brief glitch to logic 1

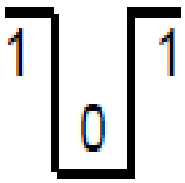

Fig -1: static 0- hazard

Static 1-hazard

Output should stay logic 0
Gate delays cause brief glitch to logic 1

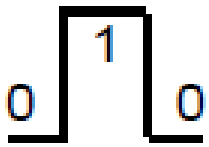

Fig -2: static 1 hazard

1.3 Eliminating Static Hazards

In 2-level logic circuits
Assuming single-bit changes.
Glitches happen when a changing input spans separate k map
Implicants used in the gate realization.
Example:
1101 to 0101 change can cause a static-1 glitch

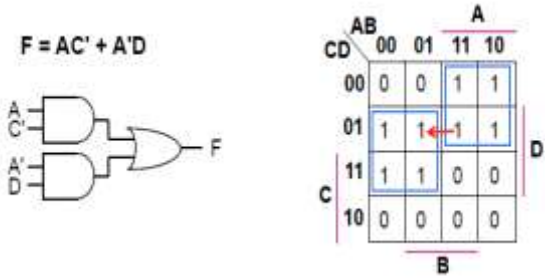

Fig- 3: Eliminating static hazard

1.4 Dynamic hazards

Output should toggle cleanly.
Gate delays cause multiple transitions.

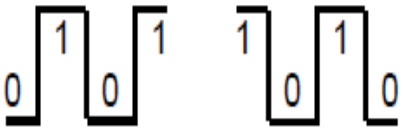

Fig- 4: Dynamic Hazards

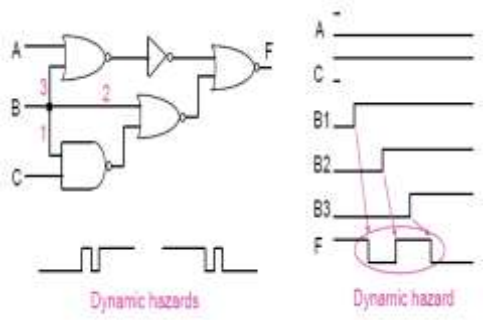

Fig- 5: Dynamic Hazards

2. EXISTING SYTEM

In the existing design DCDLs have been designed in a 90-nm CMOS technology, to the state-of-the-art. Simulation results show that novel circuits result in the lowest resolution, with a little worsening of the minimum delay with respect to the previously proposed DCDL with the lowest delay. We verify the logic in Simulations itself which tells the correctness of developed glitching model as shown in fig 3.1a and sizing strategy. As example application, existing DCDL is used to realize an All-digital spread-spectrum clock generator (SSCG). The employ of existing DCDL in this circuit allows to reduce the peak-to-peak absolute output jitter of more than the 40% with respect to a SSCG using three-state inverter based DCDLs.

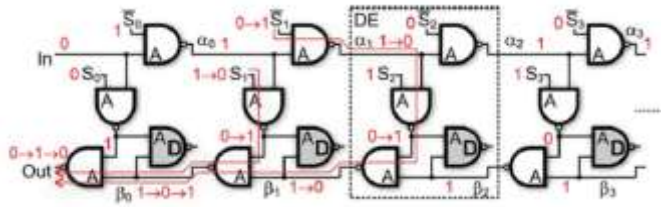

Fig- 6: Glitch present in NAND Control code increased by1

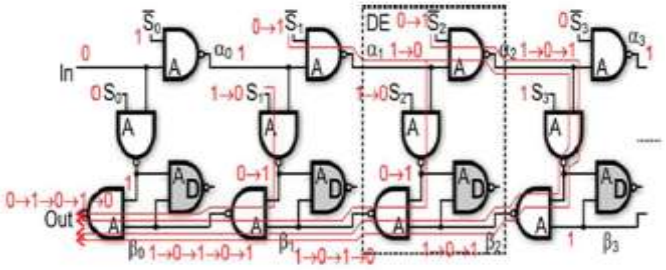

Fig-7: Glitch present in NAND Control code increased by2

The control signal S_i and T_i . control signal 01 means the delay element should go pass state ,11 means the delay element should go turn state,10 means the delay element should go to post turn are

Table -1: control codes

S_i	T_i	DE state
0	1	Pass
1	1	Turn
1	0	Post Turn

A first weakness is due to the different delays of the inverter and the multiplexer which results in a mismatch between odd and even control-codes. This mismatch results in an increased INL.

A second drawback is due to the large multiplexer delay, which provides a resolution higher than the resolution of both NAND based DCDLs and TINV-based DCDLs.

2.1 FLASH MEMORY NOR VS NAND

Introduction

Two main technologies dominate the non-volatile flash memory market today: NOR and NAND. NOR flash was first introduced by Intel in 1988, revolutionizing a market that was then dominated by EPROM and EEPROM devices. NAND flash architecture was introduced by Toshiba in1989. Most hardware engineers are not familiar with the differences between these two technologies. In fact, they usually refer to NOR architecture as "flash", unaware of NAND flash technology and its many benefits over NOR. This is mainly due to the fact that most flash devices are used to store and run code (usually small), for which NOR flash is the default choice.

The Major Differences Table 2 highlights the major differences between NOR and NAND. It shows why NAND and NAND-based solutions are ideal for high capacity data storage, while NOR is best used for code storage and execution, usually in small capacities.

This table can also be used as a quick reference guide to compare NAND, NOR and Disk on Chip, since it addresses the main issues that need to be considered when choosing a flash-based storage solution.

2.2 NAND Vs NOR

The Major Differences Highlights the major differences between NOR and NAND. It shows why NAND and NAND-based solutions are ideal for high capacity data storage, while NOR is best used for code storage and execution, usually in small capacities

Table2 –NAND Vs NOR

PARTICULARS	NAND	NOR
Capacity	8MB-1024MB	1MB-16MB
Performance	Fast Erase (3msec) Fast write Fast read	Very Slow erase (5 sec) Slow write Fast read
Erase Cycles	100,000 – 1,000,000	10,000 – 100,000
Life span	At least as high as NAND. Usually much better thanks to True FFS.	Less than 10% the life span of NAND.
Interface	SRAM-like	Full memory interface

3.PROPOSED SYSTEM

3.1 BLOCK DIAGRAM OF GLITCH FREE CIRCUIT

A digital delay line is a discrete element in digital filter theory, which allows a signal to be delayed by a number of samples. If the delay is an integer multiple of samples digital delay lines are often implemented as circular buffers. This means that integer delays can be computed very efficiently. AND based DCDL as shown in block diagram.

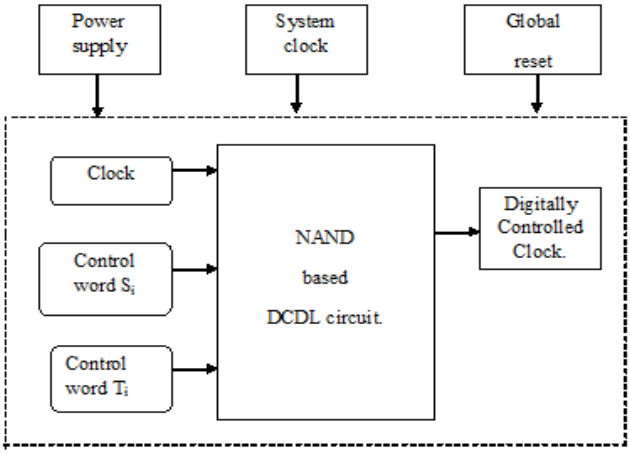

Fig -8: Block Diagram Of Glitch Free Circuit

3.2 GLITCH FREE NAND CIRCUIT

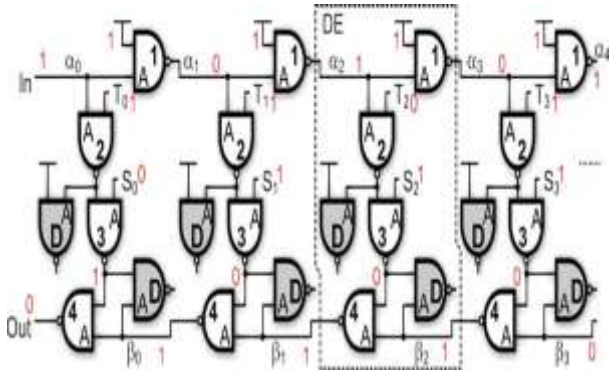

Fig -9: Proposed glitch-free NAND-based DCDL (inverting topology).

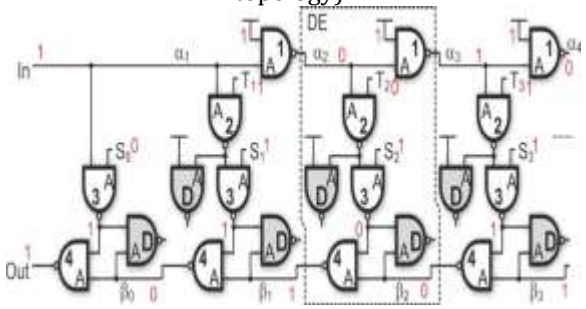

Fig -10: Proposed glitch-free NAND-based DCDL (non inverting topology).

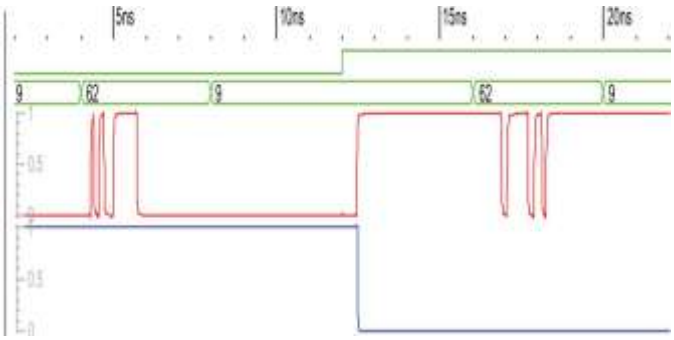

Fig -11: Glitching Problems of the NAND-Based DCDL

4. RESULTS

The glitch free NAND based digitally controlled delay line is proposed here. In this project first am designed one digitally controlled delay line (DCDL) using NAND gates, after that I verified the three stats in the DCDL namely pass state, turn sate and post turn state. Finally am designed 64 DCDL and this provides two 64 bit control word for change the frequency of output clock.

GLITCH PRESENT

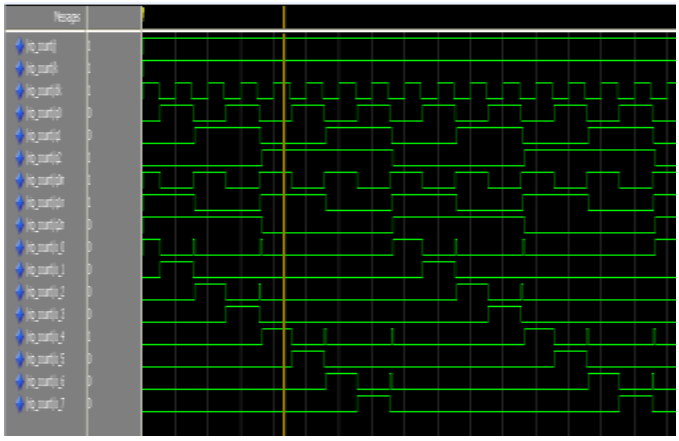

Fig -12: Glitch Present

GLITCH FREE

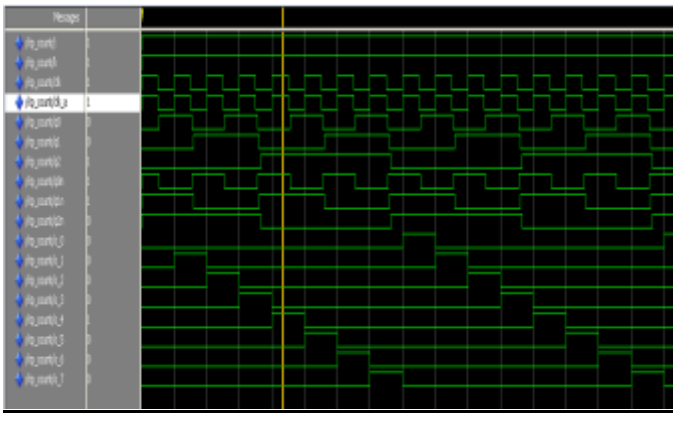

Fig -13: Glitch free

5. CONCLUSION

The simulation results confirm the correctness of developed model and show that proposed solutions improve the resolution with respect to previous approaches. As example application proposed DCDL is used to realize an all-digital SSCG. The employ of proposed DCDL in this circuit allowed to reduce the peak-to-peak absolute output jitter of more than the 60% with respect to an SSCG using three-state inverter-based DCDLs.

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