International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395-0056
Volume: 05 Issue: 09 | Sep 2018 www.irjet.net p-ISSN: 2395-0072

Analysis of BJT with respect to JFET Biasing

Md Zubair Khan[1], Syed Mustafa[2], Noor Ul Abedin[3], Dr. Syeda Gauhar Fatima[4]

[1,2]Undergraduate B.E (E.C.E) Student, Deccan College of Engineering and Technology - Hyderabad
[3] Postgraduate M.E (E.C.E – D.S.E) Student, University College of Engineering (A), O.U - Hyderabad
[4] Professor, Dept of E.C.E, Deccan College of Engineering and Technology - Hyderabad

---***---

Abstract – *As transistor is the major element for amplification. Well aware the common two types of transistor are BJT and JFET, used in analog electronics extending upto working as a switch in digital electronics. In this work the obtained output voltage of JFET when biased is analyzed, keeping in same analyzing a BJT with the same operating conditions. Giving significance to appropriate portions of BJT and JFET respectively.*

Key Words: Biasing, NPN BJT Transistor, N-Channel JFET, Multisim.

1. INTRODUCTION

In this work, a lucid but fundamental approach is considered and analysed with respect to both the mathematical and CAD approach.

This approach being of analog transistors basics, which is a fundamental platform for digital, the biasing fundamentals are being considered and the BJT is been analysed with the biasing technique of a JFET. Here trying to illustrate that a BJT can be biased on the basis of JFET biasing.

Preferring a NPN BJT transistor and N-Channel JFET for the analysis.

1.1 Biasing Transistor (NPN BJT)

The fundamental biasing of the BJT involves the following major implementation:

1. Emitter – Base (EB) should be Forward Biased.
2. Base – Collector (BC) should be Reverse Biased.

Here we are considering a NPN BJT transistor.

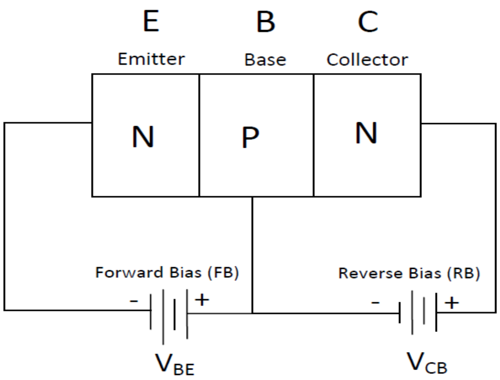

Fig -1.1: Biasing of an NPN BJT Transistor

1.2 Biasing Transistor (N-CHANNEL JFET)

The fundamental biasing of the JFET involves the biasing with the voltage across Gate – Source (V_{GS}) Reversed Biased.

Here we are considering an N-Channel JFET transistor.

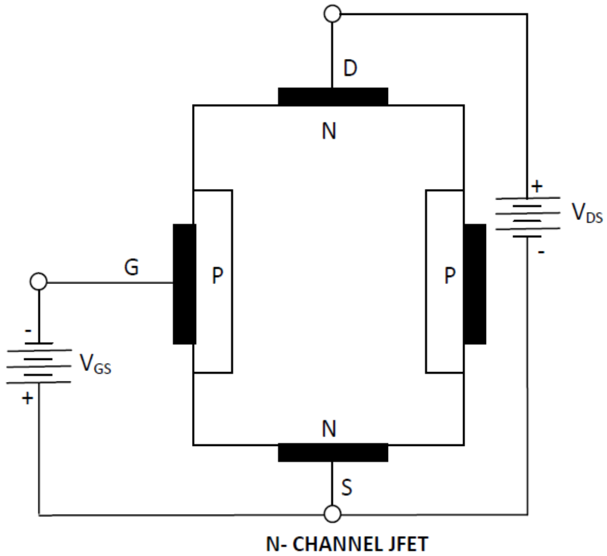

Fig -1.2.1 : Biasing of an N-Channel JFET Transistor

Representing the N Channel JFET blocks/portions on comparison to NPN BJT transistor.

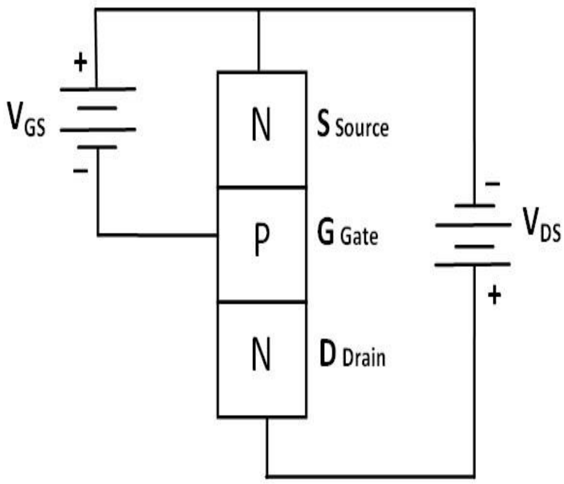

Fig -1.2.2 : Biasing Block Diagram of an N-Channel JFET Transistor

2. THEORETICAL IMPLEMENTATION

2.1 Bias Analysis of JFET (N-Channel):

Biasing the N-Channel JFET Transistor as shown in the circuit.

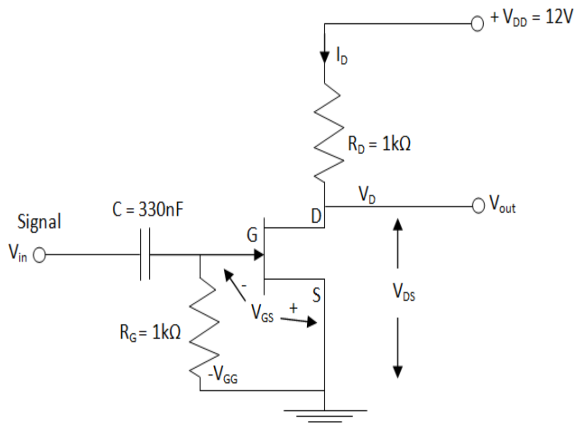

Fig -2.1: Biasing Circuit of an N-Channel JFET Transistor

The gate is always negative with respect to source and no current flows through resistor R_G and gate terminal, that is $I_G = 0$.

Therefore $V_G = I_G R_G = V_G = 0$ (Since I_G=0)

Therefore V_{GS} is equal to the applied voltage, that is V_{GG}.

The gate-source voltage V_{GS} is given as,

$$V_{GS} = -V_G - V_S = -V_{GG} - 0 = -V_{GG}$$

The current then causes a drop in voltage across the drain resistor R_D and is given as,

$$V_{RD} = I_D R_D$$

and output voltage, $V_{out} = V_{DD} - I_D R_D$

Implementing the biasing with the following values:

1. V_{DD} = 12V
2. R_G = 1kΩ
3. R_D = 1kΩ
4. C = 330nF

Substituting the above in the biasing equations, we obtain the output voltage,

i.e. by using,

$V_{out} = V_{DD} - V_{RD}$

$V_{out} = V_{DD} - I_D R_D$ (Since $V_{RD} = I_D R_D$)

By considering the drain current I_D = 1.852 mA, (obtained using Multisim) we get,

$V_{out} = (12) - (1.852\times10^{-3})\ (1000) = 10.148V$

The output voltage obtained is $V_{out} = 10.148V \approx 10V$.

2.2 Analysis of BJT (NPN) using JFET Biasing:

Now, here biasing the NPN BJT transistor with the fundamental biasing topology of the N-Channel JFET as shown in the circuit.

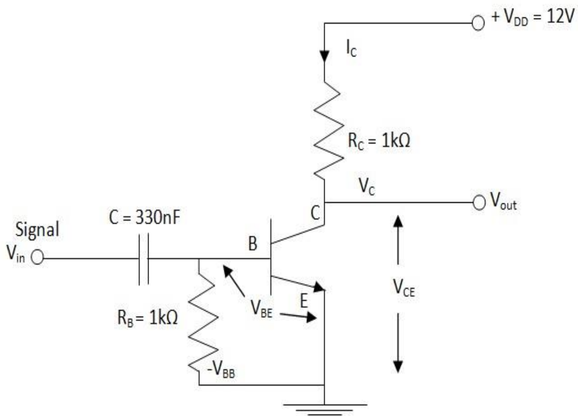

Fig -2.2: Biasing Circuit of an NPN BJT Transistor using JFET Biasing

The Base-Emitter voltage V_{BE} is given as,

$$V_{BE} = -V_B - V_E = -V_{BB} - 0 = -V_{BB}$$

The current then causes a drop in voltage across the collector resistor R_C and is given as

$$V_{RC} = I_C R_C$$

and output voltage, $V_{out} = V_{DD} - I_C R_C$

Implementing the biasing with the following values:

1. V_{DD} = 12V
2. R_B = 1kΩ
3. R_C = 1kΩ
4. C = 330nF

Substituting the above in the biasing equations, we obtain the output voltage,

i.e. by using,

$V_{out} = V_{DD} - V_{RC}$

$V_{out} = V_{DD} - I_C R_C$ (Since $V_{RC} = I_C R_C$)

By considering the collector current I_C = 1.854 mA, (obtained using Multisim) we get,

$V_{out} = (12) - (1.854\times10^{-3})\ (1000) = 10.146V$

The output voltage obtained is $V_{out} = 10.146V \approx 10V$.

3. IMPLEMENTATION ON MULTISIM

The analysis is finally illustrated and the output is obtained using the Multisim CAD tool.

The following circuit illustrations are been done:

1. Analysis of N-Channel JFET

2. Analysis of NPN BJT Transistor

3.1 Analysis of N-Channel JFET:

Using the Multisim CAD tool we have used the following electronic components,

1. N Channel JFET (BC 264B)
2. $R_1 = R_G = 1k\Omega$
3. $R_2 = R_D = 1k\Omega$
4. $C = C_1 = 330nF$

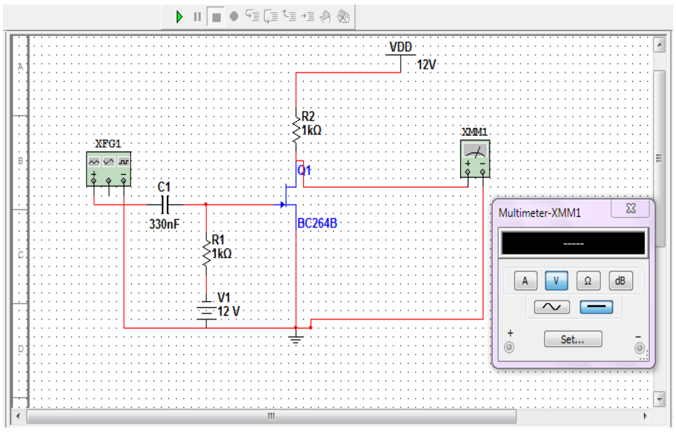

Fig -3.1.1: Initial Bias Circuit of an N-Channel JFET Transistor

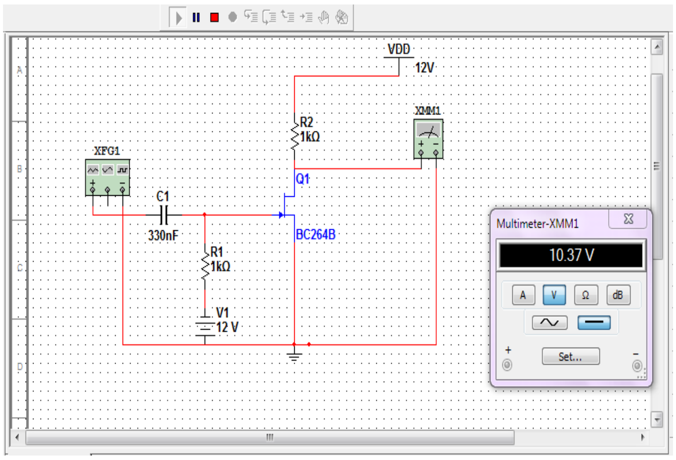

Fig -3.1.2: Output Voltage of an N-Channel JFET Transistor

As seen from the above analysis, the output Voltage i.e. $V_{out} = 10.37\ V \approx 10V$ is obtained.

Now implementing the same biasing technique considering an NPN BJT transistor.

3.2 Analysis of NPN BJT Transistor:

Using the Multisim CAD tool we have used the following electronic components,

1. NPN BJT Transistor (BC 547BP)
2. $R_1 = R_B = 1k\Omega$
3. $R_2 = R_C = 1k\Omega$
4. $C = C_1 = 330nF$

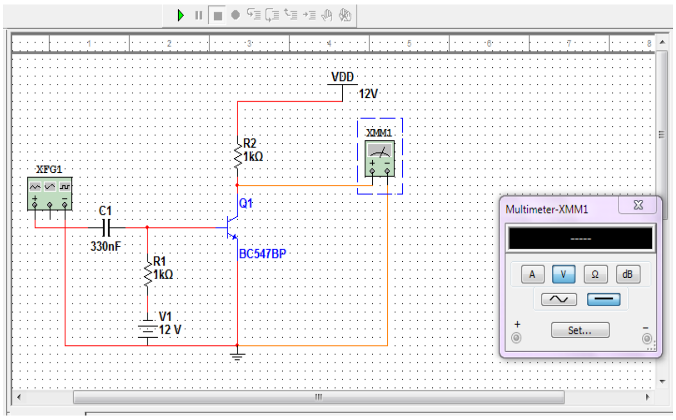

Fig -3.2.1: Initial Bias Circuit of an NPN BJT Transistor

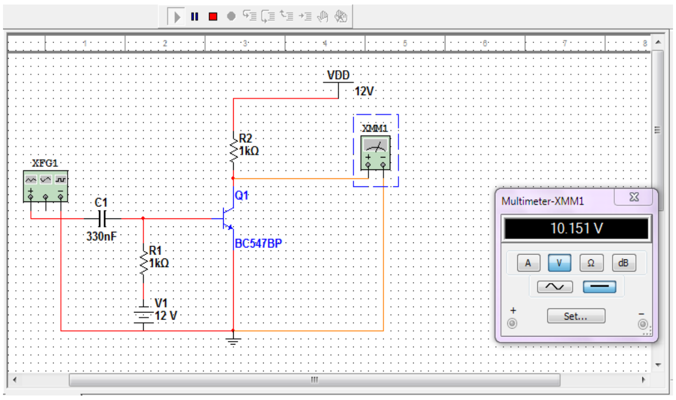

Fig -3.2.2: Output Voltage of an NPN BJT Transistor

As seen from the above analysis, the output Voltage i.e. $V_{out} = 10.151\ V \approx 10V$ is obtained.

4. CONCLUSION

The analysis are been done on the basis of N-Channel JFET transistor biasing technique. The same fundamental approach has been implemented on a NPN BJT transistor, with the help of Multisim CAD tool. The analysis has obtained similar output voltages (V_{out}). Therefore as per the analysis, a NPN BJT can be biased using a N-Channel JFET biasing topology.

International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395-0056
Volume: 05 Issue: 09 | Sep 2018 www.irjet.net p-ISSN: 2395-0072

5. Future Scope

The analysis can be a futuristic scope for JFET biasing as a fundamental tool for transistors biasing with focus of giving mandatory importance to its implementation and use in digital and analog electronics.

6. References

[1]. Electronic Devices and Circuits by S Salivahanan and N Suresh Kumar

[2]. Electronic Devices and Circuits by J B Gupta

[3]. Electronic Devices and Circuits by Jacob Millman

[4]. Integrated Electronics by Jacob Milliman, Chrisitos C. Halkias and Chetan D Parikh

[5]. Electronic Devices and Circuits by P. John Paul

[6]. Principles of Transistor Circuits by S W Amos and Mike James

[7]. Electronic Circuits – Discrete and Integrated by Donald L Schilling and Charles Belove

[8]. Principles of Electronics by V. K. Mehta

[9]. Transistor Circuit Techniques - Discrete and Integrated by G.J. Ritchie

[10]. Encyclopedia of Electronic Components Volume 1 by Charles Platt

[11]. Easy Electronics by Charles Platt

[12]. Electronics from the Ground Up : Learn by Hacking, Designing, and Inventing by Ronald Quan

[13]. Analysis and Design of Analog Integrated Circuits by Paul R Gray and Robert G. Meyer

[14]. Understanding Modern Transistors and Diodes by David L. Pulfrey

[15]. Field Effect Devices by Robert F. Pierret

[16]. Electronic Principles by Albert Paul Malvinos

[17]. Electronic Devices and Circuit Theory by Louis Nashelsky and Robert Boylestad

[18]. Electronics, Principles and Applications by Charles A Schuler

[19]. Operational Amplifiers and Linear Integrated Circuits : Theory and Application by James M. Fiore

[20]. Grob Basic Electronics Textbook by Bernard Grob

[21]. Grob's Basic Electronics Textbook by Mitchel E. Schultz

AUTHORS

Mr. Md Zubair Khan is a B.E Final year undergraduate student of Deccan College of Engineering and Technology from E.C.E stream.

Mr. Syed Mustafa is a B.E Final year undergraduate student of Deccan College of Engineering and Technology from E.C.E stream.

Mr. Noor Ul Abedin is a postgraduate student of University College of Engineering (A), Osmania University in E.C.E with specialization in Digital Systems Engineering (D.S.E). He has worked as an Assistant Professor, Dept. of E.C.E, Deccan College of Engineering and Technology. His fields of interest are Analog and Digital Electronics. He has lectured and thought various engineering subjects which include Anlaog Electronic Devices & Circuits, VLSI Design, Networks & Circuits, Antennas & Wave Propagation, Electronic Instrumentation, Automation in Process Control, Power Electronics, Digital Electronics & Logic Design and Linear Integrated Circuits.

Prof. Dr. Syeda Gauhar Fatima is working as a Professor in Dept. of E.C.E, Deccan College of Engineering and Technology with a teaching experience of 19 years. She has an esteem academic performance in teaching/lecturing in almost all the aspects of analog and digital electronics and communication subjects. She has 12 publications titled to her name with also being a coordinator to several technical workshops and has guided several UG level major projects.