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Implementation of 64-bit MAC unit with different Adder circuits

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Abstract - *The multiplication and adders constitute most intrinsic logics required in extensively large number of applications involving computation and arithmetic. These units drastically affect the performance parameters of integrated circuits on an SOC i.e. area, frequency of operation and power dissipation in the circuit. The arithmetic units located at the heart of RISC processors also form a basis of the complex computations. Hence, in this paper a MAC unit has been designed and the performance of the design has been analyzed using different addition topologies i.e. ripple carry adder, carry save adder and carry look ahead adder.*

Key Words: ripple adder, carry save adder, carry select adder, carry look ahead adder, array multiplier

1. INTRODUCTION

VLSI Design focusses on implementation of the digital logics requiring minimal area, delay and power consumption leading to high performance of digital integrated circuits.

In computing, MAC (Multiply and Accumulator) unit plays a significant role to calculate the product of two bit streams and thus adding the result to the already existing data into the accumulator unit. Hence the MAC unit comprises of a multiplier, an adder circuit and an accumulator to contain the final result.

The optimization of a MAC unit is very useful as the multiplier unit involves large area consumption on an integrated circuit and the adder unit contributes to extremely large combinational delays in the circuits thus affecting the performance. However if the optimization of a MAC unit is achieved for high end processors such as 64 bit processors, it can help in turn optimizing different processors used in enormous applications such as signal processing, core arithmetic computation etc.

An adder is a combinational logic in MAC unit which is also in turn used in the multiplier unit that drastically affects the performance of the MAC unit. If the MAC unit is designed for the processing of large number of bits like 32 bit or 64 bit then the adders drastically affect the performance of the device.

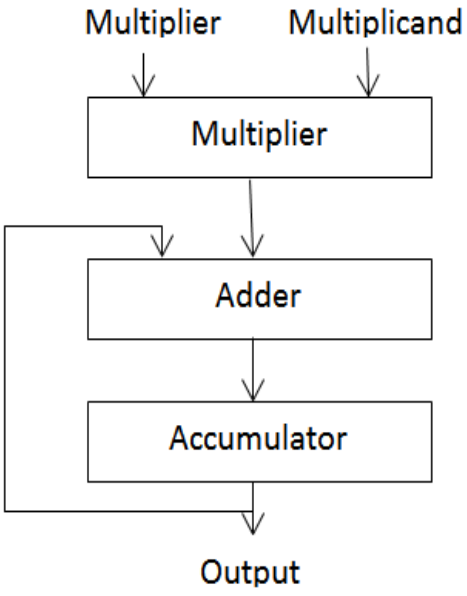

Figure 1: Block Diagram of MAC Unit

2. LITERATURE SURVEY

Extensive research is going ahead in the field as the MAC unit constitutes an integral part of the processors used for arithmetic computation, signal processing etc.

Athira Koranath, et.all, compared different multipliers including booth and Wallace tree multipliers and found that the modified Wallace tree is the best in terms of area and power.

Dr. Kittur, et.all, has implemented the design of MAC unit making use of the algorithm of modified Wallace multiplier. The adder circuit used by the authors is carry save adder. The results computed in the paper signify the operating frequency of MAC unit as 127 MHz. The total power dissipated by the circuit is 177.732 mW. They have used Verilog-HDL for writing the RTL.

R.UMA, Vidya, et.all, in paper, the author studied various types of adders and there comparison on various parameters. They concluded that, the fastest adders for any digital combinational logic are carry select adder and carry save adder. However, they consume larger area in comparison to the ripple carry adder. The topologies for his applications that put a constraint on the area and power dissipation in a circuit need to use any of the adders among ripple carry, carry skip and carry bypass adder. Again they put a constraint on the performance by increasing the delay.

Sumit Vaidya, et.all, in paper talked about comparison of different multipliers on basis of delay and power and found that the most suitable multiplier for different applications is Booth Multiplier. It is extremely useful in terms of different VLSI design parameters such as performance, delay, power consumption and complexity. In addition also consumes less on chip area. Instead Array Multiplier consumes more power. However for certain applications Wallace Tree multiplier is extremely useful if there is a constraint of minimal delay.

Considering the literature survey different papers authors have concluded different results as some of the papers signify the Wallace tree multiplier to be the best multiplier or some of the authors have marked the Booth Multiplier as a best multiplier to be used. But there is the requirement of a generic solution for the choice of the architecture for MAC unit so that it can be used generically for the computation applications of different fields.

2. ADDERS ARCHITECTURES

Different adders that can be used for the design of a MAC unit are ripple carry adder, carry save adder and carry look ahead adder.

Ripple adder is a regular arrangement of single bit adders which is being used traditionally. In the design the carry-output of one stage is connected to the carry-input of the next stage. The design is shown in Figure 2:

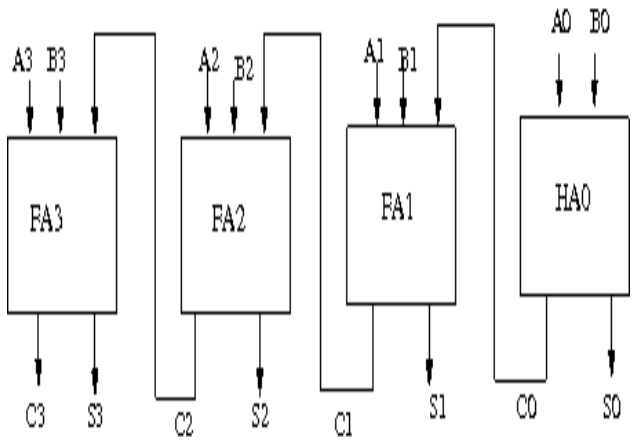

Fig -2 Ripple carry adder

Propagation of the carry generated by the full adder circuits is avoided using the carry save adder logic. The circuit sends the intermediate carries towards the outputs. Like ripple carry adder it does not propagate the carry to the next stage. The carries thus generated are propagated at the end when all the intermediate carries have been generated. Consequently two outputs are obtained one is the sum (S) and another bit vector as carry (C). Therefore total delay imposed by the circuit is equivalent to the delay as that posed by a single full adder circuit. However, it occupies more area in comparison to the ripple carry adder i.e. n times as that occupied by the full adder cell.

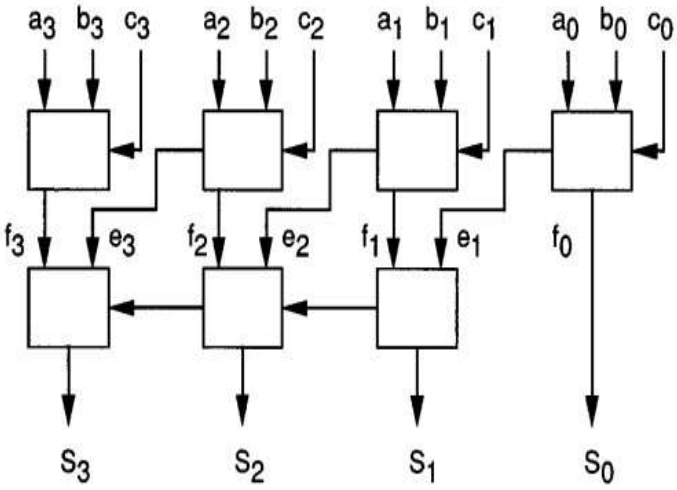

Fig – 3 Carry Save Adder

The carry-look ahead adder follows an entirely different logic for addition by computing group generate signals and group propagate signals. It does not wait for the carry of the previous stage as in case of ripple carry order which helps in optimizing the speed of the circuit. As the carry generated in a circuit stage does not depends on the operands at that instant but at stage i + 1 it is marked by the generation of carry in the previous stage i. Hence it leads to the conclusion that a separate network for carry propagation can be implemented thus reducing the delay to wait for the carry generated at various stages.

The carry-look ahead adder follows a two level logic circuit in which, AND gates are followed by an OR gate. For each carry input c_i on loading of adder inputs in parallel, all generator group terms g_i and propagation group terms p_i are created simultaneously. Henceforth carry for each bit is computed independently in the circuit. In actual, the carry signal c_i is obtained through two-stage logic simultaneously, which results in a constant time complexity in the circuit.

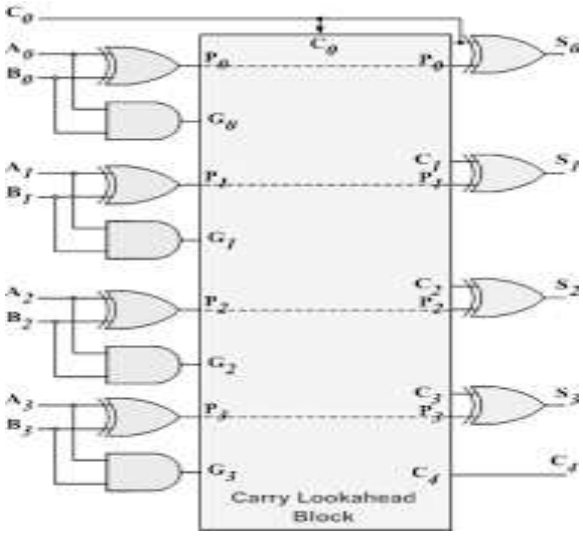

Fig-4 Carry look ahead adder

4. SIMULATION RESULTS

The RTL Design of the adder units is verified using Xilinx ISE Design Suite 14.1 which has been further used to synthesize the RTL written in VHDL and then compare the synthesis reports results for different adders implemented in a MAC unit consisting of array multiplier.

Fig –5a shows the ripple carry adder waveform for 64-bit computation. Fig-5b shows the waveform for 64-bit carry save adder. Fig-5c shows the waveform for 64-bit carry look ahead adder.

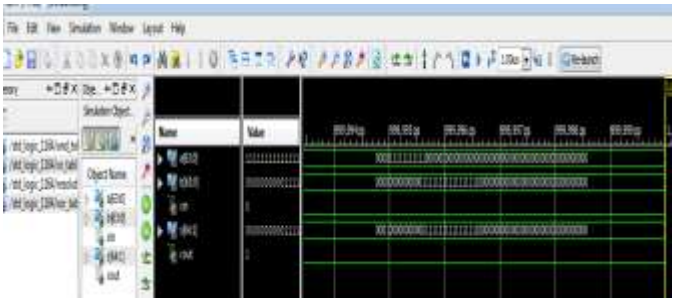

Fig-5a 64-bit ripple carry adder

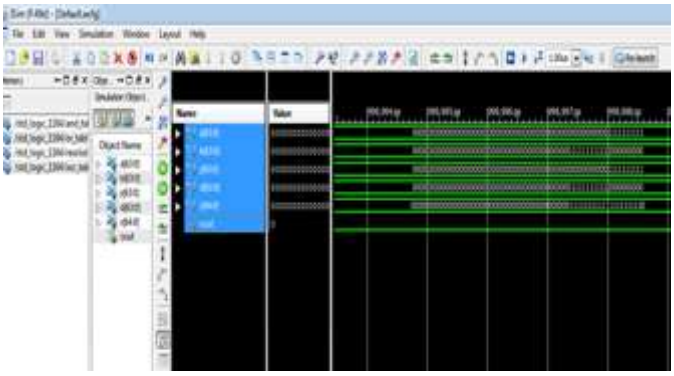

Fig-5b 64-bit carry save adder

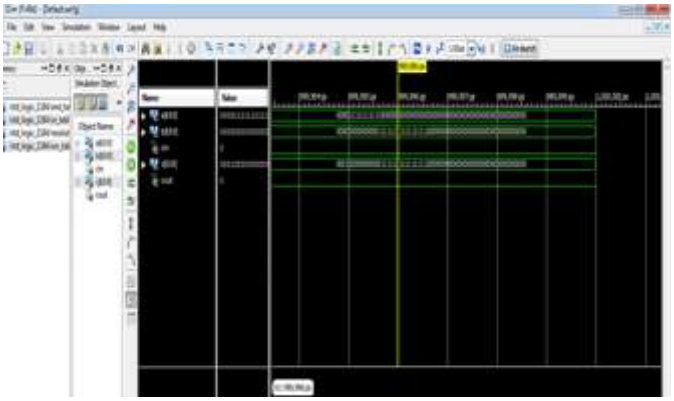

Fig-5c 64-bit carry look ahead adder

Fig-6 shows the simulation result of a 64-bit array multiplier with which the MAC unit has been combined finally for the comparison of different adders.

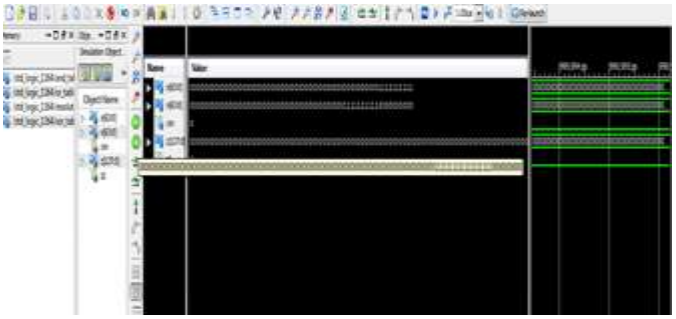

Fig-6 64-bit array multiplier

Fig-7a shows MAC unit comprising of ripple carry adder and array multiplier. In Fig-7b carry save adder has been used and in Fig-7c carry look ahead adder has been used to implement the MAC unit.

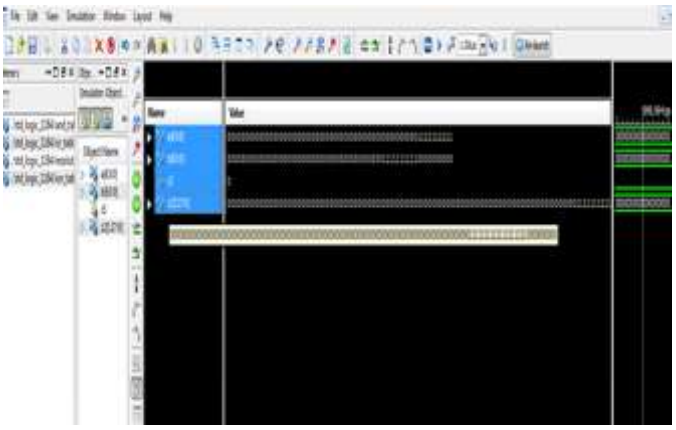

Fig-7a 64-MAC unit using ripple carry adder

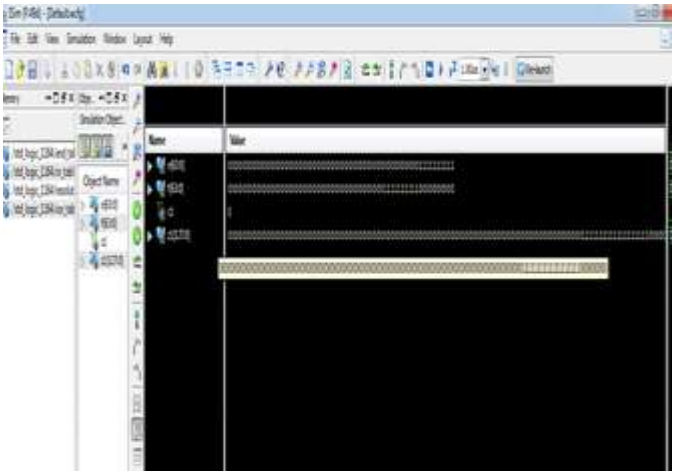

Fig-7b 64-MAC unit using carry save adder

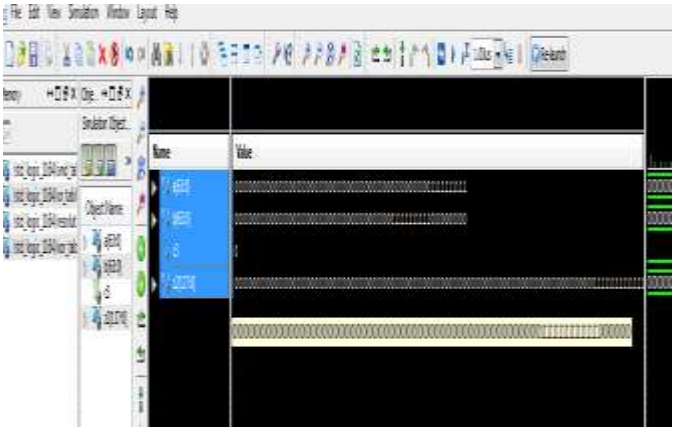

Fig-7c 64-MAC unit using carry look ahead adder

Table 1 shows the synthesis results of different 64-bit adder units.

Table-1: Synthesis report of 64-bit adders

Parameters	Ripple	Carry Save	Carry Look Ahead
No. Of Slices	74	220	96
4 I/Ps Lut's	128	382	127
Bonded I/O	194	322	193
Level Of Logic	66	67	65
Combinational Delay(ns)	42.84	40.383	55.662
Logic Delay(%)	31.6	33.6	39.1
Route Delay(%)	68.4	66.4	69.1
Total Power(W)	0.374	0.236	0.375
QuIscient Power(W)	0.365	0.227	0.366
Destination Port	65	66	65
Total No. Of Paths	4353	29817	4288

Table 2 shows the synthesis result of 64-bit MAC unit constituted of array Multiplier unit and different adder configurations.

Table-2: Synthesis result of 64-bit MAC units with different adders

Parameters	Ripple	Carry Save	Carry Look ahead
No. Of Slices	5318	5349	5318
4 I/Ps Lut's	9284	9355	9284
Bonded I/O	257	257	257
Level Of Logic	2735	2687	2735
Combinational Delay(ns)	1532.50	1530.435	1532.50
Logic Delay(%)	26.1	56.7	25.5
Route Delay(%)	73.9	43.3	74.5
Total Power(W)	0.252	0.168	0.249
Destination Port	128	128	128

5. CONCLUSION

From synthesis results it has been observed that a 64-bit carry save adder is taking maximum area on the chip but its combinational logic delay is less in comparison of carry look ahead adder circuit. Carry save adder is found good in case of less power consumption as compared to the other two adders. However when these topologies of adders are in turn combined with array multiplier for implementing a MAC unit. It consumes the area almost equivalent to that of the other adders. But the routing delay of the circuit is less as compared to the MAC unit combined with the other adders. Power consumption is again an add on advantage in the circuit as it consumes less power i.e. 0.227W as compared to other adders.

Hence, it is concluded that MAC unit implemented using carry save adder is useful for the low power applications but it is not useful for the applications where area on chip is a major constraint.

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