A Literature Survey on Modular Multilevel Converter & Key Challenges

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Abstract: - *This paper presents a review on Modular Multilevel Converter (M²C) which was a popular series of topology and has been applied in industries in recent years. Modular multilevel converter (M²C) is an emerging technology for various applications including HVDC transmission and wind energy conversion systems. Submodule based M²C architecture dominates over other conventional converters topologies, due to various technology, control as well as economic advantages. This paper presents a comprehensive review of different submodules and topologies in M²C. Different types of submodule architectures are discussed to provide an overview of evolving technology. Different submodules are grouped in accordance to their output terminal voltage levels. The key challenges of M²C are also highlighted.*

Key Words: Modular Multilevel Converter, Half Bridge Submodule, Modulation

1. INTRODUCTION

The Modular Multilevel Converter (M²C) (Fig. 1) have been attractive in both industrial applications and academic researches since from its invention in 2001 [1]-[4]. To better understand and utilize the converter, critical features, shortcomings and their solutions of the M²C are surveyed in this paper, which can provide an overview of the current status of the researches on this topology.

The power converter topology of MMI (Modular Multi level Inverter) has been intensively researched, developed, and valuated against many features like high modularity, simple scalability, low expense of filters, robust control, simple in design and redundancy.

This converter is composed by identical power cells connected in series, each one built up with standard components, enabling the connection to high voltage poles. Although the MMI and derived topologies offer several advantages, simultaneously they also introduce a more complex design of the power circuit and control goals, which have been the main reason for the recent and ongoing research.

In this paper, a comprehensive review of M²C topology and its submodule architecture is presented. Different submodules are grouped in accordance to their output terminal voltage levels. Along with the basic operation of M²C -HVDC, the key issues and challenges are also discussed.

This paper is arranged as follows. Section II discusses the basic M2C topology and its operation. Section III is dedicated to several SM architectures proposed over a time. Challenges and key issues have been discussed in brief in Section IV.

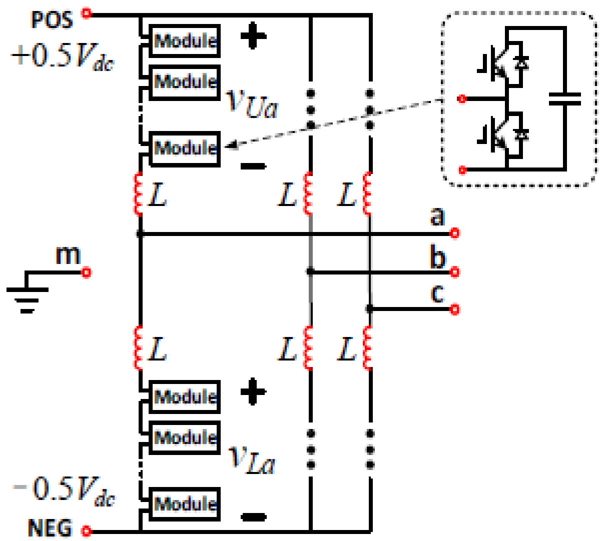

Fig. 1. The schematic of the modular multilevel converter (M²C)

2. MODULAR MULTILEVEL CONVERTER TOPOLOGIES AND MODELING

2.1. Converter and Cell Description

One of the typical configurations of the M²C is the dc to three-phase converter used in HVDC applications, shown in Fig. 2. In this topology two arms form a converter phase, where the dc system is connected to the upper (P) and lower (N) sides of the phase and the three-phase ac system is connected to the middle point of each phase (a, b, c).

The arms connected to the positive bar are usually referred as positive, or upper, arms and the arms connected to the negative bar are referred as negative, or lower, arms.

The ac and dc systems are usually modeled as voltage sources and the lines as inductors. This figure also shows the arm inductance *L* which must be connected in series with each group of cells in order to limit the current due to instantaneous voltage differences of the arms.

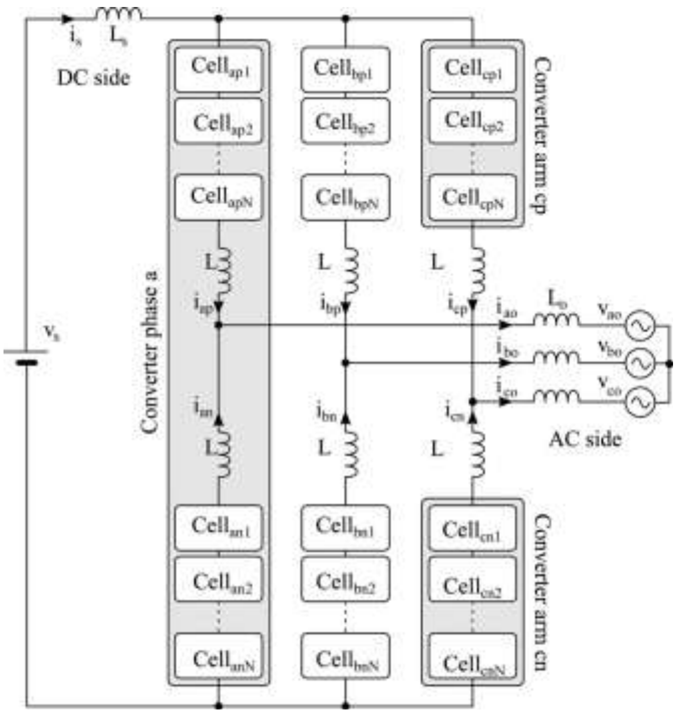

Fig2. DC/Three-phase modular multilevel converter circuit topology

There are several power cell topologies proposed in the literature, the known ones are shown in Fig. 3. The most common cells are the full-bridge and half-bridge, of Fig. 3(a) and (b), respectively. The half-bridge cells can generate only zero and positive voltages, so there is inevitably a dc component in the arm voltage.

This kind of cell thus only is used when the M²C is connected to a dc system. On the other hand, full-bridge cells can generate positive, zero, and negative output voltages, hence, they can be used when the M²C is connected to either ac or dc systems. One of the drawbacks to full-bridge cells is the higher number of components, compared to half-bridge cells.

The unidirectional cell, shown in Fig. 3(c), has been proposed to reduce the number of semiconductors per cell, but the switching states are restricted depending on the current direction [5].

The efficiency of the cells can be improved, replacing the standard cell by multilevel structures, such as neutral point clamped or flying capacitor [6], as shown in Fig. 3(d) and (e), respectively, or by using a twin module [7].

One of the challenges of controlling the M²C is keeping the capacitor voltages balanced. It is possible to modify the power cell connecting an inverter and a resonant circuit, as shown in Fig. 3(f), to balance the capacitor voltages transferring power among cells inductively [8].

Finally, the topology of the cells can be completely modified from a voltage source dc link to a current source dc link, as shown in Fig. 3(g). These power cells have been proposed to achieve a higher voltage and power rating than traditional voltage source cells [9].

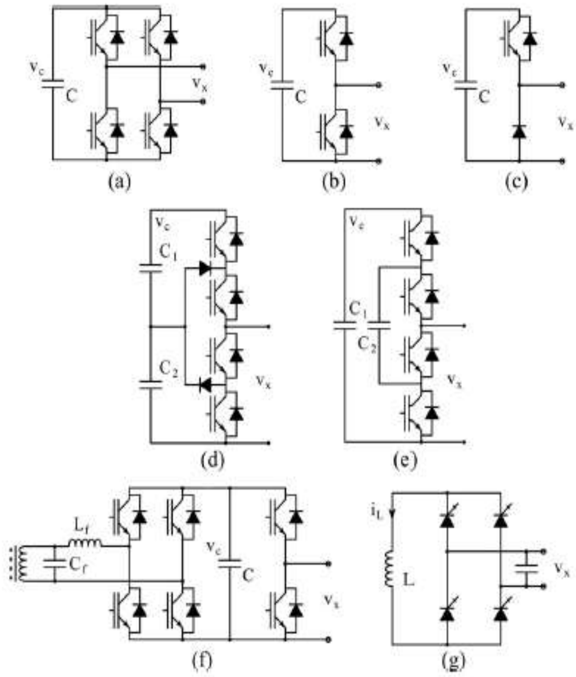

Fig. 3. Power cell topologies. (a) Full-bridge. (b) Half-bridge. (c) Unidirectional cell. (d) Multilevel NPC cell.

(e) Multilevel flying capacitor cell. (f) Cell with resonant inverter for inductive power transfer. (g) Current source cell.

2.2 Converter Modeling and Simulation

The modeling of M²C s could become extremely complex and its simulation could be highly time consuming, due to the large amount of cells. To avoid this problem, several approaches have been proposed in the literature to simplify its model. The simplest one is to consider all the power cells in each arm as a single equivalent voltage source [10], as shown in Fig. 4(a).

This model is very simple to analyze and to simulate, being also possible to obtain independent dynamical models of currents to further simplify the analysis. To further refine the converter model, switching effects and capacitor dynamical behavior can be included, considering the arms as controlled voltage and current sources [11], as shown in Fig. 4(b).

This model provides more accurate results than the previous one, but it requires longer simulation time and the analysis becomes more complex due to coupled dynamics. A matrix representation is usually adopted to simplify the analysis and simulation in both models [12].

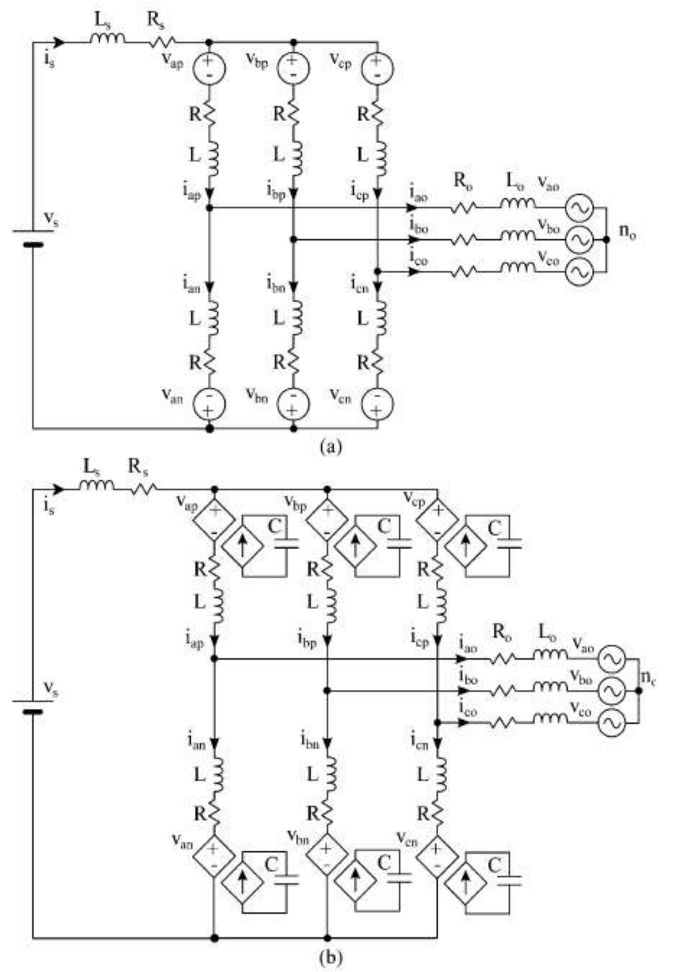

Fig. 4. Models of the M²C. (a) Considering the arms as voltage sources. (b) Considering switching effects and capacitor dynamics.

3. MODULATION APPROACHES OF THE M²C

A. Space-Vector Modulation (SVM)

In paper [13] the SVM was mentioned to be a possible modulation scheme. But in later high voltage applications, the M²C consists of too many modules to be modulated by SVM because of the complex vector calculation and selection, for instance as many as 200 in HVDC application. Therefore, the staircase modulation and PWM modulations are implemented in practical applications.

B. Staircase Modulation

In staircase modulation that renders low switching

Frequencies, the power devices generally switch on and off twice during one cycle of line voltage, to minimize the switching losses in high power applications. Then a staircase waveform will be generated, following a sinusoidal envelope [14]. As long as the staircase pattern is determined, the way to shape the pattern by switching the modules can simply follow the description in [15].

There are two ways to calculate the switching time and level to form a staircase pattern in the staircase modulation, the selective harmonic elimination modulation and nearest level modulation. In [16] the staircase modulation with selective harmonic elimination (SHE) technique is suggested to be used for the M²C modulation shown in Fig5(c) and (d). The switching angles of all steps of the staircase are calculated by solving the harmonic equations with associated modulation index and harmonic elimination requirement. By this approach, lower order harmonics which have relatively high magnitudes can be eliminated, and hence the total harmonic distortion (THD) of the AC voltage of the M²C is reduced. Normally the switching angle tables are pre-calculated and stored in the memory off-line to save the computation resources, but both of the number and scale of the tables will be too large when it comes to hundreds of voltage levels and a wide range of modulation indexes.

It is not realizable to calculation the switching angles for every modulation indexes in advance. The switching tables can only be calculated for several number of modulation indexes, such that the THD may not be optimized for certain operation voltage. Therefore, an on-line switching-angles calculator is proposed for the M²C modulation [17]. In this technique, reducing the THD of the voltage is targeted through the instantaneous comparison between the pure sinusoidal voltage reference and the voltage signal synthesized using Fourier analysis. The error from the comparison is used to update the switching angles in the direction for the error to be eliminated using the least-mean squares method [17]. But this approach is still complicated for large number of voltage levels.

Compared to the SHE technique, the nearest level modulation (NLM) is much simpler and more applicable for the applications with large amount of modules, which simply selects the output voltage level nearest to the reference. To obtain the switching patterns the voltage reference is multiplied by the number of positive voltage levels *n*, then apply the round function to find the required output voltage level [18]. The relationship between the THD and sampling frequency, number of modules and the modulation index value can be found in [19].

C. Pulse Width Modulation (PWM)

Because of the approximation nature of round function used in nearest level modulation, the voltage level selection at each sampling period always contains error. To address this problem, a modulation approach based on the nearest level modulation is proposed to achieve a PWM pattern without carriers [20]. Only one module is operating at PWM mode in each switching cycle and then the average value of the AC voltage will be equal to that of the reference at this switching cycle. This approach reduces the THD at the cost of a little more switching losses, which is quite effective when the module number is relatively low.

Traditional level-shifted and phase-shifted multicarrier based PWM which are widely used in other multilevel converters can be applied as well in the modulation of the M²C shown in Fig 5(a) and (b). In [21], implementation and harmonic comparisons of that PWM modulation have been elaborated in details and all the associated waveforms are given. The phase-shifted PWM turns out to have the lowest THD but the most switching events, namely the highest switching losses.

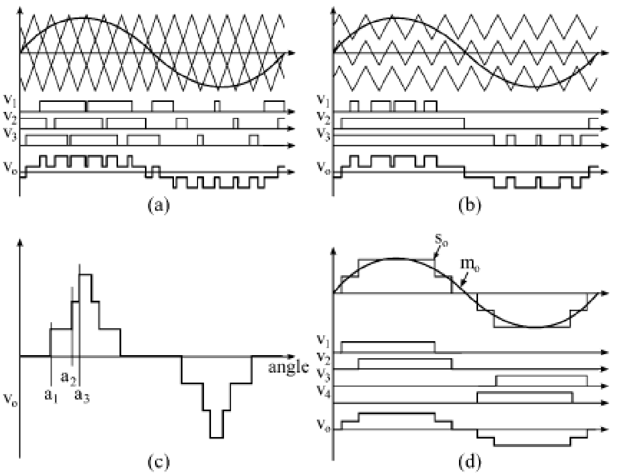

Fig. 5. Modulation techniques. (a) Phase shifted PWM.

(b) Level shifted PWM. (c) Multilevel SHE. (d) Staircase modulation.

4. KEY ISSUES AND CHALLENGES

Besides all the advantages, M²C possess several issues and control challenges that provide an opportunity to researchers for further improvement in existing architecture and control schemes. These challenges include design constrains, control issues, pre-charging of capacitors and startup process, modeling etc. [22], [23], [24], [25], [26].

A. Design Constraints

Primary design constrains are:

- Size of inductor
- Size of capacitor
- Semiconductor losses
- Reliability

Inductor of M²C performs filtering for high-frequency harmonics in arm current and works as limiter for dc-side fault current and so, its dimension is greatly affected by short circuit dc current and arm ripple current. Size of capacitor is a function of voltage ripple and cost. Further, semiconductor power loss is also significant constraint in M²C designing, as M²C structure employs around 200 SMs per arm. Reliability of M²C structure is directly proportional to the redundant SMs. Considering these issues, multiple hybrid structures of M²C as well as of SMs are developed. Unfortunately, most of them sacrifice one or another advantage of M²C like; modularity, efficiency, dc side fault ride through capability, etc.

B. Control Challenges

One of major concern/challenge in M²C control is capacitor voltage balancing. Other control challenges include

- Voltage balancing of SM capacitors
- Control of output current
- Control of circulating current
- Minimizing voltage ripples
- Generating proper reference for input current
- Maintaining dc voltage in accordance with the reference

Although many control schemes have been developed to handle above issues, but the necessity of simultaneous control of all the parameters without sacrificing efficiency is still a major concern.

C. Capacitor pre charging and start up

For fast and smooth start up, the capacitors of M²C require a recharging. For the same, multiple solutions have been proposed but unfortunately, these either require costly dc circuit breakers or complex control schemes or both.

D. Modelling

A practical structure of M²C includes more than 200 SMs per arm. Further, each SMs include multiple semiconductor devices and capacitors. Under such scenario, the analysis of the system becomes difficult as considering all the details would require huge amount of storage memory and becomes as slow process. On the other hand, accelerating the process would sacrifice the amount of details.

5. CONCLUSION

This paper has presented a brief summary of pivot aspects of the M²C as well as other related multilevel converter taking advantage of the feature of the M²C. The M²C is systematically introduced from its modeling, modulation, and control, rendering an overview of the state of-art researches on the converter. In Those topologies related to or derived from the M²C are introduced from their motivation of invention and the most basic features. The intention of authors is to provide a comprehensive understanding of the modular multilevel converters associated with specific applications, and for reader to consider where to go to maximize advantages of the topologies.

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