Design and Simulation of Op-Amp based Comparator for Sigma Delta Modulator

Basaveshwara B R[1], Dr. Kiran A Gupta[2]

[1]M. Tech, VLSI D& ES, Dept. of ECE, Dayananda Sagar College of Engineering. Bangalore, India
[2]Professor, PG Co-ordinator VLSI D & ES, Dayananda Sagar College of Engineering, Bangalore, India

---

Abstract – *This paper explains design and simulation of Op-Amp based Comparator for the analog application in Sigma Delta Modulator. The Op-Amp based comparator designed in this paper has been verified for static and dynamic operations. The comparator is designed for the required specifications of the Sigma Delta ADC. The CMOS design of the circuit has been verified using Cadence IDE simulator for 45nm technology node and* the *layout has been created with DRC and LVS verification. This module has been used in the sigma delta modulator operating on short radio wave frequency of 3.8MHz*

***Key Words*: Sigma Delta Modulator, Op-amp, Cadence, CMOS, 45nm.**

1. INTRODUCTION

The comparator is the main block in the design of the Sigma Delta Comparator. A one-bit quantizer can be implemented as a comparator whose output toggles between high and low voltage levels, VOH and VOL, based on the polarity of its input voltage with respect to the reference voltage.

However, since investigation of all existing comparator architectures is beyond the scope of this paper, here we limit our discussion to open-loop comparators which is one of the most commonly used structures in Sigma-Delta ADCs.

A like integrators, comparators must satisfy both static, and dynamic requirements in the design part of the Sigma Delta Modulators. As the names imply, static characteristics deal with dc performance of the comparator, i.e. gain, input resolution ($Vin_{(min)}$), and output voltage levels, whereas dynamic characteristics such as slew rate and propagation delay(tp) describe the transient operation of the comparator.

The major design presented in this paper at the architectural level and in circuit level of the comparator presents is taken from the [1-2]. The design steps followed in the paper is from [3], for the design of (W/L) of the transistors in the circuit with parameters of the design at the circuit level.

Clock regenerative comparators are widely used in high speed ADCs because they have positive feedback in regenerative latches to take fast decisions of signal comparison [6]. The digital version of this design has been proposed in the paper [7] which gives FPGA and digital implementation of reconfigurable low pass decimation Architecture for 3.8 MHz.

The clocked digital comparator design from paper [10] explains the major concerns about the High-Gain with the low power. The complete design of the Sigma-Delta Modulator and their blocks with architecture is given in [4]. The design part of comparator presented in this paper is referred from the [3], which helps out the designing part of the comparator with low power and high speed.

This paper explains the basics of the comparator and the parameters of the comparator in the Section 1.1. The implementation of CMOS schematic of the proposed design of the comparator in the Cadence Virtuoso in 45nm CMOS technology is represented in the Section 1.2. The Section 2 explains the results obtained from the design and the comparison of the design parameters with the previous work has been given in this Section.

The Section 3 concludes the paper with the presented design and results required for the particular application of the comparator.

1.1 Op-amp based Comparator

The comparator block present in Sigma-Delta Modulator is shown in the Fig.1.

The comparator is a circuit that compares one analog signal with another analog signal or a reference voltage and outputs a binary signal based on the comparison. The design of the comparator is based on Op-Amp operated in open loop mode.

The comparator is basically a 1-bit Analog-to-Digital Converter and the symbolic representation is given as shown in Fig.1.

Comparator is one of the main blocks in almost all ADC's, depending upon its size and structure it can have a severe impact on the performance of ADC.

The speed and resolution of an ADC is directly affected by the input offset voltage, the delay and input signal range.

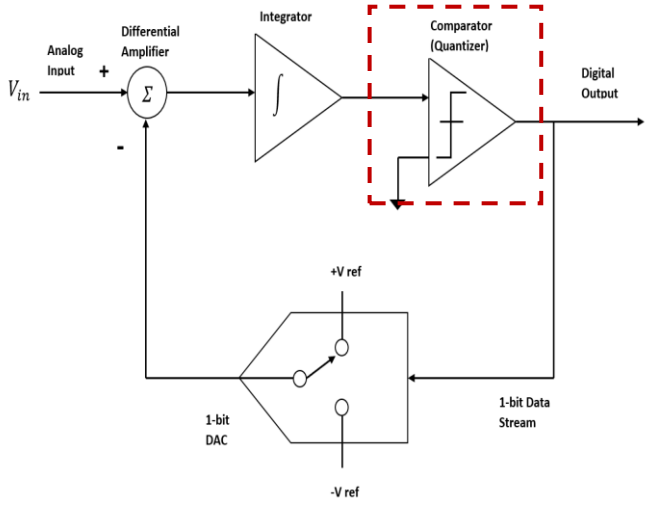

Fig -1 Comparator in Sigma-Delta Modulator.

The output of the above comparator is given below:

$$V_{out} = \begin{cases} V_{OH} & if\ V_{in} > V_{Ref} \\ V_{OL} & if\ V_{in} < V_{Ref} \end{cases}$$

Where,

VOH – The high-level output of the comparator.
VOL – The low-level output of the comparator.

1.2 Design of a comparator.

The schematic of a comparator is shown in the above Fig.-2. The comparator is typically 1-bit ADC is driven by the output of an integrator fed by the differential amplifier in the sigma delta modulator circuit.

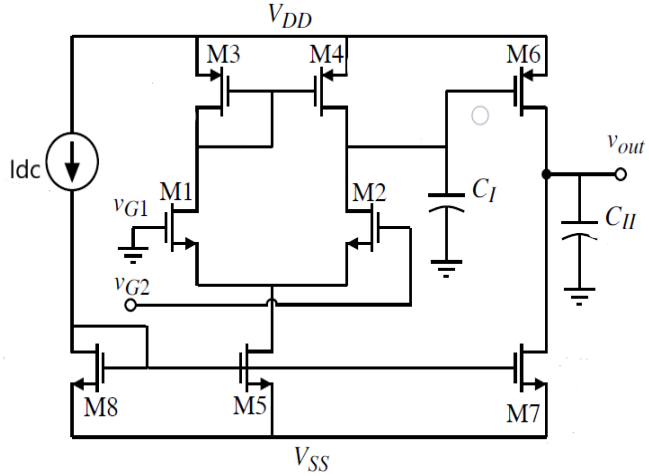

Fig-2: Schematic of the Op-Amp based Comparator

The Comparator compares the input signal from the integrator with the reference signal and gives the corresponding output. It will give a positive signal or Logic "1" whenever the input signal is greater than the reference signal and negative or logic "0" when the input signal is smaller than the reference signal.

The pulse generated so by the Comparator is given as an input to the DAC which is connected as a feedback to the Sigma Delta Modulator circuit. The aspect ratios or (W/L) ratios of the comparator MOSFETs are calculated using equations (1.1) - (1.5). Here it can be observed that the W/L ration is directly proportional to the trans conductance of n-device and the current flowing.

$$\left(\frac{W}{L}\right)_{1,2} = \frac{(g_{m1})^2}{\mu_n C_{ox} \times 2 \times I_1} \quad (1.1)$$

$$g_{m1} = GBW \times C \times 2\pi \quad (1.2)$$

$$\left(\frac{W}{L}\right)_{3,4} = \frac{I_5}{(\mu_p C_{ox}).[V_{DD} - (ICMR)^+ - V_{T3} + V_{T1_{min}}]} \quad (1.3)$$

$$\left(\frac{W}{L}\right)_{5,8} = \frac{2 \times I_5}{(\mu_n C_{ox}) \times V_{DS5_{sat}}^2} \quad (1.4)$$

$$\left(\frac{W}{L}\right)_6 = \frac{g_{m6}}{g_{m4}}\left(\frac{W}{L}\right)_4 \quad (1.5)$$

$$\left(\frac{W}{L}\right)_7 = \frac{I_6}{I_5}\left(\frac{W}{L}\right)_5 \quad (1.6)$$

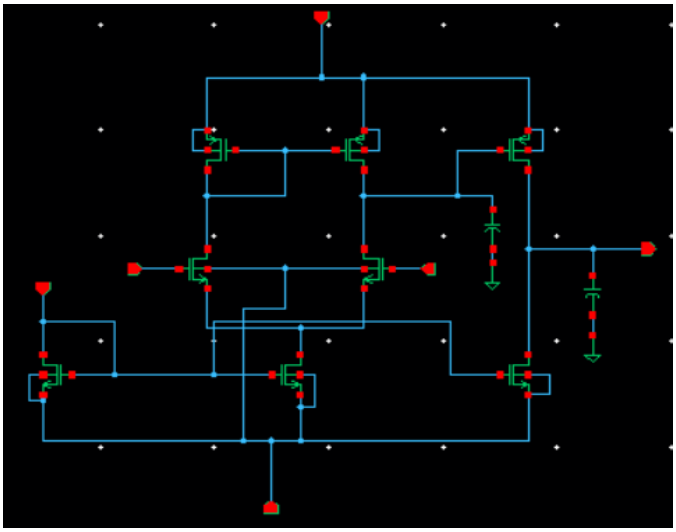

Fig-3 Schematic of the comparator in transistor level.

The design is implemented in 45nm CMOS technology. For each transistor length is taken as 45nm and width is calculated from the W/L ratio.

2. RESULTS

The simulation results of the proposed comparator are given below. The transient analysis of a comparator is shown in the Fig. 4 where green colour signal with sine wave indicate the input signal and the red colour signal is the output wave of the comparator.

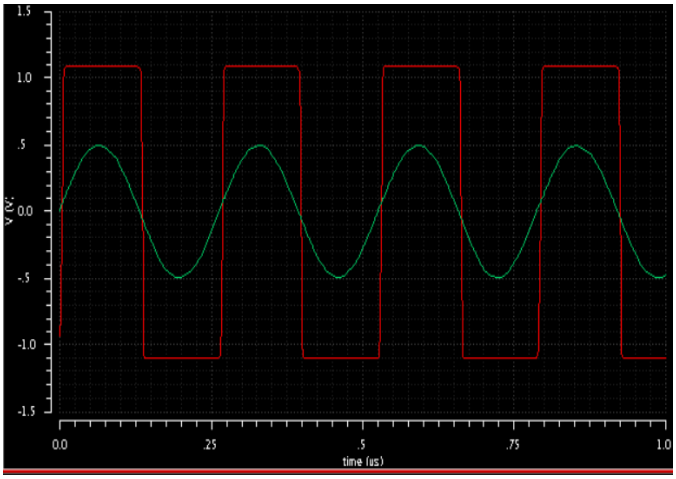

Fig-4 Transient results of Comparator

The designed comparator has the propagation delay of 0.52 ns and power dissipation of the comparator is 25.6 µw. The offset voltage obtained from the DC Voltage Transfer curve is 26mV.

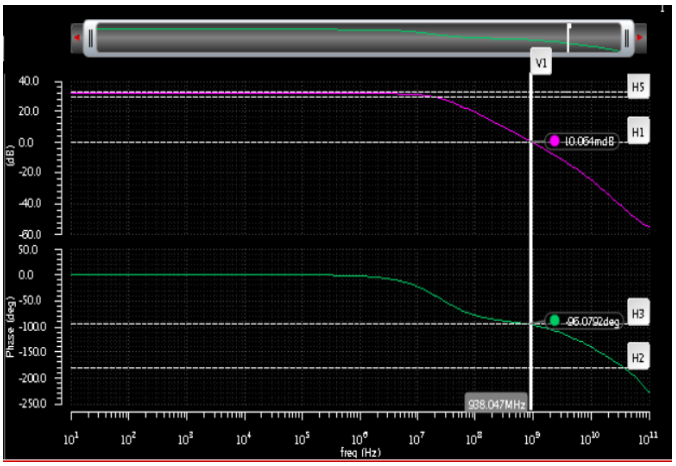

Fig-5 The AC Gain and Phase of the comparator.

Fig. 5 gives the gain and phase margin of the designed comparator as 32dB and 84^0. The above results are measured from the AC Gain and AC Phase margin graph.

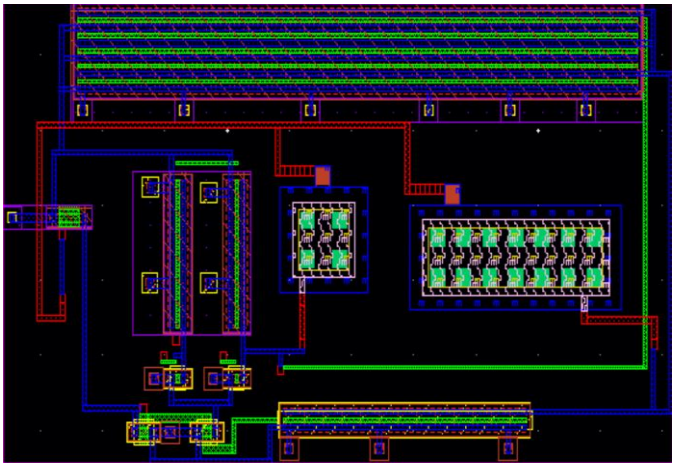

Fig-6 Layout of the comparator using 45nm.

Fig. 6 represents the layout of the comparator using 45nm technology. The MIMcap (Metal-Insulator-Metal) capacitor is used for the representation for the C_I and C_{II} in the layout part.

Table:1 Comparison of parameters and results

Parameters	This work	[9]	[8]
CMOS Technology	45nm	45nm	250nm
Supply voltage(V)	1.1	1.2	1.6
Propagation delay(ns)	0.52	50	0.71
Power dissipation(W)	25.6µ	40.6µ	0.78m

3. CONCLUSION and FUTURE WORK

The designed op-amp based comparator can be used in the sigma delta modulator. The propagation delay of 0.52 ns with the power dissipation of 25.6 µw has been reported. The design met the functionality of the basic comparator. This design is the most suitable one for the design of the Sigma Delta modulator/ADC. In future the multi-bit comparator can be used in the higher order of the comparator that can reduce the noise and offset in the comparator.

REFERENCES

[1] R. Jacob Baker, "CMOS Mixed-Signal Circuit Design" 2nd Edition, *Wiley-IEEE*, 2013.

[2] DA. Johns, K. Martin, "Analog Integrated Circuit Design: Second Edition", *John Wiley & Sons*, 2008.

[3] Philips E. Allen and Douglas R. Holberg, "CMOS Analog Circuit Design", 2nd edition, *New York: Oxford University Press,* 2004.

[4] Jose M. de la Rosa, "Sigma-Delta Modulators: Tutorial Overview, Design Guide, and State-of-the-Art Survey", *IEEE Transactions on Circuits and Systems -I: Regular papers*, Vol. 58, no. 1, January 2011.

[5] T. Sepke, J. K. Fiorenza, C. G. Sodini, P. Holloway, and H.-S. Lee. "Comparator-based switched-capacitor circuits for scaled CMOS technologies". In Proc. *IEEE International Conference Solid-State Circuits,* volume 49, pages 220–221, Feb 2006.

[6] A. Naveena Venancias, K. Hariharan and R. Parameshwaran "High Gain Op-amp based Comparator Design for Sigma Delta Modulator", *Indian Journal of Science and Technology,* Vol 9(29), August 2016.

[7] Kiran Agarwal Gupta, Tejashree Patil, "Low pass Reconfigurable Decimation Filter Architecture for 3.8MHz Frequency", *2nd IEEE International Conference on Recent Trends in Electronics Information & Communication Technology (RTEICT)*, May 19-20, 2017, India.

[8] NurulIffah Mohamad Azizi, Siti Hawa Ruslan, "Design of A Low Power 0.25 µm CMOS Comparator for Sigma-Delta Analog-to-Digital Converter" *IEEE, Student Conference on Research and Development (SCOReD)*, 2015.

[9] P. E. Allen, and D. R. Hollberg, "Two-stage open-loop comparators, in *CMOS Analog circuit Design, Oxford, Oxford University Press*, 2nd Edition, 2002.

[10] Sameer Thakre, Pankaj Srivastava, "Design and Analysis of Low-Power High-Speed Clocked Digital Comparator", *Global Conference on Communication Technologies*, 2015.