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PROXIMITY COUPLED CAVITY BACKED PATCH ANTENNA FOR LONG RANGE UHF RFID TAG

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Abstract - *A novel proximity coupled cavity backed patch antenna for long range RFID tag has been proposed in this paper. The RFID tag may withstand better amount of impact or scratch as the circuitry is protected inside the metal cavity. The novel feeding structures include a full network for impedance tuning. A patch structure having two shorting joints has been proposed, where it not only offer mechanical support but also to tune the resonant frequency of the antenna. A prototype was developed and gained about 5.7 dBi, which gives it a reading range of up to 23 m.*

Key Words: Novel proximity, Antenna, RFID tag, Resonant frequency, Prototype, Metal cavity.

1. INTRODUCTION

Ultra high frequency (UHF) RFID technology has been increasingly used for automatic identification because of its high speed, long reading range and low cost. Various RFID tags with reading range values from several centimeters to 12m have been designed for different applications. Among these designs, near-field RFID was designated for item level applications due to its low cost. Meander line dipoles are low cost and have medium size and long reading range which make them popular in logistics or assets management applications. For applications where reliability and durability are much more important than cost, such as identification of vehicles, heavy equipment or some metallic objects, patch antenna and PIFA are popular.

When the size of an antenna is made much smaller than the operating wavelength, it becomes highly inefficient. Its radiation resistance decreases, while proportionally, the reactive energy stored in antenna neighborhood rapidly increases. Both phenomena make small antennas difficult to match to the feeding circuit, and they display a high Q with very narrow bandwidth when it's matched. There are various solutions to overcome this problem. The best way making small antenna is application of fractal geometry. In recent years, the fractal shape antenna elements have drawn interests of many antenna designers. Fractal geometries are featuring two common properties: fractals are space-filling contours, meaning electrical lengths play such as a viable miniaturization technique and self similarity property. Fractal shaped antenna have various advantages, such as wideband, multiband and reduced size in wire antennas but in micro strip patch antennas the gain and impedance bandwidth decreases seriously, so we should solve this problem using the methods of broad banding of a patch antenna. For improving the inherently narrow bandwidth of a micro strip antenna, it is very effective to use an electrically thick substrate. Several studies for feeding the micro strip antenna with a thick substrate have been reported, such as the L-shaped probe and the capacitive probe-fed structure. Recently the proximity-coupled micro strip antenna with a linear slot in ground plane has also been proposed. It should be noted that the proximity-coupled micro strip antenna without a slot in the ground plane is hard to achieve impedance matching.

1.1 EXISTING SYSTEM

In applications where extreme durability is required, such as forklifts, trucks or shipping containers, the tags must withstand potential impact or scratch. Moreover, long reading range is desired to maintain a safe clearance between the RFID reader and vehicles or containers. One candidate that satisfies both criteria is the class of cavity backed antennas. The cavity can offer both protection against impact or scratch and high gain for long range operations. Although high gain antenna with a protection case (such as plastic or rubber) is also sufficient, metal encased tags are more favorable in some industries such as oil/gas and large equipment manufacturers. The advantage of metal encased tags is that they can be directly welded on the equipment or tools, which saves the effort for drilling holes on hard metals. Additionally, metal tags can be easily integrated into metal frames of large structures.

BOWTIE-TYPE RFID TAG ANTENNA

A bowtie-type RFID tag antenna embedded in a metallic cavity. An improved version using artificial magnetic conductor (AMC) has been reported**.** Both of these antennas realized a gain of up to 7 dBi and reading range exceeding 20 m. However, since a dipole antenna was used, the depth of the cavity was near 50 mm (approximately $\lambda/6$), which makes the whole antenna bulky, expensive and cumbersome to install.

An alternative is a cavity backed patch antenna which is capable of offering a comparable gain with appreciably lower profile

DRAWBACK

- Extreme durability is required
- Bulky process
- High expensive process
- Air gap problem occur

1.2 PROPOSED SYSTEM

A proximity coupled cavity backed patch antenna for long range RFID tag is proposed. The proximity feed and RFID chip are fully enclosed inside the cavity to provide protection. The proximity feed has a π network for impedance tuning. The proposed antenna has a patch structure mounted on the cavity by a rim. The patch structure also offers a way to tune the resonant frequency of the antenna.

ADVANTAGES

- Achieve desired resonant frequency
- Sufficient frequency is present
- Reduce the air gap problem

REQUIREMENTS: HARDWARE REQUIREMENTS

- Processor : Dual core processor
- Hard disk : 160 GB
- RAM : 2 GB
- SOFTWARE REQUIREMENTS
- Matlab 2010
- Windows 7

2. PROPOSED PROCESS DESCRIPTION

RFID TECHNOLOGY

Radio Frequency Identification (RFID) is a technology that uses radio frequency communication to identify, track locations and manage objects, people or animals. The technology is getting popular due to its advantages and low implementation cost plays a critical role as well. It is widely used to track assets and their stock level and at the same time able to track their location on the shelves or warehouse as well. Since it is able to track their location, this also able to find assets which are tagged but have went missing. Other than tracking items, it is also used to track people movement or crowd control through proximity cards and door card readers.

As it seems that RFID technology is being implemented across many different industries, this project looks into the possibility of using the same technology in the military and security industry, exploring the location tracking or positioning capability especially for those who are involved in life threatening missions. The main idea is to embed RFID tags in their uniforms, which able to transmit the information back to the command centre, specifying the wearer's location, hence people in the command centre is able to have a full picture and have better deployment plan.

The main objective of this project is to design and simulate a UWB micro strip antenna which is capable of operating in the range of 3GHz to 5GHz and show a return loss of less than -15dB in the operating range, using the Agilent - Advance Design System.

PROPOSED ANTENNA DESIGN PROCESS

The antenna comprises a cavity, a proximity feed, and a cavity cover with a patch on it. The cavity has thickness of 5 mm and a depth of 3.18 mm to accommodate two 1.52 mm substrates. The proximity feed is a dipole like structure with the RFID chip to be bonded at its center. The proximity feed is fabricated to be sandwiched between two 1.52 mm dielectric substrates. Detailed structure of the cavity cover and the proximity feed is further presented in Fig.2. The thickness of the cavity cover is 1 mm, and it comprises a patch and a rim.

The rim was designed for mounting the cavity cover to the body. Two shorting joints connect the patch to the rim from the middle of its non-radiating edges. The shorting joints will not dramatically affect radiating characteristics of the patch antenna which resonates at the lowest order mode since the electric field reduces to zero in the middle of non-radiating edges. The proximity feed is located in the center of the cavity and has three sections: a coupling section, a _ network for impedance tuning, and a chip bonding section with 1.4 mm gap where an RFID chip can be bonded or soldered. The width of the coupling portion is We, its length is 10 mm, and it extends out of the patch for a distance of Lext. Impedance tuning can be made by the two sets of stubs and the micro strip line in the π network.

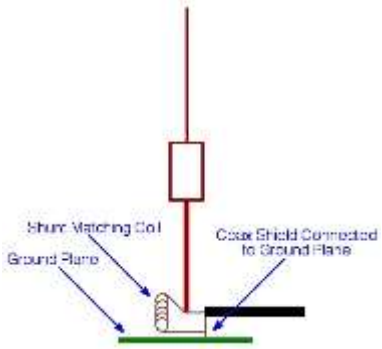
INDUCTIVE MATCHING PROCESS

Impedance matching is an essential part of antenna design. The input impedance of an antenna needs to be reasonably close to the amplifier impedance (e.g. 50 Ohm), otherwise the signal is reflected back to the amplifier and not radiated by the antenna. In many applications matching circuits consisting of discrete inductors and capacitors, or transmission lines are used to improve the impedance matching characteristics of the antenna. This white paper discusses the optimization of matching circuits especially to antenna applications. Although the design of matching circuits sounds simple, there are many practical considerations that need to be addressed.

If you're planning on using a remotely tuned antenna, and an automatic antenna controller, then inductive matching is your only choice if you're seeking fully automatic operation.

Inductive matching works by borrowing a small amount of capacitive reactance from the antenna (by tuning the antenna slightly above the actual transmitting frequency). This borrowed capacitance, and the shunt matching coil's inductance, form a high pass, LC network which transforms the antenna's low impedance (typically 25 ohms or so) to that of the 50 ohm feed line. Installed and adjusted properly, shunt matching will provide a decent match (<1.6:1) over several octaves. Enclosing the matching coil, even in plastic, will affect the frequency versus reactance of the coil, effectively reducing its bandwidth.

Further, the coil must be as clear of surrounding metal as possible. For example, factory supplied shunt coils are often mounted against the antenna's mounting bracket. For best results, these coils should be relocated. You should avoid commercial units which surround the mast, or ones which short out a portion of the coil to achieve a match, as this reduces the effective Q of the coil which increases overall losses. Obviously then, open air, shunt matching coils provide the best match, and least loss of any other matching methodology.



MEMORY ORGANIZATION OF PIC16F877

The memory of a PIC 16F877 chip is divided into 3 sections. They are

1. Program memory
2. Data memory and
3. Data EEPROM

1. PROGRAM MEMORY

Program memory contains the programs that are written by the user. The program counter executes these stored commands one by one. Usually PIC16F877 devices have a 13 bit wide program counter that is capable of addressing 8K×14 bit program memory space. This memory is primarily used for storing the programs that are written to be used by the PIC. These devices also have 8K*14 bits of flash memory that can be electrically erasable /reprogrammed. Each time we write a new program to the controller, we must delete the old one at that time. The figure below shows the program memory map and stack.

2. PIC16F87XA DATA MEMORY ORGANIZATION

The data memory of PIC16F877 is separated into multiple banks which contain the general purpose registers and special function registers. According to the type of the microcontroller, these banks may vary. The PIC16F877 chip only has four banks BANK 0, BANK 1, BANK 2, and BANK4. Each bank holds 128 bytes of addressable memory.

3. DATA EEPROM AND FLASH

The data EEPROM and Flash program memory is readable and writable during normal operation. This memory is not directly mapped in the register file space. Instead, it is indirectly addressed through the Special Function Registers. There are six SFRs used to read and write this memory:

- EECON1
- EECON2
- EEDATA
- EEDATH
- EEADR
- EEADRH

The EEPROM data memory allows single-byte read and writes. The Flash program memory allows single-word reads and four-word block writes. Program memory write operations automatically perform an erase-before write on blocks of four words. A byte write in data EEPROM memory automatically erases the location and writes the new data. The write time is controlled by an on-chip timer. The write/erase voltages are generated by an on-chip charge pump, rated to operate over the voltage range of the device for byte or word operations.

All microcomputer systems, irrespective of their complexity, are based on similar building blocks.

These are shown in Figure 1 and consist of the following:

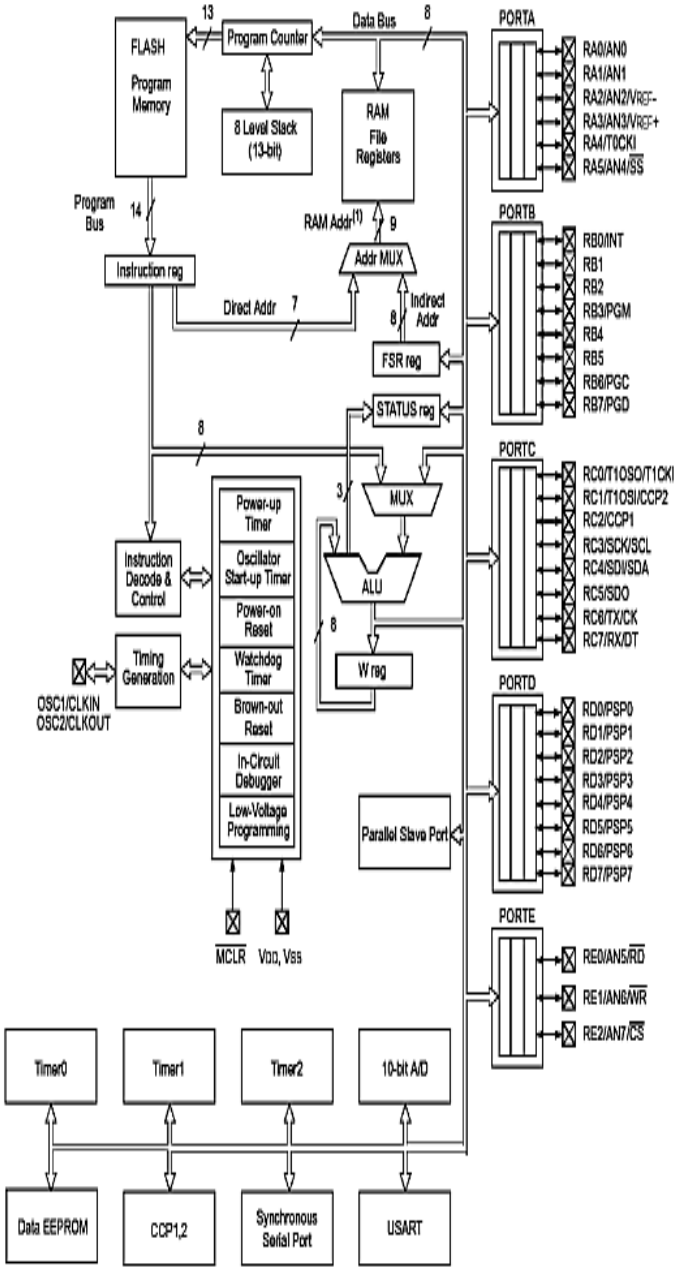
² CPU - the part that does all logic and arithmetic functions

² RAM - storage for programs and/or program variables

² ROM - read-only parts of programs

² I/O - connection to external devices

Device	Program FLASH	Data Memory	Data EEPROM
PIC16F874	4K	192 Bytes	128 Bytes
PIC16F877	8K	368 Bytes	256 Bytes



Note 1: Higher order bits are from the STATUS register.

PIN DESCRIPTION

Pin No	Function	Name
1	Ground (0 V)	Ground
2	Supply voltage; 5V (4.7V – 5.3V)	Vcc
3	Contrast adjustment; through a variable resistor	VEE
4	Selects command register when low; and data register when high	Register Select
5	Low to write to the register; High to read from the register	Read/write
6	Sends data to data pins when a high to low pulse is given	Enable
7	8-bit data pins	DB0
8		DB1
9		DB2
10		DB3
11		DB4
12		DB5
13		DB6
14		DB7
15	Backlight Vcc (5 V)	Led+
16	Backlight Ground (0V)	Led-

TEST RESULT AND ANALYSIS

TESTING

A program represents the logical elements of a system. For a program to run satisfactorily, it must compile and test data correctly and tie in properly with other programs. Achieving an error-free program is the responsibility of the programmer. Program testing checks for two types of errors: syntax and logic.

When a program is tested, the actual output with the expected output is going to compare. When there is discrepancy, the sequence of instructions must be traced to determine the problem. Breaking the program down into self-contained portions, each of which can be checked at certain key points, facilitates the process. The idea is to compare program values against desk-calculated values to isolate the problem.

Testing is an important stage in the system development life cycle (SDLC). The test case is a set of data that a system will process as normal input. As its philosophy behind testing is to find errors the data are created with the express intent of determining whether the system will process them correctly.

Software testing is an important element of software quality assurance and represents the ultimate review of specification, design and loading. The increasing visibility of software AR a system element and the costs associated with a software failure are motivating for well planned through testing.

TEST OBJECTIVES

These are several rules that can save as testing objectives they are: Testing is a process of executing program with the intent of finding an error. A good test case is one that has a high probability of finding an undiscovered error. If testing is conducted successfully according to the objectives as stated above it would in cover errors in the software also testing demonstrator that software functions appear to the working according to specification that performance requirements appear to have been met.

PROGRAM TESTING

There are three ways to test a program

1. for correctness
2. For implementation, efficiency and
3. For Computations complex city.

Test for correctness is supposed to verify that a program does actually what it is designed to do. This is much more difficult than it May appear at first, especially for large programs. Test for implementation efficiency attempt to find ways to make a correct program faster or use less storage.

TESTING AND CORRECTNESS

The following ideas should be a fact of any testing plan.

- Preventive measures
- Spot-checks
- Testing all parts of the program
- Test data
- Looking for trouble
- Time for testing

The entire testing process can be divided into three phases.

- Unit Testing
- Integrated Testing
- Final/System Testing

TEST CASES

SYSTEM TESTING

System testing is testing conducted on a complete, integrated system to evaluate the system's compliance with its specified requirements. System testing falls within the scope of black box testing, and as such, should require no knowledge of the inner design of the code or logic.

UNIT TESTING

In unit testing, the entire program that makes the system tested. Unit testing first focuses on the modules, independent of one another to locate errors. This enables to detect errors in coding and the logic within the module alone. In the unit testing control path are tested to remove errors within the boundary of the module.

INTEGRATION TESTING

Integration testing can proceed in a number of different ways, which can be broadly characterized as top down or bottom up. On top down integration testing the high level control routines are tested first, possibly with the middle level control structures present only as stubs.

FUNCTIONAL TESTING

Functional testing is a type of black box testing that bases its test cases on the specifications of the software component under test. Functions are tested by feeding them input and examining the output, and internal program structure is rarely considered (Not like in white-box testing).

WHITE BOX TESTING

This is a test case design method that uses the control structure of the procedural design to derive test cases. Using it, the software engineer can derive test cases that, Guarantee that all independent paths within a module have been exercised once.

BLACK BOX TESTING

This focuses on the functional requirements of the software. It enables the software engineer to derive sets of input conditions that will fully exercise all functional requirements for a program. It attempts to find errors such as:

- Incorrect or missing functions
- Interface errors
- Errors in data structures or external database access

ANALYSIS

Test analysis is the process of looking at something that can be used to derive test information. This basis for the tests is called the test basis.

The test basis is the information we need in order to start the test analysis and create our own test cases. Basically it's a documentation on which test cases are based, such as requirements, design specifications, product risk analysis, architecture and interfaces.

We can use the test basis documents to understand what the system should do once built. The test basis includes whatever the tests are based on. Sometimes tests can be based on experienced user's knowledge of the system which may not be documented. From testing perspective we look at the test basis in order to see what could be tested. These are the test conditions. A test condition is simply something that we could test.

While identifying the test conditions we want to identify as many conditions as we can and then we select about which one to take forward and combine into test cases. We could call them test possibilities. As we know that testing everything is an impractical goal, which is known as exhaustive testing. We cannot test everything we have to select a subset of all possible tests. In practice the subset we select may be a very small subset and yet it has to have a high probability of finding most of the defects in a system. Hence we need some intelligent thought process to guide our selection called test techniques. The test conditions that are chosen will depend on the test strategy or detailed test approach. For example, they might be based on risk, models of the system, etc.

3. CONCLUSION

A proximity coupled cavity backed patch antenna was proposed for long range RFID tags. The proposed antenna features a thick metal patch with a rim which is mounted on a cavity. The proximity feed and RFID chip were fully enclosed and protected inside the cavity. It has a realized gain of approximately 5.72 dBi, which can provide a reading range of up to 23 m. The metal cavity is expected to sustain fair amount of mechanical impact or scratch. Moreover, a _ network was incorporated with the proximity feed to allow fine tuning of the antenna input impedance. The shorting joints between the patch and the rim not only offered mechanical support for the patch but can also be used to tune the resonant frequency of the antenna. The bandwidth of the proposed design was approximately20 MHz. However, by tuning the matching network, wider band width may be expected. Although the gain is smaller than in previous works, it can be improved by increasing the cavity depth or patch width.

REFERENCES

[1] P. V. Nikitin, K. Rao, and S. Lazar, "An overview of near field UHF RFID," in IEEE international Conference on RFID, vol. 167. Citeseer, 2007.

[2] K. S. Rao, P. V. Nikitin, and S. F. Lam, "Antenna design for UHF RFID tags: a review and a practical application," IEEE Transactions on Antennas and Propagation, vol. 53, no. 12, pp. 3870–3876, Dec. 2005.

[3] L. Mo and C. Qin, "Planar UHF RFID tag antenna with open stub feed for metallic objects," IEEE Transactions on Antennas and Propagation, vol. 58, no. 9, pp. 3037–3043, Sep. 2010.

[4] H.-D. Chen and Y.-H.Tsao, "Low-profile PIFA array antennas for UHF band RFID tags mountable on metallic objects," IEEE Transactions on Antennas and Propagation, vol. 58, no. 4, pp. 1087–1092, Apr. 2010.

[5] S.-L. Chen and K.-H.Lin, "A slim RFID tag antenna design for metallic object applications," Antennas and Wireless Propagation Letters, vol. 7, pp. 729–732, 2008. [6] D. Kim and J. Yeo, "A passive RFID tag antenna installed in a recessed cavity in a metallic platform," IEEE Transactions on Antennas and Propagation, vol. 58, no. 12, pp. 3814–3820, Dec. 2010.

[7]"Dual-band long-range passive RFID tag antenna using an AMC ground plane," IEEE Transactions on Antennas and Propagation, vol. 60, no. 6, pp. 2620–2626, Jun. 2012.

[8] N. C. Karmakar, "Investigations into a cavity-backed circular-patch antenna," IEEE Transactions on Antennas and Propagation, vol. 50, no. 12, pp. 1706–1715, Dec. 2002.

[9] J.-C. Cheng, N. Dib, and L. P. Katehi, "Theoretical modeling of cavitybacked patch antennas using a hybrid technique," IEEE Transactions on Antennas and Propagation, vol. 43, no. 9, pp. 1003–1013, Sep. 1995.

[10] R. Garg, Microstrip antenna design handbook. Artech house, 2001.

[11] Tagformance. http://www.voyantic.com/tagformance.