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Low Frequency CMOS Sigma-Delta Analog to Digital Converter for Medical Application

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Abstract - *In mobile and portable devices low power dissipation, low noise, high speed, less offset voltage is required. The performance of such systems mainly depends on Analog to Digital Converters(ADC). An ADC consists of gain amplifiers and comparators. In wireless applications oversampling ADC has become popular because of its increased performance and flexibility. Oversampling uses a sampling rate that is much greater than the bandwidth of the signal of interest and Sigma Delta ADC is one such converter.*

The Sigma Delta ADC has two major blocks: one is the modulator and the other is the decimator. The basic architecture of Sigma Delta Modulator consists of a differential amplifier, an integrator, a comparator and a Digital to Analog Converter(DAC) in the feedback loop of the modulator. The main objective of this project is to design and simulate analog circuits for Sigma Delta ADC in 180nm CMOS technology using Cadence EDA tool.

Key Words: **Analog to Digital Converter, Sigma-Delta ADC, Op-Amp, Switched capacitor integrator, CMOS.**

1.INTRODUCTION

Recent research on portable and wearable health care systems emphasizes both on higher performance to meet customer demand for low-cost and low-power. This reduction in power can be achieved by moving towards smaller feature size. However, as we move towards smaller feature size, the process variations and other non-idealities will greatly affect the performance of the device. One of the applications where low power dissipation, low noise, high speed, less offset voltage are required is Analog to Digital Converters (ADC) for mobile and portable devices in biomedical applications. The performance limiting factors of such ADC are gain amplifiers and Comparators. In wireless application of biomedical devices, oversampling ADC has become popular because of its increased performance and flexibility. Oversampling uses a sampling rate that is much greater than the bandwidth of the signal of interest. Sigma-Delta ADC is a low-cost, low-bandwidth, low-power, high-resolution ADC.

The rest of the paper is organized as follows. Section 2 explains the architecture and the design of the proposed Sigma-Delta ADC. Section 3 discusses each circuit's operation principle. Measured results are presented in Section 4. Finally, Section 5 draws our conclusion.

2. ARCHITECTURE OF THE PROPOSED ADC

A basic first-order Sigma-Delta modulator can be seen in Fig 1. Here, an integrator and a 1-bit ADC are in the forward path, and a 1-bit DAC is in the feedback path of a single-feedback loop system. The variables labeled are in terms of time, T, which is the inverse of the sampling frequency and k, which is an integer. The 1-bit ADC is simply a comparator that converts an analog signal into either a high or a low. The 1-bit DAC uses the comparator output to determine if VREF or - VREF is summed with the input.

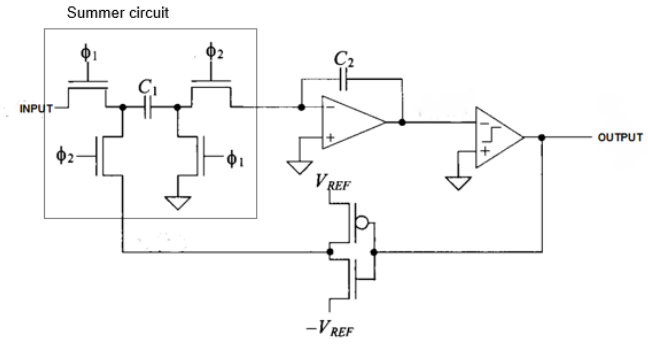


Fig-1: A first-order sigma-delta modulator

3.CIRCUIT DESIGN

3.1. Two stage Op-Amp

Two stage Op-Amp configuration shown in Fig 2 is one of the most widely used operational amplifier. It provides a good common mode range, good voltage gain and a good output swing. The PMOS transistors are used as input differential pair. The PMOS current mirror acts as a load circuit, in order to increase the common mode rejection ratio(CMRR) of the Op-Amp. The n-MOS current mirror circuit serves as a constant current source providing bias current to the differential pair. The single ended output of the differential pair is driving the PMOS transistor of the common source stage.

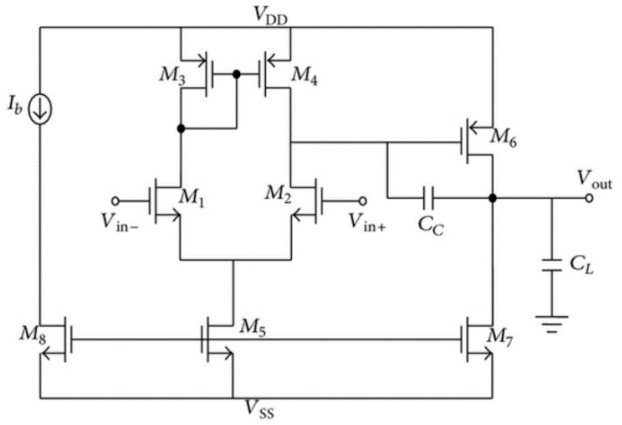


Fig-2: Schematic of Op-Amp

3.2. Analog comparator

A Comparator is a circuit that performs the operation of comparing two analog input signals and decoding the difference in to a single digital output signal. Fig 3 shows the symbol of Comparator.

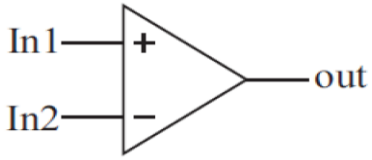
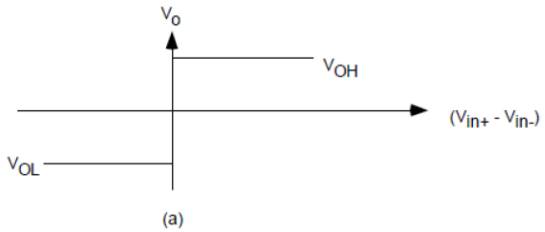


Fig-3: Comparator symbol

Comparator is one of the most critical block of almost all ADC's, depending upon its size and structure it can have a severe impact on the performance of ADC. The speed and resolution of an ADC is directly affected by the input offset voltage, the delay and input signal range. Comparators are classified depending upon the nature of signal, functionality and inputs, like voltage and current Comparators, continuous and discrete time etc. Some of the basic applications of Comparators is ADC, function generation, signal detection. The Comparator takes the analog input and gives a binary or digital output as shown in Fig 4.



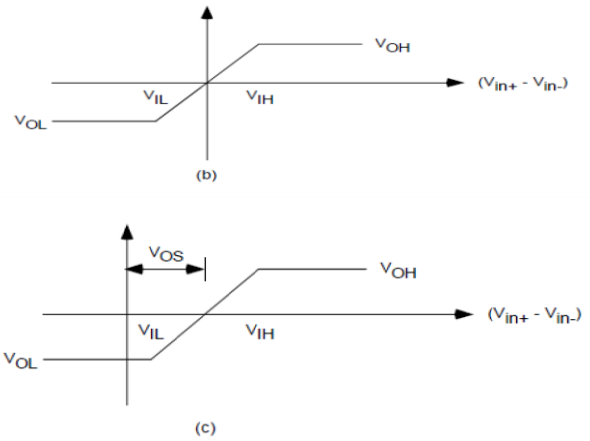


Fig-4: (a), (b), (c) Different outputs of Comparator

Fig 4 (a) defines the output of the Comparator as shown in equation (1)

$$V_o = \begin{cases} V_{OH} & if\ V_{in+} - V_{in-} > 0 \\ V_{OL} & if\ V_{in+} - V_{in-} < 0 \end{cases} \quad (1)$$

This is not realizable as its gain is infinity. Fig 4(b) shows the characteristic of a realizable first order Comparator as shown in equation (2)

$$Vo = \begin{cases} V_{OH} & if(V_{in+} - V_{in-}) > V_{IH} \\ A_V(V_{in+} - V_{in-}) & if\ V_{IL} < (V_{in+} - V_{in-}) < V_{IH} \\ V_{OL} & if(V_{in+} - V_{in-}) < V_{IL} \end{cases} \quad (2)$$

One of the non-ideal characteristic of Comparator is presence of input offset. That is the output does not change until the difference input reaches the input offset voltage. Fig.4(c) shows these characteristics of the output which is defined in equation (3)

$$Vo = \begin{cases} V_{OH} & if(V_{in+} - V_{in-}) > V_{IH} \\ A_V(V_{in+} - V_{in-}) - A_V V_{OS} & if\ V_{IL} < (V_{in+} - V_{in-}) < V_{IH} \\ V_{OL} & if(V_{in+} - V_{in-}) < V_{IL} \end{cases} \quad (3)$$

If the input is sufficiently small then the output will not slew and the transient response will be a linear one. The settling time is defined as the time needed for the output to reach a final value within a determined tolerance, when excited by a small signal. The settling time of small signal is determined by the gain bandwidth product of the amplifier. If the input magnitude is sufficiently large then the Comparator will slew by virtue of not having enough current to charge or discharge the compensating or load capacitor. The slew rate is determined from the slope of the output during the rise or fall of the output. It is limited by the current sourcing or current sinking capability in charging the output capacitor. Settling time is very important in analog signal processing. It is very much necessary to wait until the amplifier has settled to within a few tenths of percent of its final value in order to avoid errors in the accuracy of processing the analog signal. A longer settling time indicates the reduction in the rate of processing analog signal.

3.3. Switched Capacitor Integrator

Integrators are used in many analog systems. The circuit operates in sampling and integration modes as shown in Fig 5. In the sampling mode S1 and S3 are ON and S2 and S4 are OFF, allowing the voltage across C1 to track Vin while the Op-Amp and C2 hold the previous value. In the transition to the integration mode, S3 turns OFF first, injecting a constant charge on to C1, S1 turns OFF next and subsequently S2 and S4 turn ON. The charge stored on C1 is therefore transferred to C2 through the virtual ground node. Since S3 turns OFF first, it introduces only a constant offset, which can be suppressed by differential operation. Moreover, because the left plate of C1 is "driven", the charge injection or absorption of S1 and S2 contributes no error. Also, since node X is a virtual ground, the charge injected or absorbed by S4 is constant and independent of Vin.

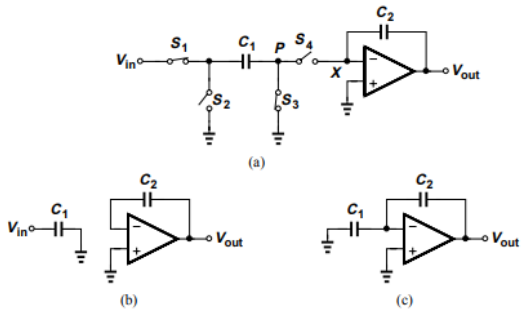


Fig-5: (a) Parasitic-insensitive integrator, (b) circuit of (a) in sampling mode, (c) circuit of (a) in integration mode.

3.4. 1-bit DAC

It is a circuit for converting a digital usually binary code to analog signal (current, voltage or charges). The DAC acts as an interface between digital world and analog world. The DAC takes digital signal as the input and outputs an analog signal in form of current, voltage or charge. Fig 6 shows the basic symbol of a DAC.

Fig-6 : 1-bit DAC

3.5 Decimation Filter

Decimation is the process of reducing the sampling rate, this usually implies lowpass-filtering a signal, then throwing away some of its samples. Down sampling is a more specific term which refers to just the process of throwing away samples, without the lowpass filtering operation. When decimation is performed on a sequence of samples of a signal or other continuous function, it produces an approximation of the sequence that would have been obtained by sampling the signal at a lower. The decimation factor is usually an integer or a rational fraction greater than one. This factor multiplies the sampling interval or, equivalently, divides the sampling rate. Fig 7 shows the D-Flip flop as a Decimation Filter.

4. RESULTS

The Sigma-Delta A/D converter stands out to be the most advanced, among all the Data converters. A block level schematic of a first order Sigma-Delta Converter as shown in Fig 8 consists of Integrator, a Comparator (1bit ADC), 1-bit DAC. In the circuitry, a 1-bit ADC (generally known as a Comparator) is driven by the output of an integrator which is fed with an input differenced with the output of a 1-bit DAC. In Nyquist rate A/D converters, the sampling rate is twice the input signal frequency for error free signal approximation. Only way to decrease the Quantization noise or better signal representation is sampling the signal many more times. This is the fundamental theory in Sigma-Delta ADC.

A sinusoidal signal of 250mV and frequency of 250Hz is input to the switched Capacitor circuit whose other terminal is connected to the feedback output signal of 1bit DAC. The output of this circuit is given to the integrator and the other terminal of integrator is connected to a ground. the output of the integrator is given to the Comparator. The Comparator compares the input signal from the integrator with the reference signal and gives the corresponding output as shown in Fig.8. It will give a positive signal whenever the input signal is greater than the reference signal and negative when the input signal is smaller than the reference signal. The pulse generated so by the Comparator is given as an input to the DAC which is connected as a feedback to the ADC circuit. This process is iterated several times to get a series of digital bit stream. The simulation result of the circuit is shown in Fig.9.

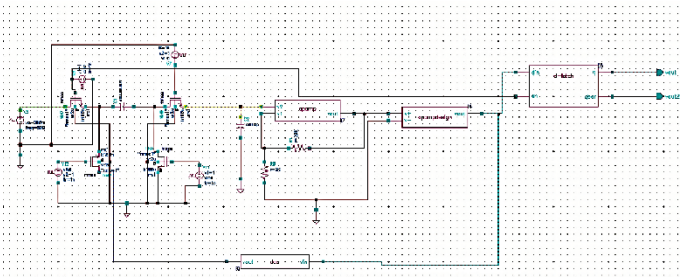


Fig-8: Schematic of a Sigma-Delta ADC

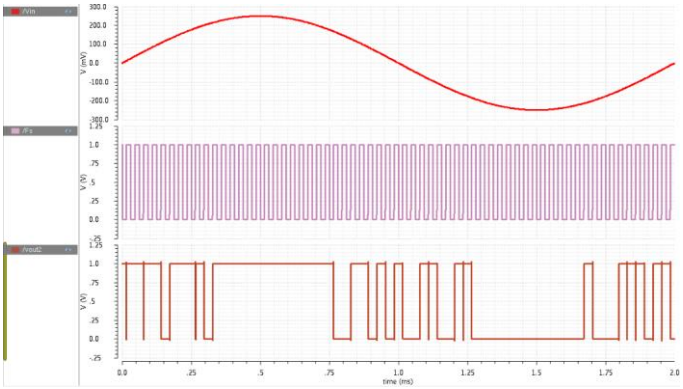


Fig-9: Simulation result of Sigma-Delta ADC

The simulation is carried out for sinusoidal signal as an input analog signal and corresponding digital stream of pulses at the output of the Modulator circuit is obtained. This is achieved due to the continuous iteration of the input signal to the Modulator. At the output of this a Decimation Filter is used to decimate the oversampled signal and to produce a digital output.

5. CONCLUSIONS

A Sigma-Delta Analog to Digital Converter is designed by using Op-Amp which is one of the key components, which helps in the smooth operation of the integrator circuit. The zero-crossing Comparator is designed using Op-Amp, which compares the input signal with reference voltage i.e. zero and gives the corresponding result which is then fed to 1-bit Digital to Analog (DAC) circuit in the feedback path of the system. This process is iterated and a pulse of digital signal is achieved at the output of the system. The Sigma-Delta ADC was simulated using a standard 180nm CMOS technology using Cadence EDA tool.

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