

AUTOMATIC CAR PARKING SYSTEM CIRCUIT USING VERILOG HDL

Abhiyash Hodge¹, Hrishikesh Humnabadkar², Akshay Bidwai³

^{1,2,3}Electronics and Telecommunication, Department Vishwakarma Institute of Technology, PUNE, INDIA

Abstract— Gone are the days when we were seeing only a few number of vehicles on road. Out of them, the number of cars can be equated to almost to a very small number. But with increasing urbanization and population, in the last few decades, there has been a considerable and enormous rise in the number of vehicles. Also, there has been a substantial rise in the number of four-wheelers. Due to this increased number, the problem of parking has come out to be an important issue. In huge malls, educational institutes, organizations the limited parking space and increased vehicles have led parking problems. People usually waste huge time in parking vehicles at such places. In order to cater to this problem here is an attempt to design the system known as “Automatic Car Parking System”. The system automatically checks the availability of free slots and parks customer vehicles. Also, it tells the customer to remember the number of parking slot at which their vehicle is parked so that it can find their vehicle and remove it from the parked place. In order to design the proposed circuit, a Verilog HDL code is implemented which is then further synthesized on FPGA to get the required design.

Index Terms— number of car, parking, time wastage, automatic system, Verilog HDL, Questa Sim, FPGA.

I. INTRODUCTION

HE main cause of parking problems worldwide is ever increasing population and with it the number of vehicles. The place available for parking is limited but the number of vehicles increasing on road daily has no check. According to the recent trends, there has been an exponential rise in the sale of cars. The number of cars sold worldwide increased tremendously from 39.2 million in 1999 to 81.57 million in 2018. In 20 years the sales were raised by a value as high as approximately equal 40 million. The statistics in the form of a graph are represented in Figure 1.

Due to this enormous increase in traffic on road, the immediate next consequence that was observed was a sudden increase in congestion problems on road. Figure 2 depicts the increase in congestion problems from 1987 to 2003. This gave rise to an increasing number of accidents on roads and also the travelling time required to reach destination increased. Even to cover a small distance consumed much

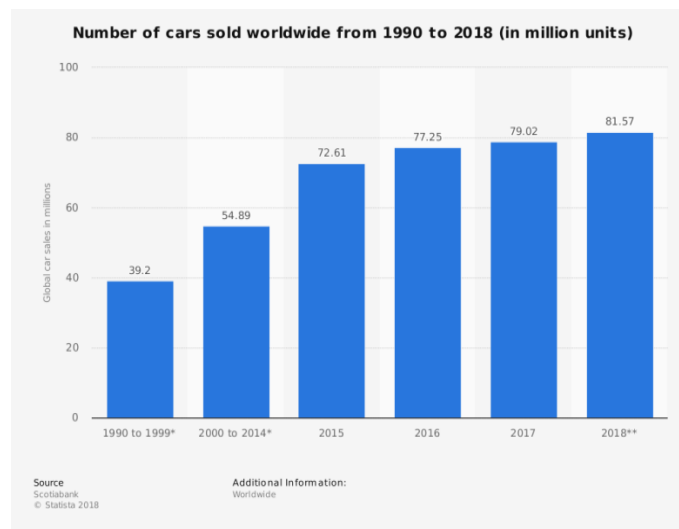


Fig.1 Statistics showing number of cars sold worldwide from 1990 to 2018 time.

To solve and sort out these parking problems in huge malls, educational institutes and to avoid wastage of time at parking, of people visiting such organizations, here is an attempt made to make the parking process a lot easier. Also, with the help of evolving technologies, the system can be updated further to bring about a fully automated parking system. At places with parking problems, people have to wait in a long queue and search for free slots available as there is no method to trace the vacant slots automatically. Even if there are slots available, visitors don't get to know due to huge infrastructure and they end up wasting time in searching for slots. The time that would have been useful to do some

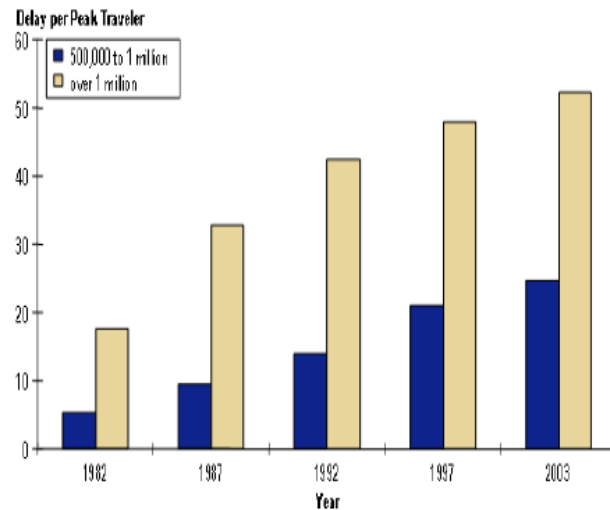


Fig.2 Graph showing congestion problems in urban areas important work is just wasted in parking vehicle.

Our system continuously monitors the available parking slots at such places and displays the available free slots at the entrance. This saves the time of visitors which would have been wasted in standing long queue and hunting for the available free slots manually.

II Background Study And Related Work

Soh Chun Khang, et.al (2010) presented work on parking system in which the number of slot which is available for parking is send as a message to driver. Driver can resend sms demanding for a new position when the earlier allotted slot gets filled [1]. Huachun tan, et.al (2009) proposed a system which is helpful to find the park at places where there a large parking lot. This is done by capturing images through camera mounted at each parking slot. Information such as number plate of car and colour are recognized and stored in data. This data therefore includes information about all cars parked in the lot and hence it is possible to find any car easily [2]. S.V.Srikant, et.al(2009) camp up with system to detect the free parking slots. Author has used wireless communication technology to make the parking system more efficient [3]. Gongjun Yan, et.al (2011), proposed an intelligent parking system which was based on secured wireless system and sensor communication. Efficient parking space utilization and quick search of free slot was the work involved [4].

Insop Song et.al, (2006) worked upon system using Field Programmable Gate Array(FPGA) using Fuzzy Logic Controller. Advantage of this system is reduction in computation time [5].

III Main Body of the Paper

A: Technique:

The flowchart of the system follows as shown in Figure 3. Proposed System continuously searches for available free parking slots and guides the visitor to a particular parking slot. The circuit is developed by writing a Verilog Code using QuestaSim and ModelSim Softwares. Further it is synthesized using Xilinx. Also, after parking, the system also prompts the visitor or vehicle owner to remember the parking slot number.

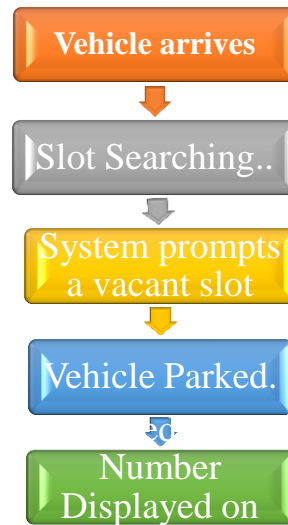


Fig.3. Flowchart of system

Each parking slot consists of sensor mounted which continuously detects presence of vehicles and communicates the status to the display at the entrance. Accordingly, the complete information i.e. the total number of slots available, the vacant parking slots and the filled parking slot. With the help of this information, one can then easily park his/her vehicle at desired place. As soon as the vehicle is parked, the system prompts number at which the vehicle is parked. This will be helpful in finding vehicle again.

B: Description:

Questa Sim

The Questa Advanced Simulator is the core simulation and debug engine of the Questa Verification Solution; the comprehensive advanced verification platform capable of reducing the risk of validating complex FPGA and SoC designs.

The Questa Advanced Simulator achieves industry leading performance and capacity through very aggressive, global compile and simulation optimization algorithms of System Verilog and VHDL, improving System Verilog and mixed VHDL/System Verilog RTL simulation performance by up to 10X. Questa also supports very fast time to next simulation and effective library management while maintaining high performance with unique capabilities to pre-optimize and define debug visibility on a block by block basis enabling dramatic regression throughput improvements of up to 3X when learning a large suit of test.

We used this software for coding in Verilog and simulating the design. Simulation gave results in the form of waveform.

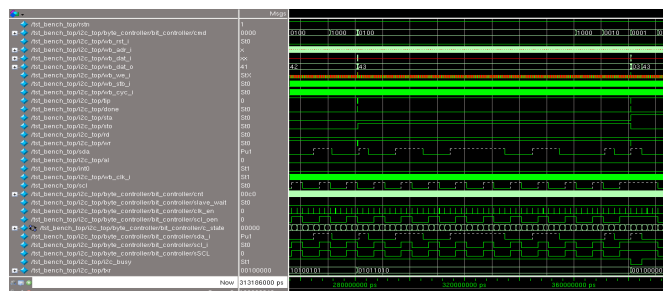


Fig.4. Simulation Window

ModelSim

ModelSim is multi-language HDL simulation environment by Mentor Graphics for simulation of hardware description language such as VHDL, Verilog and SystemC and includes built-in C debugger. It can be used independently, or in conjunction with Intel Quartus Prime, Xilinx ISE or Xilinx Vivado. Simulation is performed using the graphical user interface(GUI) or automatically using scripts. ModelSim uses a unified kernel for simulation of all supported languages, and the method of debugging embedded C code is the same as VHDL or Verilog.

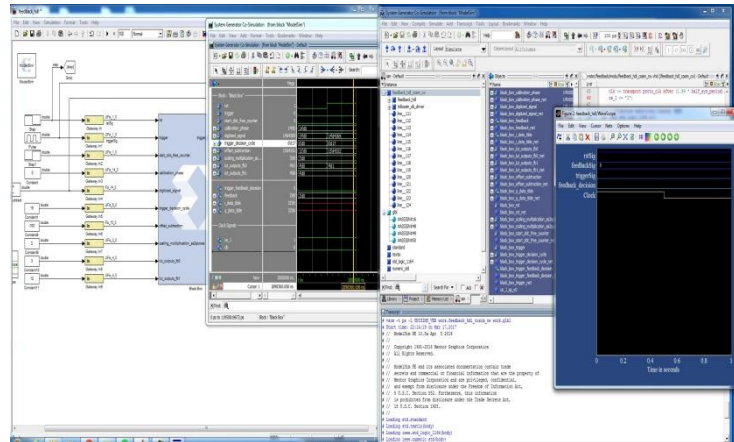


Fig.5. Simulation Window

Xilinx

Xilinx is a software tool produced by Xilinx for synthesis and analysis of HDL designs, enabling the developer to synthesize (“compile”) their designs, performing timing analysis examine RTL diagrams, simulate a design’s reaction to different stimuli, and configure the target device with the programmer. Xilinx ISE(Integrated Synthesis Environments) was used to synthesize the design that was implemented using Verilog code. With the help of this software, the required RTL Schematic and Technology Schematic for the project was obtained. Also Area Report which indicates the number of gates required, number of latches used, the board utilization efficiency was generated through Xilinx. It gave a fair idea about the requirement of circuit hardware components and their quantities.

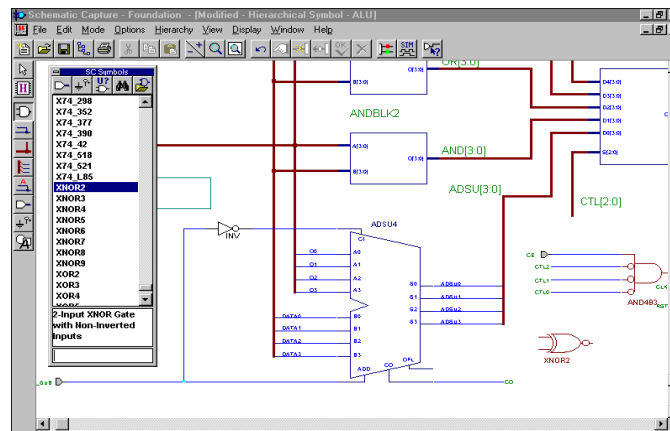


Fig.5. RTL Schematic Window

IV Performance and experiments

The primary aim of this project is to solve the problem of parking and to avoid time wastage of people visiting big organization and congested places. For designing this system and for hardware synthesis, a code is written in Verilog HDL. This is then converted to hardware design or synthesized using Xilinx ISE. The code written makes use of certain useful special features of Verilog Language such as functions, tasks, blocking and unblocking statements, fork join, repeat, etc. Use of these features makes a coding a lot more generalized and helps in executing complex statements.

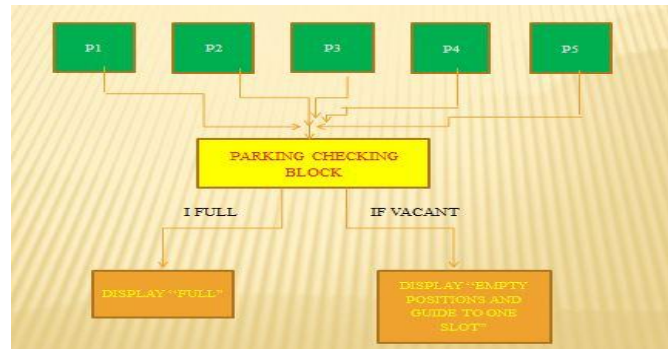


Fig.6. Flow of System

Results

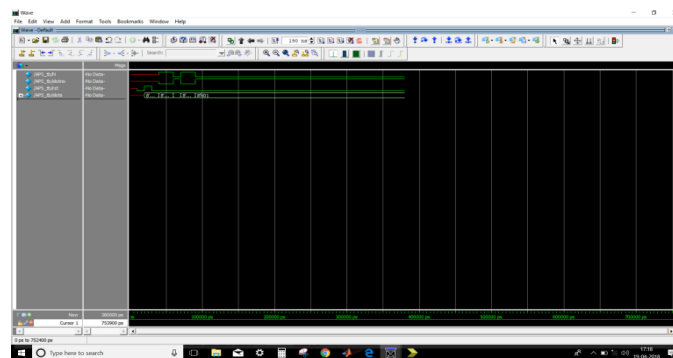


Fig.7. Waveforms

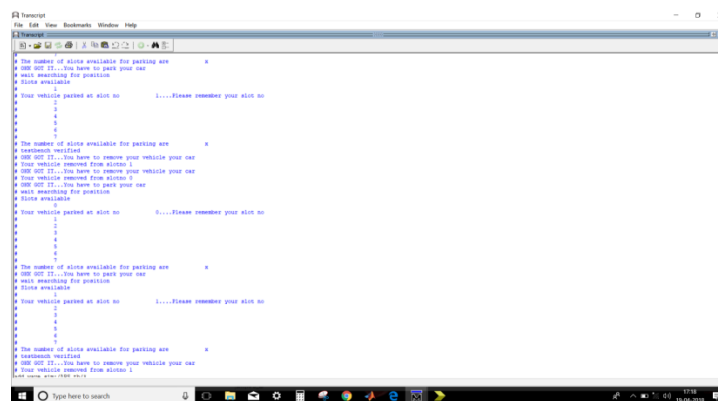


Fig.8. Output on Display

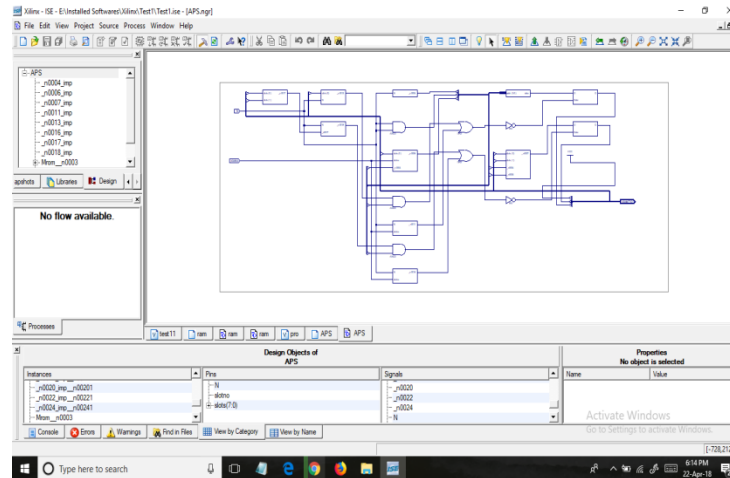


Fig.9. RTL Schematic

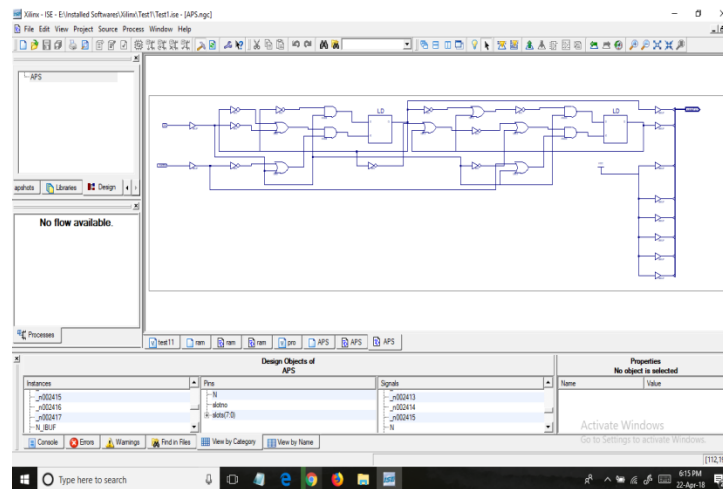


Fig.10. Technology Schematic

CONCLUSION

This type of system is very useful as it avoids wastage of time of people in an unproductive work. Also it eliminates the tedious work of finding a vacant parking at crowded places such Malls, Huge Organizations by loitering here and there and wasting our time doing so. With the help of this system, one can get a complete view of parking slots, out of which, the number of filled and empty slots just at entrance on a display. Then one directly go to that slot to park his/her vehicle. As soon as vehicle is parked, the empty slot on screen changes to filled slot. So, if implemented, this will save a lot of time of people and also will help in technological advancement of society.

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