A New Multilevel Inverter with Fault-Tolerant Capability

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Abstract – Multilevel inverters (MLI's) have been increasingly implemented for high power DC-AC conversion. Recently, avenues are also being explored to employ MLI's for low power applications. However, for increased number of levels, component count remains a challenge. In this paper a new inverter topology is proposed which utilizes six active switches along with asymmetric source configuration to synthesize 7-level waveform which is capable to tolerate switch fault. A cascaded H-bridge inverter with similar source configuration would require eight active switches, all operating at high switching frequency. A modulation procedure is proposed using which the switches with highest blocking voltages operate at fundamental frequency. Working of the proposed inverter is explained and concepts are validated with simulation results.

Index terms – Multilevel inverter, topologies, asymmetric source configuration.

I. Introduction

Since past few decades, multilevel voltage source inverters have gained reputation as cost-effective and efficient solution for high power DC to AC conversion applications [1]. A multilevel inverter (MLI) utilises several input DC levels and power semiconductor devices to synthesize a staircase waveform. The voltage stresses experienced by the power switches are lower as compared to the overall operating voltage level [2]. The multilevel stepped waveform has better harmonic profile as compared to the two level waveform obtained from the conventional inverters. Further advantages of MLIs are higher efficiency, reduced dv/dt stresses on the load and possibility of fault tolerant operations [3]. In recent times, avenues are also being explored to employ MLIs for low power applications [4-6] apart from their application in medium/high power and high voltage systems.

The harmonic profile of the multilevel waveform improves as the number of levels increases. However, it leads to increased count of power switches and accompanying gate driver circuits, heat sinks and protection circuits. Thus, the overall system becomes complex and expensive. Therefore, newer topologies are being proposed so as to reduce the number of power switches for an increased number of levels in the output.

The so-called 'cross-connected sources based multilevel inverter (CCS-MLI)' has been recently proposed by Gupta and Jain [7] with a view to reduced the device count. It is shown in [7] that the CCS-MLI topology leads to a substantial decrease in component count as compared to the classical topologies. It also leads to simplicity and better efficiency.

In this paper, a 'Seven level asymmetric source based MLI' has been added to the CCS-MLI so as to 'increase' the number of levels in the output. In this paper, working of the proposed structure has been briefly discussed which consist of two switched sources connected in series. The proposed topology needs less number of switching devices as compared to classical topologies. Therefore it may present potential for application in high voltage/power apparatus. Also, the proposed topology exhibits configurational and functional similarity with the CHB topology in two ways: (i) isolated input DC voltages are required; and (ii) it offers the possibility of combining the input DC levels into all additive values. Therefore, the proposed topology can be employed for applications where CHB converters are implemented (e.g. in medium voltage drive applications where a phase shifting transformer with multiple secondary windings is generally employed mainly for the reduction of line-current distortion, thus providing isolated DC sources [9]).

II. Proposed structure of seven level inverter

A five-level inverter based on CCS-MLI topology is shown in Fig.1 (a). It consists of six power switches and two sources E_1 and E_2 such that $E_1 = E_2 = E$. The structure synthesizes five levels in the output viz. 0, $\pm E$ and $\pm 2E$. The CCS-MLI topology with the proposed 7 -level asymmetric source based MLI is shown in Fig.1 (b). The structure consists of six switches and two asymmetric dc sources. The configuration is such that $V_1 = V$ and $V_2 = 2V$. Various valid states for the structure are shown in Table I. It can be seen that seven levels are obtained in the output waveform; these levels are 0, $\pm V$, $\pm 2V$, $\pm 3V$.

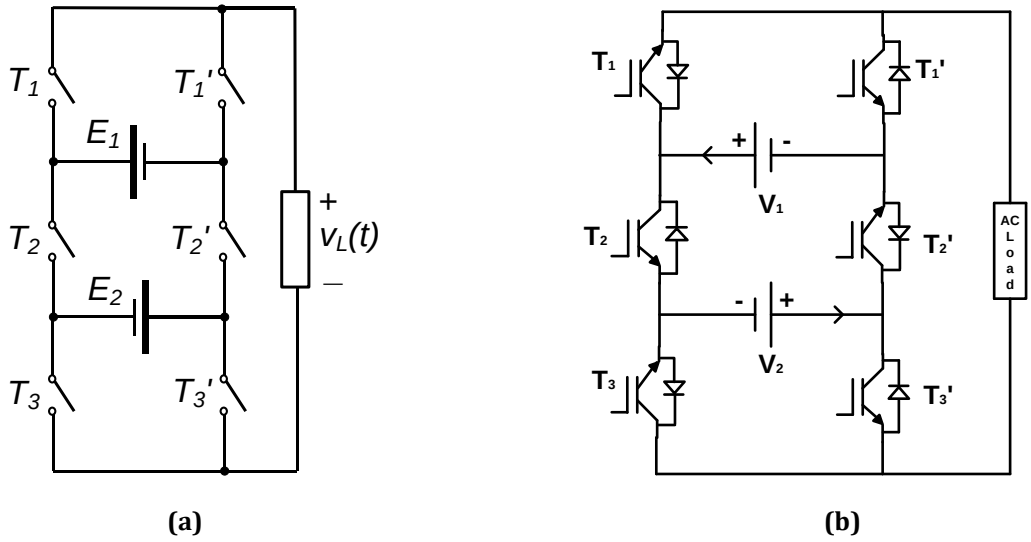


Fig.1 (a) A five-level CCS-MLI as proposed in [7]; (b) 7- level asymmetric source based MLI

Table I

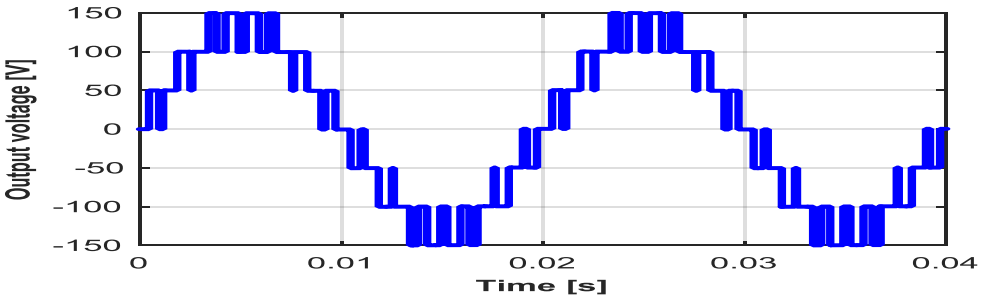
Valid switching states for the structure proposed in Fig.1 (b)

STATE	Output Voltage V_L (t)	ON state switches
1	0	T_1,T_2,T_3
2	0	T_1‘,T_2’,T_3’
3	V	T_1,T_2’,T_3’
4	2V	T_3, T_1‘,T_2’
5	3V	T_1, T_2’,T_3
6	-V	T_1‘,T_2,T_3
7	-2V	T_1,T_2, T_3’
8	-3V	T_1‘,T_2,T_3’

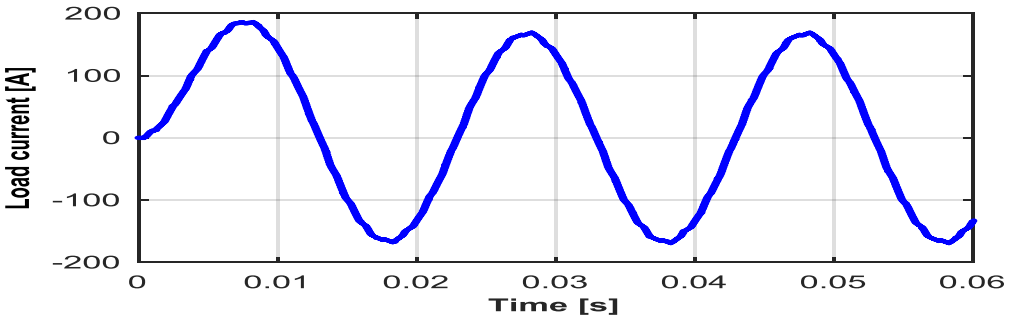
III. Simulation Study

In order to validate the functionality of the proposed structure, a simulation study is carried out using MATLAB/Simulink along with the SimPowerSystem tool. The circuit shown in Fig.1 (b) is modelled with V_1 = 50V and V_2 = 100 V. An RL load is considered at the output terminals with R = 2Ω and L = 5 mH. Since the structure is a 7-level inverter, a sine-triangle pulse width modulation (PWM) is administered with six carrier signals of 1000 Hz each and a sinusoidal reference signal of 50 Hz frequency. The so-called ‘universal control scheme’ as proposed in [8] is used to modulate the topology.

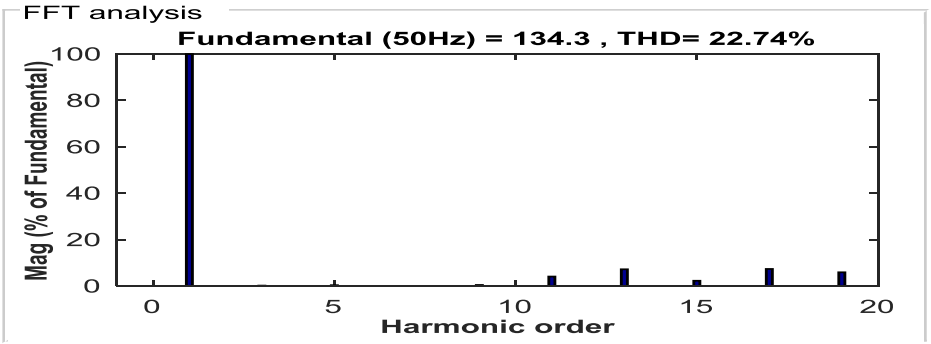
Simulation results are shown in Fig.2. The load voltage is shown in Fig.2 (a). It can be seen that it is a seven-level waveform of 50 Hz frequency. It consists of equal sized steps of 50V each. The load current waveform is sinusoidal and is inductive in nature as expected. Waveform exhibits total harmonic distortion (THD) of 22.74% without filter.



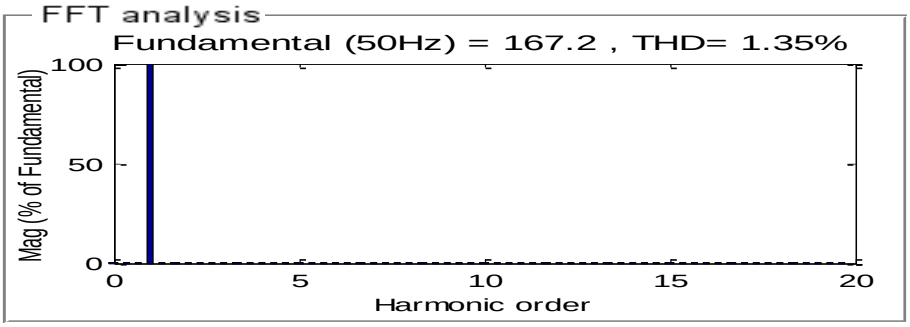
(a)



(b)



(c)



(d)

Fig.2 Simulation results for proposed 7- level inverter; (a) output voltage (b) its load current (c) THD for output voltage (d) THD for load current

IV. Conclusion

In this paper a new topology for seven- level inverter with switch level fault tolerance is proposed. It is a topology as various switches have different blocking voltages and it employs asymmetric source configuration for maximization of levels in the output waveform. In this paper a seven- level asymmetric source based MLI is proposed for the CCS-MLI topology for increased number of levels in the output. A multicarrier PWM scheme is introduced which helps to optimize the switching frequencies of various power switches with different voltage stresses. Working of the structure is shown with the help of a seven-level inverter. Simulation results based on MATLAB/Simulink are presented to validate the proposed concept.

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