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A NEW MULTILEVEL INVERTER TOPOLOGY FOR POWER APPLICATIONS

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Abstract - *Multilevel Inverter (MLI) has become popular in recent years for high power applications. But its major drawbacks are complex control circuitry and a large number of power devices required there-in. This paper proposes a novel multilevel inverter topology using a H-bridge output stage with three bidirectional auxiliary switches. This circuit configuration results in a significant reduction in the number of power devices and capacitors when compared to the conventional MLIs. In addition, the Total Harmonic Distortion (THD) generated by an MLI can greatly be reduced by Fuzzy Logic Control (FLC). Consequently the performance of the MLI is greatly enhanced*

Index Terms- H-bridge, MLI, FLC, Bi-directional Switches, THD.

1. INTRODUCTION

An MLI in a power electronic system is the one which yields the desired ac output voltage from a single dc input. With a large number of auxiliary switches, the inverter output voltage waveform approaches a nearly sinusoidal waveform using the fundamental frequency switching scheme. The various topologies presented in the literature as multilevel inverters [1] show some characteristics in common. The advantages of MLIs are

(i) The reduction in the voltages applied to the main power switches helps operation at elevated load voltages.
(ii) Reduced commutation frequency applied to the power components.
(iii) Limiting the transient voltage automatically.

The drawbacks associated with the multilevel configurations are

(i) Circuit complexity.
(ii) A large number of power switches required to be commutated precisely.

In the early years MLIs were used only in some high power applications such as high power motor drives in shipping industries, petro-chemical industrial applications, high voltage power transmission, power line conditioners etc. [2]-[11].

A single-phase inverter is usually used for low-power applications which are less than one kW. The output voltage waveform of a MLI is composed of voltages, typically obtained from capacitor voltage sources. Multilevel starts from three levels. As the number of levels reach very large, the THD in output approaches zero. The number of obtainable voltage levels, however, is limited by voltage unbalance problems, voltage clamping requirement, circuit layout and packaging constraints.
The proposed new H-bridge multilevel inverter topology has been developed from the generalized MLI configuration shown in Figure.1

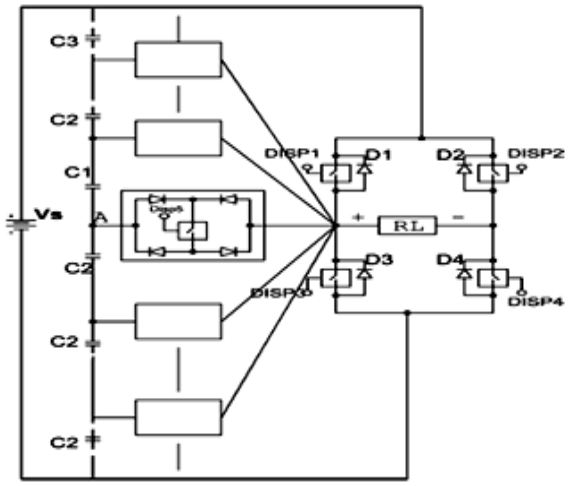

Figure. 1 Generalized multilevel inverter configuration of the new topology

The percentage reduction in the number of power switches compared to conventional H-bridge multilevel inverter is shown in Table 1

Table 1 COMPARISON BETWEEN TWO INVERTER TOPOLOGY AT FOUR DIFFERENT LEVELS

Inverter type		Cascaded	Proposed Topology	% Reduction
Number of switches	5-level	8	5	37.5
	7-level	12	6	50
	9-level	16	7	56.25
	11-level	20	8	60

This new topology has the advantage of less number of switching devices. It can also be extended to any desired number of levels. The block diagram of modes of operation of a nine-level inverter is presented in Figure 2 where similar modes can be realized for higher levels. The inverter operation is controlled using switching angles based on PWM with the help of pulse generator. These angles are achieved by solving the equations using the theory of resultants. The validity of the proposed topology and the harmonic elimination method are verified on MATLAB SIMULINK for nine-level inverter. This paper presents new topology of multilevel inverters using programmed PWM technique.

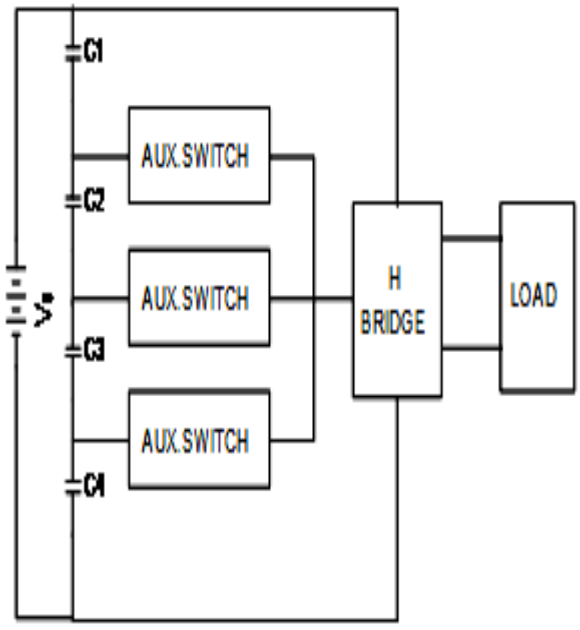

Figure. 2 Block diagram of a new nine-level H-bridge inverter topology

II. MULTILEVEL INVERTER TOPOLOGY

The single-phase nine-level inverter which was developed from the generalized inverter shown in Figure.1is presented in Figure 3. It comprises a single-phase conventional H-bridge inverter with three bi-directional switches. A capacitor voltage divider is formed by C_1, C_2, C_3, and C_4. The modified H-bridge topology is advantageous over other topologies, i.e., less number of power switches, less number of power diodes, and less number of capacitors for inverters of the same number of levels.

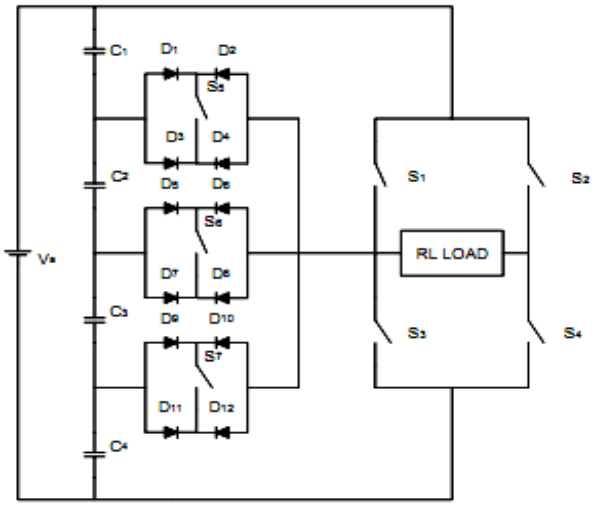

Figure. 3 Proposed nine-level H-bridge inverter topology

Proper switching of the inverter can produce nine output voltage-levels (1 0 0 % o f V_{dc}, 7 5 % o f V_{dc}, 50% of V_{dc}, 25% of V_{dc}, 0 , -25% of V_{dc}, -50% of V_{dc}, -7 5 % o f V_{dc}, -100% of V_{dc}) from the dc supply voltage.

The above inverter's operation can be divided into nine switching states. Table 2 shows the switching combinations that generate the required nine output levels (1 0 0 % o f V_{dc}, 7 5 % o f V_{dc}, 50% of V_{dc}, 25% of V_{dc}, 0 , -25% of V_{dc}, -50% of V_{dc}, -7 5 % o f V_{dc}, - 100% of V_{dc}). In this configuration the four capacitors in the capacitive voltage divider are directly connected across the DC bus and since all switching combinations are activated in an output cycle, the dynamic voltage balance between the two capacitors is automatically restored.

Table 2 SWITCHING COMBINATIONS REQUIRED TO GENERATE THE NINE-LEVEL OUTPUT VOLTAGE WAVEFORM

S_1	S_2	S_3	S_4	S_5	S_6	S_7	V_{out}
On	Off	Off	On	Off	Off	Off	V_{dc}
Off	Off	Off	On	On	Off	Off	$3V_{dc}/4$
Off	Off	Off	On	Off	On	Off	$V_{dc}/2$
Off	Off	Off	On	Off	Off	On	$V_{dc}/4$
On	On	Off	Off	Off	Off	Off	0
Off	On	Off	Off	On	Off	Off	$-V_{dc}/4$
Off	On	Off	Off	Off	On	Off	$-V_{dc}/2$
Off	On	Off	Off	Off	Off	On	$-3V_{dc}/4$
Off	On	On	Off	Off	Off	Off	$-V_{dc}$

III.FUZZY LOGIC CONTROL (FLC)

FLC is the evolution of a set of simple linguistic rules to determine the control action. In an FLC system there is no necessity for a plant model. The plant can be a single input, single output or multi-input, multi-output system. The configuration of FLC scheme is shown in Figure.4. The above FLC is composed of three parts such as fuzzification, inference engine, defuzzification etc which are described below.

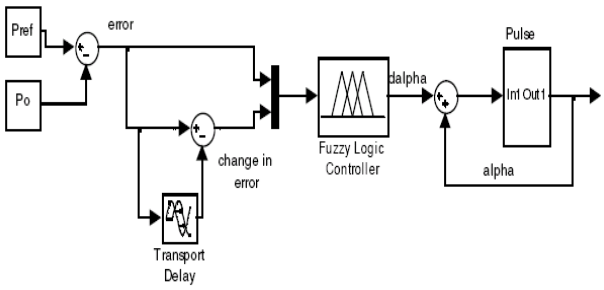

Figure 4: Configuration of Fuzzy Logic Controller (FLC)

FUZZIFICATION

To translate the values of error (e) and change in error (Δe) calculated by using sampling interval. The output from the FLC is the change in control signal (Δα). Triangular Membership Functions (TMF) is selected for all these variables. The membership functions of the each variables error (e), change in error (Δe) and change in control signal (Δα) are shown in Figure.4.1, Figure.4.2 and Figure.4.3 respectively.

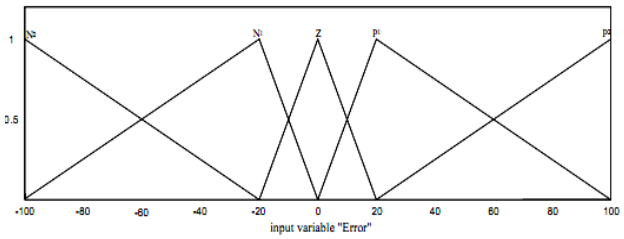

Figure. 4.1: Membership function for error (e)

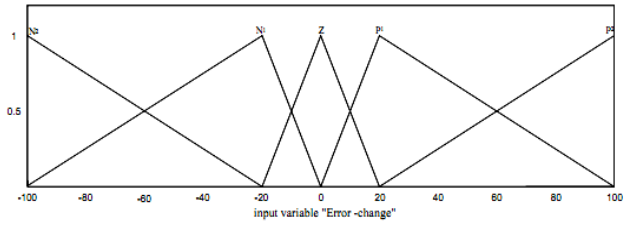

Figure. 4.2: Membership function for change in error (Δe)

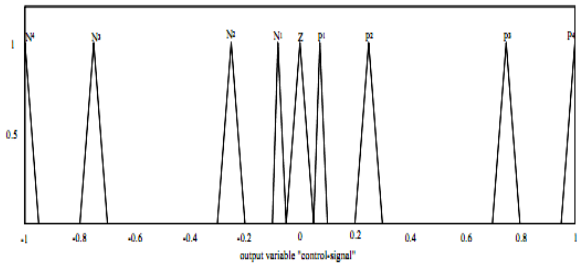

Figure. 4.3: Membership function for control signal (Δα)

INFERENCE ENGINE

Inference engine performs three tasks: applying fuzzy operator, implication method and aggregating all outputs. Inference engine mainly consists of two sub blocks namely, fuzzy rule base and fuzzy implication. The inputs which are now fuzzified are fed to the inference engine, and the rule base is then applied. The output fuzzy sets are then identified using fuzzy implication method. Table 3 shows the rule base of Fuzzy Logic Controller, where all the entries of the matrix are fuzzy sets of error(e), change in error(Δe) and change in control signal(Δα) to the inverter by using fuzzy implication method is min-max. The consequent fuzzy region has restricted the minimum (min) of the predicate truth while selecting output fuzzy set. The output fuzzy region is updated by taking maximum (max) of these minimized fuzzy sets during shaping of output fuzzy space.

Table 3 FUZZY MEMBERSHIP FUNCTION FOR PROPOSED FLC

Error (e) \ Rate of Change of error (Δe)	N_2	N_1	Z	P_1	P_2
N_2	N_4	N_4	N_4	N_3	Z
N_1	N_4	N_2	N_1	Z	P_3
Z	N_4	N_1	Z	P_1	P_4
P_1	N_3	Z	P_1	P_2	P_4
P_2	Z	P_3	P_4	P_4	P_4

DEFUZZIFICATION

The input for the defuzzification process is a fuzzy set, and the output is a single number. For the final desired output a non-fuzzy value of control, a defuzzification stage is required. In the proposed scheme bisector defuzzification method is used for defuzzification.

IV. MATLAB SIMULINK MODEL AND SIMULATION RESULT

The model was simulated for proposed configuration in MATLAB SIMULINK. A nine-level inverter model constructed in MATLAB SIMULINK software is shown in Figure 5. The new Fuzzy Logic Controller strategy uses reduced number of switches. This is the novel idea. The output waveforms and THD of the proposed model are presented in Figure 6 and 7 respectively.

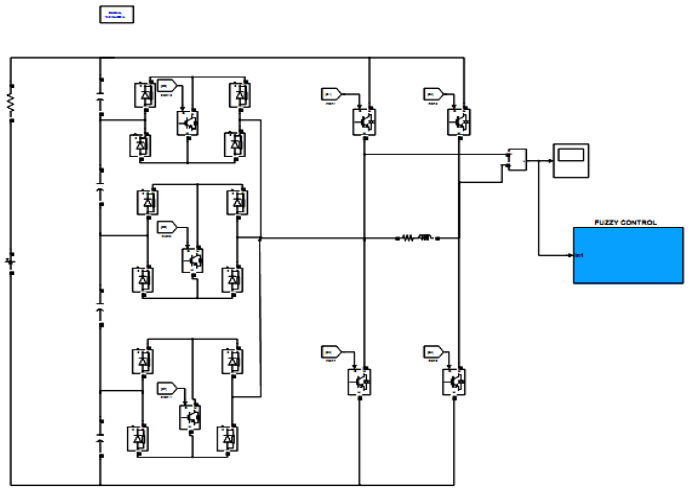

Figure.5 MATLAB SIMULINK model of proposed nine-level inverter

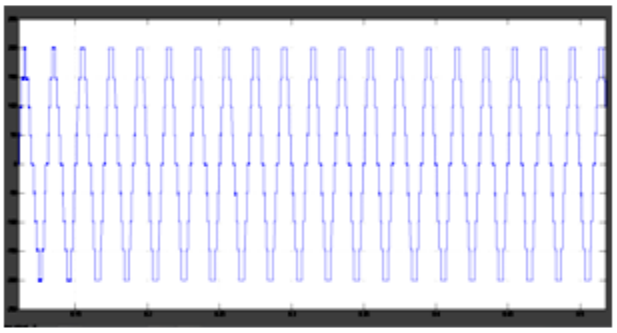

Figure. 6 output Voltage of nine-level inverter.

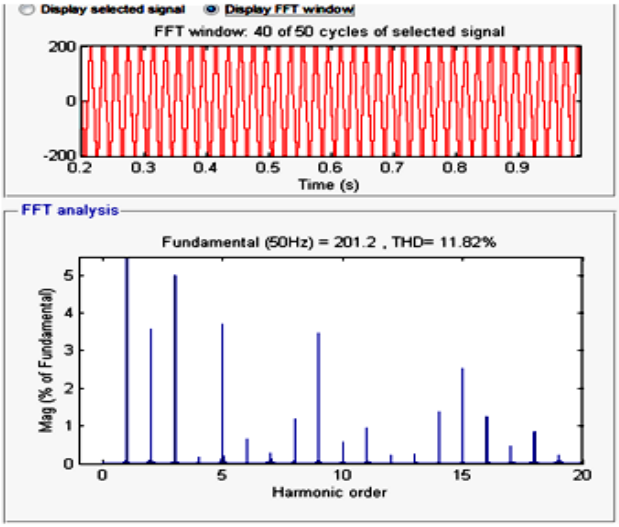

Figure.7 THD of simulated output

V. CONCLUSION

The above Multilevel inverter yields better output waveforms. They give lower THD. The simulated results show that the new multilevel topology with three bi-directional auxiliary switches performs better. The required nine level output is achieved using only seven power switches and four capacitors.

This configuration reduces the circuit complexity for low and medium power applications where standard MLI cannot compete with two-level configurations due to cost.

The working of the proposed MLI has been given in detail. Thus, the desired number of levels of the inverter's output voltage can be achieved. The THD is less in the nine-level inverter compared with that in the seven, five and three-level inverters.

A further development of the proposed topology can be

applied to any number of voltage levels with the power switches for maximum voltage, as shown in generalized multilevel inverter configuration.

BIOGRAPHIES

Mr. R.Venkatesh received the B.E. degree in Electrical and Electronics Engineering from Periyar University, Salem, India in 2004 and the M.E. degree in Embedded Systems in 2006 from Vinayaka mission university, Salem, India. Currently, he is working as Assistant Professor in Department of Electrical and Electronics Engineering, Annapoorana Engineering College, Salem and pursuing his Ph.D. in Anna University.

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