International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395-0056
Volume: 05 Issue: 06 | June-2018 www.irjet.net p-ISSN: 2395-0072

# DESIGN AND IMPLEMENTATION OF THREE PHASE GRID SIMULATOR

**Dr.Mathew K[1], Chaithra K S[2]**

*[1]HOD ECE Department, Mar Athanasius College of Engineering, Kothamangalam, Kerala, India*
*[2]M-Tech ECE Dept., Mar Athanasius College of Engineering, Kothamangalam, Kerala, India*

---

**Abstract -** *When Grid-connected systems are used they should experience scenarios like voltage sag, voltage swell, frequency variations, voltage unbalance etc. So it is necessary to test these systems under laboratory, then these scenarios do not exist and an almost stiff voltage source is obtained. But, in order to qualify the grid-connected systems, it becomes essential to test them under various grid disturbances which are mentioned earlier. The grid simulator is a hardware set up that can be programmed to generate typical conditions experienced by the grid-connected systems. It is basically an inverter that is controlled to act like a voltage source in series with a grid impedance. This paper describes the design and implementation of a three phase grid simulator. Control signal for the inverter module is given using Spartan 6 FPGA board with software implemented on Xilinx using Verilog code. Visual studio is implemented here in order to implement graphical user interface.*

***Key Words***: **Grid simulator, Three phase inverter, Spartan 6 FPGA board, Visual studio**

## 1. INTRODUCTION

With the increasing penetration of distributed generation (DG) and large-scale renewable energy systems like wind turbines or solar cells, more stringent grid codes have been issued to prescribe how those grid-connected systems to support the network during grid disturbances. For further development of grid-connected systems according to new grid codes and correlative standards, a hardware set up is necessary. Such a hardware set up is termed as grid simulator. Grid simulator is essential to design, test, analyze and verify the performance and characteristics of various grid-connected devices under different grid conditions in a laboratory [1].

The grid simulator is a high performance converter that can be controlled to act as an ideal voltage source, thus provide output voltage and frequency regulations to reproduce various grid disturbance such as voltage sag, voltage swell, frequency deviations and unbalance and so on. The grid simulator is a powerful tool to study the steady state and dynamic behavior of grid-tied systems, such as active filter and distributed generation interface converter, under various grid conditions.

In [2], a grid simulator for single phase systems has been discussed. Besides being limited to single-phase systems and primarily meant for testing of single phase distributed generation systems, the paper mainly focuses on the control of the inverter rather than the issues related to the grid simulator. In [3], there is a mention of a 250kVA grid simulator that is used to generate sag, swell and harmonic issues to test distributed generation systems. However, very little technical detail is available. In [4], laboratory grid simulator based on three-phase four-leg inverter is implemented. Employing the dual-loop control with capacitor current feedback and output voltage feed forward, the grid simulator output voltage could be precisely regulated at both steady state and dynamic development of FPGA. With the development of FPGA it is possible to use short sampling times for predictive control algorithms, being feasible the use of sampling time in a real system.

Here in this paper mainly focus on the implementation of grid simulator using FPGA.

## 2. METHODOLOGY

Grid simulator is used to simulate,test and prove the system performance.To emulate the grid faults high dynamic performance is essential to control the output voltage of simulator is necessary. As an example, during voltage faults ,the grid voltage may fall a millisecond range.In order to analse such faults a hardware want to be implemented.

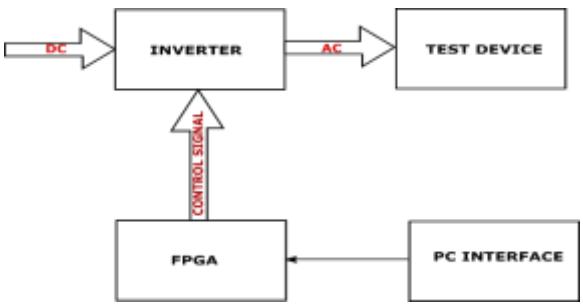


**Fig -1:** Block diagram of proposed system

Fig. 1 shows the proposed block diagram for the grid simulator. Three phase inverter is used as grid simulator. Device wanted to be tested is connected at the output side of the inverter module in order to test the device. The Inverter consists of MOSFETs as switching devices for which the gate pulses are given using a controller, FPGA. The pulses are generated by FPGA and then given to the switches. In order to make more reliable operation of the inverter module by preventing the interference from the control circuit i.e., FPGA, the use of main (inverter) and control circuit is isolated from each other. For this an optocoupler is used.

MOSFET driver IC used to amplify and isolate the switching signal which is given to the MOSFET devices. Due to the switching action of the power mosfet and non-linear characteristics of the semiconductors devices, harmonics present on the output of the inverter module. Thus to eliminate harmonics filters are used.

For user interface GUI is implemented using visual studio. There by various types of disturbances can created by controlling data from PC.

## 3. HARDWARE SET UP

Grid simulator is basically an inverter. Here three phase PWM inverter is used as simulator. Pulse width modulated inverters are the most widely used power-electronics for practical applications. These types of inverters are capable of producing AC voltages of variable magnitude as well as variable frequency. When compared with square wave inverters, the quality of output voltage almost better. There are several PWM techniques, differing in their methods of implementation. But all technique mainly focus on the generation good quality sinusoidal waveform of desired amplitude and frequency. Even though the output voltage must contain some amount of harmonics. Such a situation is acceptable in most cases as the harmonic voltages of higher frequencies can be satisfactorily filtered using lower sizes of filter chokes and capacitors.

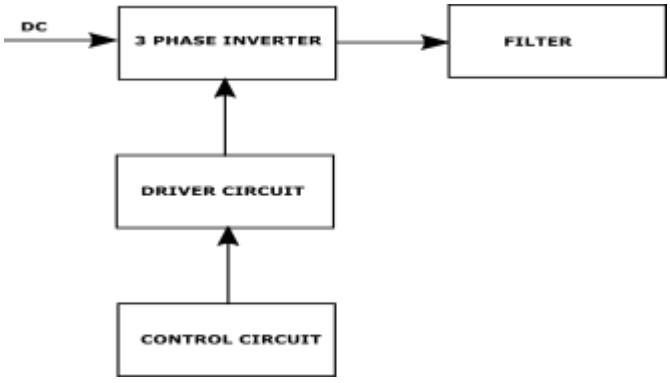


**Fig -2:** Block diagram of three phase PWM inverter

Here the switches of any leg of the inverter (S1 and S4, S3 and S6, or S5 and S2) cannot be switched on simultaneously because this would result in a short circuit across the DC link voltage supply. Similarly the switches of any leg of the inverter cannot be switched off simultaneously, to avoid undefined states in the VSI, and thus undefined AC output line voltages. Of the eight valid states, two of them (7 and 8 in Table 1) produce zero AC line voltages. In this case, the AC line currents freewheel through either the upper or lower components. The remaining states (1 to 6 in Table 1) produce nonzero AC output voltages. In order to generate a given voltage waveform, the inverter moves from one state to another. The selection of the states in order to generate the given waveform is done by the modulating technique that should ensure the use of only the valid states. Here STPWM is used as the modulation technique.

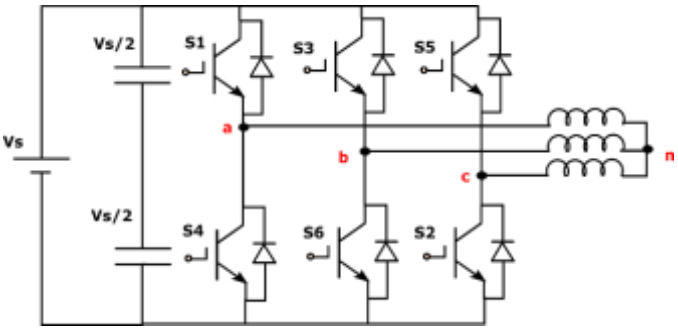


**Fig- 3:** Three phase inverter circuit

**Table -1:** Valid switch states for a three-phase VSI

| State | State | | | |
|---|---|---|---|---|
| 1, 2, and 6 are on and 4, 5, and 3 are off | 1 | | 0 | |
| 2, 3, and 1 are on and 5, 6, and 4 are off | 2 | 0 | | |
| 3, 4, and 2 are on and 6, 1, and 5 are off | 3 | | | 0 |
| 4, 5, and 3 are on and 1, 2, and 6 are off | 4 | | 0 | |
| 5, 6, and 4 are on and 2, 3, and 1 are off | 5 | 0 | | |
| 6, 1, and 5 are on and 3, 4, and 2 are off | 6 | | | 0 |
| 1, 3, and 5 are on and 4, 6, and 2 are off | 7 | 0 | 0 | 0 |
| 4, 6, and 2 are on and 1, 3, and 5 are off | 8 | 0 | 0 | 0 |

## 4. IMPLEMENTATION METHODOLOGY

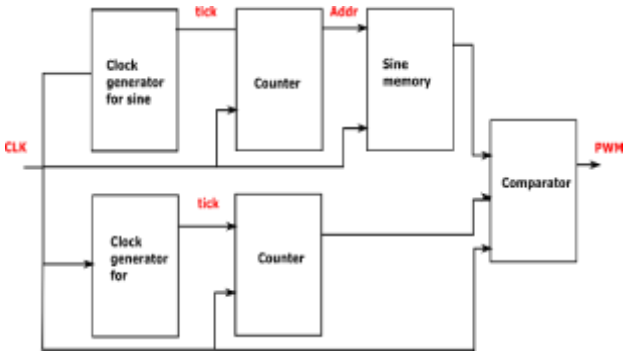


**Fig -4:** Architecture of the proposed SPWM generation unit

PWM signal for the power mosfets are generated using controller, Here FPGA is used as the controller. Fig 4.1 shows the Architecture of proposed SPWM generation unit. The clock generator subsystem takes input, FPGA input clock 50 MHz and produces a new clock signal used by the digital circuits of the proposed SPWM generator. Based upon the new clock signal corresponding sine wave and triangular wave has to be generated. Comparing message signal (sine wave) with carrier (triangular wave) gate signal for the inverter module is generated. Comparison is done by the comparator module.

In order to provide PC interface UART receiving section has been implemented. The receiver can retrieve the data bits only by using the predetermined parameters such as baud rate, parity bits etc.. We use an oversampling scheme to estimate the middle points of transmitted bits and then retrieve them at these points accordingly.

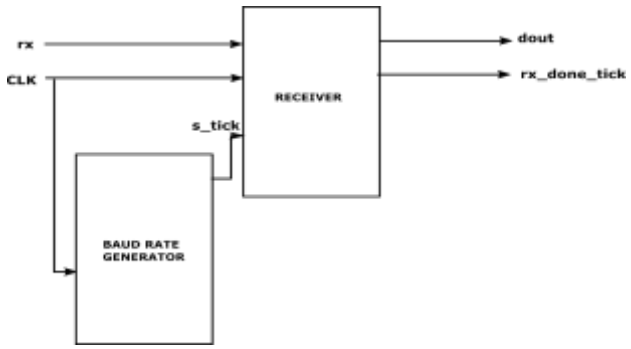


**Fig -5:** UART receiving subsystem

The oversampling scheme basically performs the function of a clock signal. Instead of using the rising edge to indicate when the input signal is valid, it utilizes sampling ticks to estimate the middle point of each bit to be transmitted. While the receiver has no information about the exact onset time of the start bit, the estimation can be off by at most 1/16. The subsequent data bit retrievals are off by at most 1/16 from the middle point as well. Because of the oversampling, the baud rate can be only a small fraction of the system clock rate.

## 5. EXPERIMENT RESULTS

Fig. shows designed grid simulator set up and it allows users to vary relevant parameters in order to simulate real world grid environments and conditions. Supported variations include frequency, phase angle, voltage amplitude, voltage drops in either single or three phase modes. Unbalanced three phase conditions can easily be simulated. It consists of FT232 module for serial communication with PC. GUI is developed using visual studio.

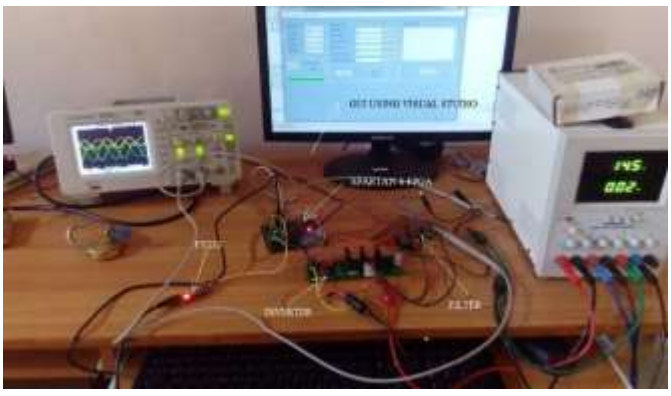

**Fig -5:** grid simulator

Fig. Shows the voltage unbalance condition. Her one of waveform has peak to peak voltage is 9V. Vpp of other wave is scaled in order to create voltage unbalance condition. This disturbance is created by scaling the output of Block rom in the required amount.

**Fig -6:** Voltage Unbalance

Fundamental sine wave has frequency equal to 50Hz. Here 54Hz sine has to be generated. By using this grid simulator we can create sine waves having frequency ranging from 32 to 127 Hz. It is depending on the duration of tick from the clock generation module for the generation of sine wave.

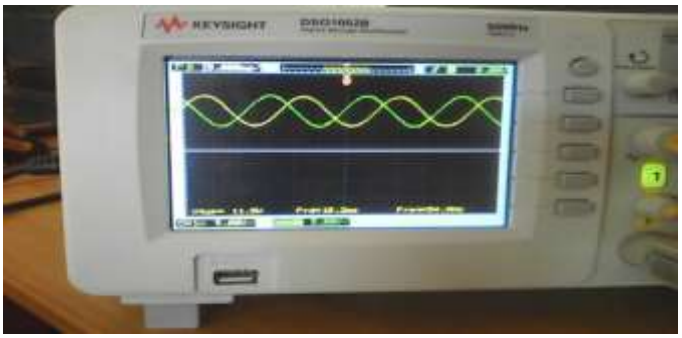

**Fig -7:** Frequency Variation

Phase miss and phase angle adjustment are the other two types of disturbances which can also be created by designed grid simulator. Fig 8 and Fig 9 are corresponding to phase miss and phase angle adjustment respectively. Phase miss is obtained by making gate signal to the corresponding mosfet to zero. Phase angle adjustment is obtained by changing the initialization of address.

Harmonic distortion is the presence of frequencies in the output of a device that are not present in the input signal. In an ideal system, the fast Fourier transform (FFT) of a sinusoid would result in a single peak at a specific frequency. However, in real-world systems, non-linearity and noise result in imperfections.

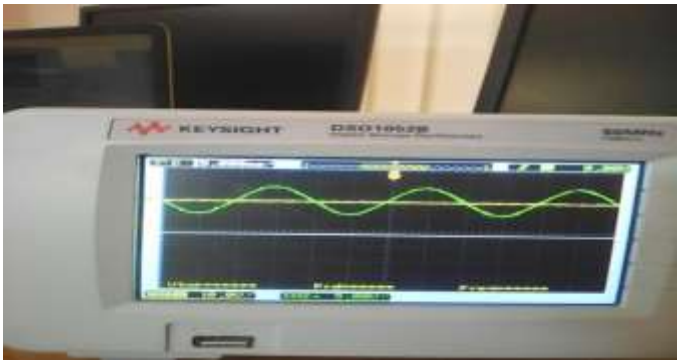

**Fig -8:** Phase miss

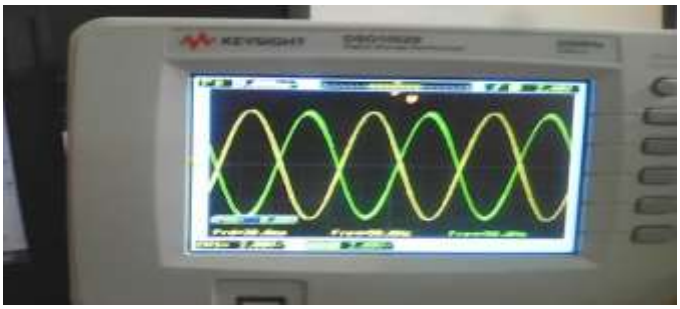

**Fig -9:** Phase angle adjustment

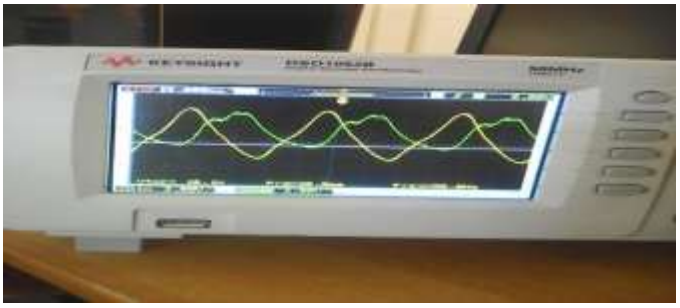

**Fig -10:** Harmonic distortion

Fig. 10.10 shows harmonically distorted waveforms. One is corresponding to third harmonic and other is correspond to fifth harmonic. These waveforms are generated by adding sine wave with another sine wave which has frequency equal to the nth times of fundamental frequency.

Within this GUI we can set comport, baud rate, data bits, stop bits and parity bits. The parameters frequency, amplitude, phase angle, no.of phases and harmonic order and frequency can be controlled. Here baud rate is selected as 19200. So the baud rate generator corresponding to 19200 is developed by using FPGA. Fig shows the GUI created using visual studio for providing user interface. We can set various values for baud rate (i.e., 2400,4800,14400,19200,9600 etc.). OPEN and CLOSE button are used to open and close the comport. Status of the comport is displayed on the Comport status group box. Send Data button is used to send data. Decimal to binary conversion or vice versa is performed using radio button change.

We can provide amplitude, phase angle and harmonic order of each phase separately. For this separate group box for amplitude, phase angle and harmonic order can be created using group box icon from toolbox. Each phase values can be set within the group box. Save button can be used to save the values of three phases to the corresponding textbox within the transmitter control portion. After saving the values using save button we can close the group box using close button.

**Fig -11:** GUI created using visual studio

## 6. CONCLUSION

The grid simulator is a useful and essential hardware that is required for the design, test and analysis of grid-connected devices. In this paper, a laboratory grid simulator based on three-phase PWM inverter is designed and implemented. FPGA is used as the controller here. There by it providing high switching frequency. The experiment results illustrate that the grid simulator is able to reproduce representative grid disturbance such as frequency deviation, harmonic distortions, and voltage unbalance and phase angle adjustment. User selectable three, two or single phase outputs cane be generated using implemented grid simulator.

## REFERENCES

[1] Arun Karuppaswamy B, Vinod John “A Hardware Grid Simulator to Test Grid-Connected Inverter Systems”.

[2] Richard Zhang, Mark Cardinal, Paul Szczecin and Mark Dame, “A Grid Simulator with Control of Single-Phase Power Converters in D-Q Rotating Frame”, IEEE, 2002, pp.1431-1436.

[3] Eloy-Garcia, 1. C. Vasquez, and 1. M. Guerrero, "Grid simulator for power quality assessment of micro-grids, " lET Power Electronics, vol. 6, pp. 700-709, 2013.

[4] R. Lohde and F. W. Fuchs, "Laboratory type PWM grid emulator for generating disturbed voltages for testing grid connected devices," in Power Electronics and Applications, 2009. EPE '09. 13th European Conference on, 2009 pp. 1-9.

[5] P. Sharath Chandra1, J.Praveen2, A.Vinay Kumar3 "Design and implementation of three phase inverter fed to drive three phase motor" International Journal of Research in Engineering and Technology.

[6] L. Tianqi, W. Danwei, and Z. Keliang, "High Performance Grid Simulator Using Parallel Structure Fractional Repetitive Control, " IEEE Transactions on Power Electronics, vol. 31, pp. 2669-2679, 2016.