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POWER EFFICIENT IMPLEMENTATION OF ASYNCHRONOUS COUNTER USING INTELLIGENT CLOCK GATING

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Abstract – *In the present field of low power design technology, it is very essential to reduce the clock power as more than 40% of the power dissipation of the circuit is due to the clock variations. Various techniques for power reduction exist at the gate level abstraction. The most effective one out of all is the clock gating technique. This technique uses the enable conditions which are attached to the registers to gate the clocks. In this paper, the power reduction of Very Large-Scale Integration (VLSI) sequential circuits is achieved by the technique of intelligent clock gating. The main concept of clock gating is to provide clock transition to a circuit or segment when it needs to toggle or shift a data and avoid unnecessary clock transitions. This clock gating technique has to be applied to every block in the design which would lead to more power consumption due to the added logic instead of reducing the power. So, this intelligent clock gating technique will minimize the power consumption such that the performance of the circuit is not hampered.*

Key Words: **Low power design, Very Large-Scale Integration, Gate level, Sequential Circuits, Intelligent clock gating, Clock transition**

1.INTRODUCTION

In the earlier days, the clock gating technique has been used exhaustively for each block of the high frequency sequential circuits. Since the number of transistors on the chip have been increasing exponentially, the tradeoff comes in the form of increased area and power consumption. So, higher level techniques such as clock gating, power gating with sleep modes had been introduced. But applying clock gating for every block in the circuit becomes too cumbersome and because of increased package density, it has become a tedious task to manually verify the power at each block. So, this intelligent clock gating technique in the Xilinx Vivado will perform the clock gating on the entire design and doesn't change the predefined logic of the overall circuit design. This also maintains the timing constraints. This technique can be applied to Xilinx series such as Virtex(6,7), Spartan(6), Zynq-7000 AP SoCs. The above-mentioned technique has been performed and verified on Zynq board. This technique uses Chip enable to block the uninfluential signals from advancing towards the corresponding design segments and hence reducing the power consumed.

For some of the System on Chip designs, the paths would be driven by multiple clock sources (one clock and gated clock), There may be a chance that data from the clock will reach faster than the clock created by gated logic. This will create the race around conditions and also leads to Timing constraints violation. In such type of Soc designs to remove the race conditions, the base clock has to be separated and gating from the gated clock. Then the separated base clock has to be routed to the clock and gating to the clock will enable the sequential elements. While clock is OFF, every sequential element will be disabled and when the clock is ON, sequential elements will be enabled. [4]

Synopsys Inc. [4] explains about problems arising in some of the SOC designs due to clock gating. It also explains how to overcome the race around condition and clock skew constraints. Gary K Yeap. [5] gives an introduction to the concept of low power VLSI design. The concept of power reduction using various techniques at different abstraction levels, and also the tradeoff between area and power have been explained. This also references the clock gating technique for power reduction. Samir Palnitkar. [2] introduced the basics of Verilog hardware description language at gate level and behavioral level abstraction. J Bhasker. [3] depicts various implementations of the design using Verilog hardware description language. Priya Singh et al. [1] mentioned the technique of intelligent clock gating and gave a brief introduction. A white Paper from Xilinx. [6] gives a precise overview of intelligent clock gating technique and also explains the design flow of the technique. Jitesh Shinde et al. [7] explains about the technique of power optimization for VLSI circuits. It also explains about the challenges encountered when implementing intelligent clock gating technique for power reduction.

In this paper, the few above limitations faced during the implementation and the tradeoffs encountered have been precisely tackled with a systematic approach. Firstly, the design flow is explained and then the need for clock gating is also explained. An asynchronous counter is built on Xilinx Vivado Design Suite and the intelligent clock gating technique is applied for this corresponding circuit. It is further simulated on Xilinx Vivado and the power consumption with and without intelligent clock gating are compared and discussed.

2. TECHNICAL STUDIES

2.1 Need for Clock Gating

Clock Tree is an important part of Placement and Routing step in the Design flow. Hence the efficient usage of clock gating, clock architecture, Implementation is good for optimizing the power. Here the Clock-gating efficiency becomes more important. To get the good clock-gating efficiency we have to first maximize the effect of gating to reduce the idle power and secondly minimize ungated part of the clock-tree.

2.2 Design Flow

The basic design flow begins with opening a new project in the Xilinx-Vivado tool and writing the RTL design code in Verilog Hardware Description Language [2]. Then, the Zynq-7, spartan-6, kintex-7, virtex-6,7 boards are chosen depending on the required application. RTL Simulation, Synthesis and Implementations are done to get the optimized power output.

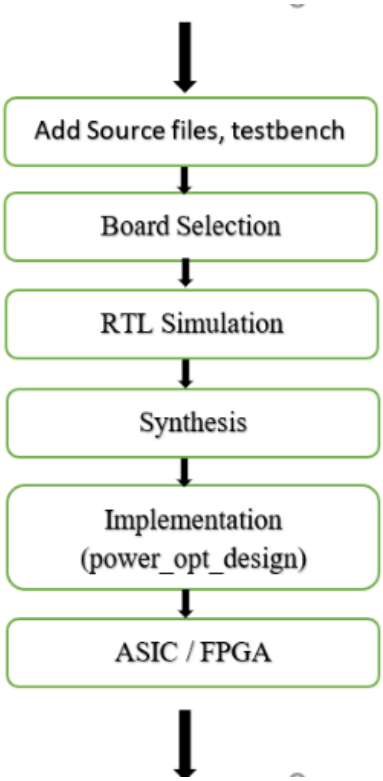

Fig-1: Flow Chart

2.2 Asynchronous Counter

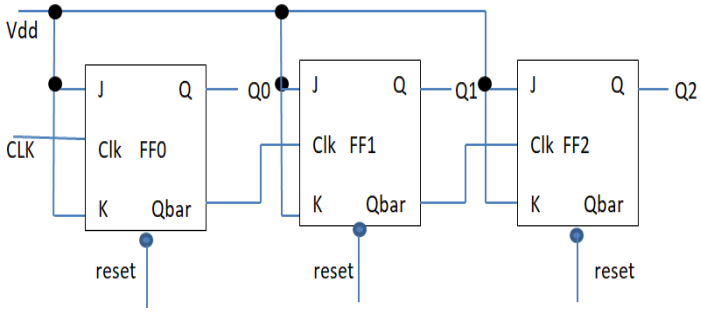

Fig-2: Circuit

Q0	Q1	Q2
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

Fig-3: Truth Table

This paper demonstrates power reduction implementation on a simple asynchronous counter with reset which counts from 0 to 7. It's very important to apply the Clock gating efficiently to this basic block as it is used in wide range of applications like Timers, Alarm Clock etc. it can be used also as a clock divider. Most of the time, the on-chip devices of the processor work at low frequencies than chip frequencies, which in turn will help in reduction of power dissipation.

2.3 Power Analysis

$P = C \times V^2 \times f$--- expression for Power dissipation [5]

P - dynamic power dissipation
V - supply voltage
f - frequency of operation (switching activities)

Power consumption in CMOS can be modeled as switching activities, overall capacitance and square of the supply voltage. Supply voltage is mostly fixed because performance of the MOSFET's get slower as we decrease the supply voltage. Capacitances also cannot be decreased because it will be difficult at the physical level abstraction where material and process technology have to be reviewed. [5]

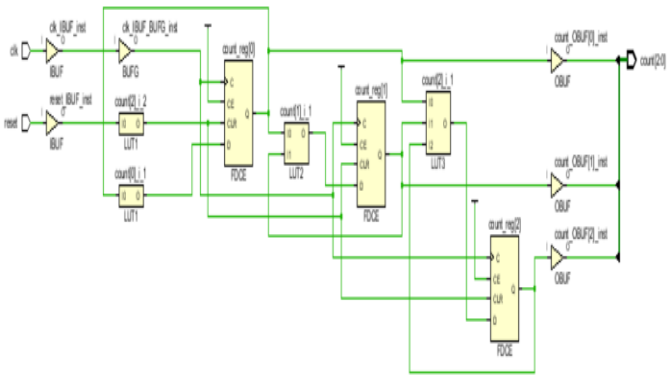

Fig-4 Schematic from Vivado

Xilinx Vivado for the Zynq boards provides the option of reducing the power at the logic level with the help of unique technique of intelligent clock gating. This study uses the ZYNQ-7 Board for further implementation.

2.4 Power Optimization Using Intelligent Clock Gating on Vivado

Generally, Power Dissipation is categorized as Static and Dynamic. FPGA consists of billions of transistors modeled as tiny capacitors. The power is consumed when it is switched on, this consumption is called Static power dissipation. We can modify only switching activity of the design by adding gating logic that will turn off the unused portions in the design. This is almost an impossible task for most of the complex designs. Vivado performs the intelligent Clock gating by finding sequential elements that do not contribute to the clock cycle. Clock-Enables and Port-Enables are appropriate to prevent unnecessary switching on the Registers and Flip-flops.

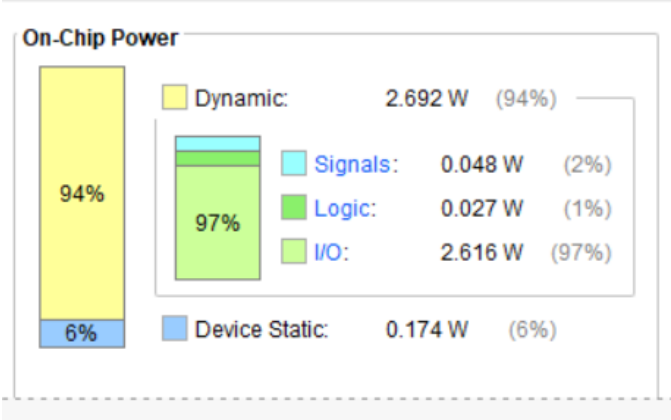

Fig-5 Power Analysis with Intelligent Clock Gating

The original Functionality remains unchanged. Pre-placement optimization will lead to maximal savings of the power. However, it is possible that timing of the circuit could be affected. The post placement optimization will ensure that they will not lead to timing violations. Vivado offers the flexibility to optimize the entire design or portions of the design. [7]

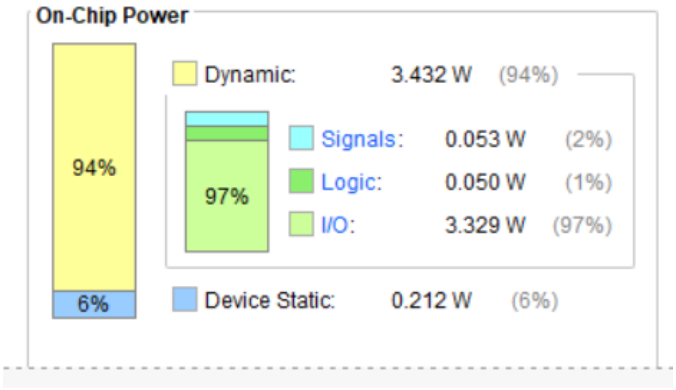

Fig-6 Power Analysis without Intelligent Clock Gating

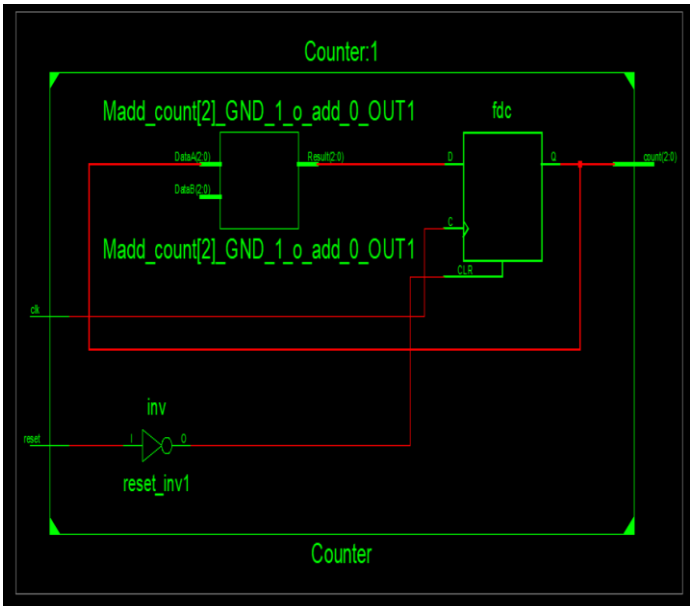

Fig-7 RTL Schematic

Fig-5 shows the power analysis with intelligent clock gating which has dynamic power of 2.692W. Fig-6 shows the power analysis without intelligent clock gating which has dynamic power of 3.432W.

Device Utilization Summary (estimated values)			[-]
Logic Utilization	Used	Available	Utilization
Number of Slice Registers	3	30064	0%
Number of Slice LUTs	4	15032	0%
Number of fully used LUT-FF pairs	0	7	0%
Number of bonded IOBs	5	250	2%
Number of BUFG/BUFGCTRL/BUFHCEs	1	16	6%

Fig-8 Device Utilization Summary

In normal register-transfer level (RTL) coding for counter related applications, one tries to use multiplexers, gates, buffers wherever required which includes lots of redundant logic. But the use of Intelligent clock Gating will introduce the clock enable signal wherever necessary. This technique shows the power reduction of 21.57% for the normal basic counter (without clock gated) simulation.

2.5 Challenges

During intelligent clock gating, the area increases since it will include the clock enable signals and their corresponding logic. The computation of such designs may consume a large amount of time to be evaluated and decide the logic for enable signals. This increases the computation time which can be overcome in the future by precomputing and storing the gating logic.

3. CONCLUSIONS

In this paper, the drawbacks of using the manual clock gating techniques have been tackled successfully. This is achieved by implementing the intelligent clock gating technique on an asynchronous counter resulting in a power reduction of 21.57% of the general asynchronous counter. And also, as mentioned above, it can be applied to various other circuits to achieve better power reduction. This amount of power reduction is very significant in the field of Low Power VLSI Design as it also successfully accomplishes to reduce the manual computation time and the timing constraints of the design.

Since the evolution of consumer electronics, the time to market has been reducing rapidly because of many automation techniques used by the manufacturing industries. The technique discussed in this paper paves way for improving the above constraint in a systematic approach.

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