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Design and Implementation of 6T FinFET SRAM Cell Using SVL Technique

Shyam Sundar Sharma[1], Nikhil Saxena[2]

[1]*Scholar Dept. of ECE, ITM, Gwalior, India*
[2]*Assistant Professor, Dept. of ECE, ITM, Gwalior, India*

Abstract - *As technology continues to scale down, leakage power has become a significant component in chip design. Leakage power is a key parameter to design low power devices because it is an important source of total power consumption. Large amount of leakage power is an issue of serious concern in portable electronics devices. Limited energy consumption in multimedia requires very low power circuits. Static Random Access Memory (SRAM) comprises a considerable proportion of the total area and total power for almost all VLSI chips as cache memory for the System on Chip (SOC) and it is expected to increase in the future in both handy devices and high-performance processors. By using low-power FinFET based SRAM cell, we can achieve higher steadfastness and longer battery life for handy application. In this paper, we have proposed a SVL technique and implemented it on FinFET based 6T SRAM cell and compare the performance, working and simulation results of FinFET based 6T SRAM and SVL technique implemented FinFET based 6T SRAM. By simulating and performing operations, we confirmed that our proposed technique reduces the power dissipation significantly in stand-by mode. All the simulations have been carried out on cadence virtuoso tool at 45 nm technology.*

Key Words: SRAM, FinFET, SVL, Leakage current, Static Power dissipation.

1. INTRODUCTION

As technology reaches sub nanometer regime, it requires a very high channel doping concentration to preserves from various Short Channel Effects (SCE) and heavy super-halo implanted by surface leakage currents. Due to the scattering of impurity in heavily doped regime, mobility and high transverse electrical field also be decreased in the 'on' mode of the device, weaken the sub-threshold swing and increased the parasitic junction capacitance [1]. FinFET is the best suitable device for minimizing the leakage power and improving stability for the SRAM cell. FinFET based SRAM cell. For reducing the leakage power, Fin height and threshold voltage can be optimized in the FinFET based SRAMs cell [2]. However, lowering the supply voltage has a strong negative impact on the SRAM cell performance under the influence of parametric variation. It necessitates a device level implementation on FinFET device to optimize the standby leakage power and the performance in the SRAM circuit. At 45nm node, Bulk MOSFET memory cell design is the challenging task by incremented Short Channel Effects (SCE) and sensitivity to parameter variations It is evident that the size of FinFET device affects the performance and the power dissipation of the memory circuit [3] .So it. is very difficult to design the optimized circuit.

As the challenges posed by continued technology scaling, FinFET device has been planned as an alternative for any other semiconductor devices used as on sub 45nm technology. These FinFET devices consist of a thin silicon body that is wrapped by gate electrodes. In FinFET devices the channel is shaped vertical to the plane of the wafer and current flows parallel to the wafer plane [4]. So the FinFET device is termed as quasi-planner device. There are some types of FinFET devices architecture were implemented. In shorted gate FinFET (SG-FinFET) device, the two gates are shorted together, resulting in a three terminal devices. This is the best replacement of the convention silicon based CMOS devices. In Independent gate FinFET (IG-FET) device, the top part of the gate terminal etched out, gives two independent gate terminals, as these two gates controlled individually. FinFET device is the most prominent candidate at sub 45nm technology as it reduces various short channel effects and low parameter variability [5]. FinFET is used to design various memory circuits on nano scale level that require low static power dissipation and adapt to the environmental conditions. In addition, FinFET device based SRAM cell offers better switching speeds and superior noise margins as well.

2. Design Of Conventional 6T FinFET SRAM Cell

Traditional engineering of 6T SRAM cell comprises of two cross-coupled inverters and two access N-MOS transistors appeared in Figure 1.

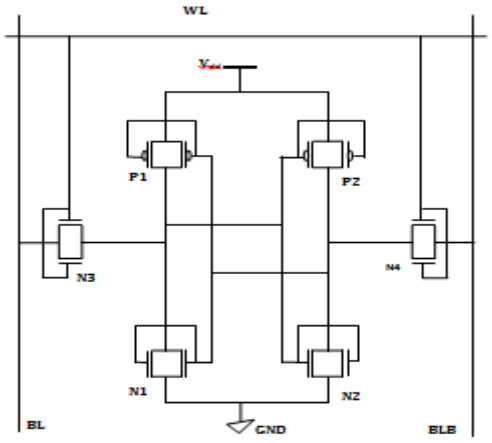

Fig -1: FinFET based 6T SRAM Cell

These cross-coupled inverters are named as latches. The two cross-coupled inverters have four transistors (P1, P2, N1, and N2); each bit in a SRAM is stored on these four MOSFETs. Source terminals of both access N-MOS transistor (N3 and N4) are associated with the Bit Line (BL) and Bit Line Bar (BLB). At the point when the word line is low, access N-MOS transistor is OFF and Bit lines (BL and BLB) are disconnected from the latch. In this situation, the latch can hold the bit as long as the voltages stay at VDD and GND. At the point when the word line is high, access N-MOS transistor is ON and Bit lines (BL and BLB) are associated with the latch. The capacity of these bit lines is to exchange the information for both write and read operation. The bit lines (BL and BLB) utilized as a part of the SRAM cell to act as I/O buses. It conveys the information bit from SRAM memory cell to the sense enhancer circuit.

2.1 6T FinFET SRAM Cell Operations

SRAM cell works in three distinct modes of operation.

2.1.2 Hold Operation

In the event that the word line is not empowered (WL=0), the access FinFET transistors (M5 and M6) detach SRAM cell from bit line (BL) and bit line bar (BLB). The two cross-coupled inverters frame latch by M1-M4 continues to strengthen one another as long as they are associated with the supply voltage (VDD). The current flow during this point from the VDD is known as leakage current.

2.1.1 Write Operation

To perform either of the operations the access FinFET transistors (M5 and M6) should be initiated first. For this, we should pull the word line high (WL=T) to initiate the access transistors (Ml and M2). Now we can perform the write operation. The desired information to be written is given to bit line (BL) and its complement is connected on bit line bar (BLB). That implies in the event that we need to write '1' to SRAM cell, we should give '1' to bit line (BL) and '0' to bit line bar (BLB). This would roll out the cell to vary its state consequently once the condition of the latch is changing the word line is deactivated (WL='0') an in this manner the desired information is written to the cell.

2.1.3 Read Operation

In almost the same way, to read the data from the SRAM cell, the word line is first declared to high (WL=1) that initiates the access FinFETs (M5 and M6) to access the latch. Now to carry out read operation, each of the bit lines are pre-charged to VDD. Now one of the bit lines would stays pre-charged and the other would be released to the ground, contingent upon the condition of the latch. Hence, if bit line (BL) stays charged, the bit line bar (BLB) should be discharged or vice versa as the case may. At this point both the bit lines are applied at the inputs of sense amplifier that finally gives the information related to stored bit by amplifying the data to a considerable level.

3. Self controllable voltage level (SVL) Circuit

SVL is simply the acronym for Self controllable Voltage Level. SVL strategy is utilized to decrease leakage current for the term of standby mode of operation i.e., whenever clock is 0 [8]. For pull up network SVL technique uses two NMOS and one PMOS transistors, two NMOS transistors which are connected in series are connected with one PMOS transistor in parallel. Similarly in pull down network two PMOS transistors which are connected in series are connected with one NMOS transistor in parallel. Clock signal is appended to pull down transistor gate terminal and Pull up transistors gate is associated with complement of clock. This way to deal with decrease leakage power makes use of a clock signal as the manipulate signal to govern supply voltage.

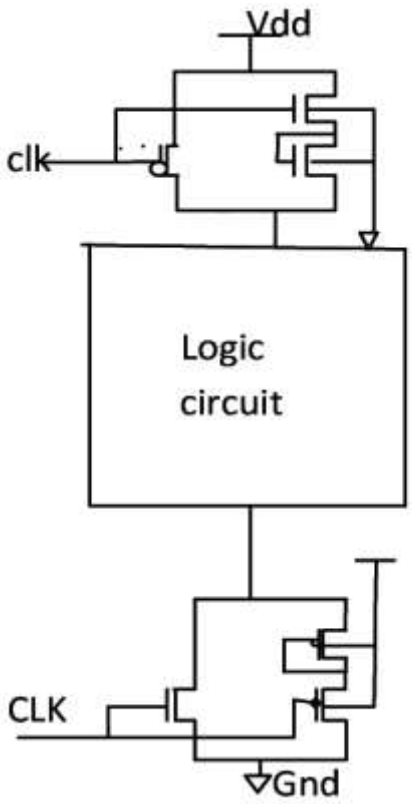

Fig -2: SVL circuit

3.1.1 SVL Technique Employed FinFET Based 6T SRAM Cell

Self controllable voltage level (SVL) is power switch procedure for leakage reduction within the device. SVL is a technique in which switch can be set either at the top of the cell, the bottom of the cell or can be placed on both top and bottom simultaneously [9]. USVL technique is applied to decrease the supply voltage and LSVL system is utilized to boost the ground node voltage. In USVL+LSVL system both techniques are used in FinFET based 6T SRAM cell as a result of that supply voltage gets decreased and at the same time ground node voltage is raised which prompts better outcomes in reducing leakage current, leakage voltage and leakage power.

Switches get turned on and off according to the input signal given to clock (CLK) which acts as a kind of control signal in active mode. In USVL system when CLK is 1, PU1 gets turned off and NU1, NU2 gets turned on weakly as a result of which VDD is provided directly throughout weakly ON switches and likewise in LSVL system CLK is 0, PL1, PL2 are turned ON weakly and NL1 gets OFF as a result of that VSS is supplied to standby SRAM.

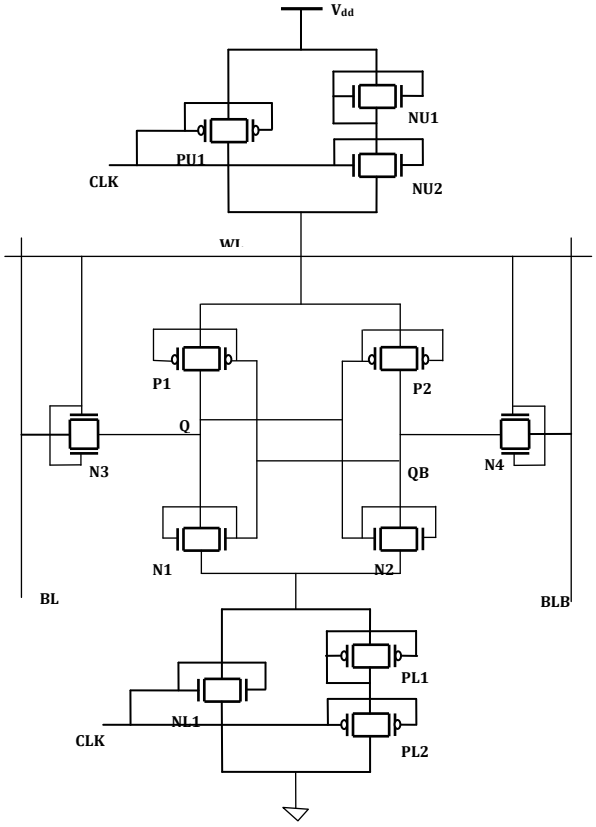

Fig -3: SVL Technique employed FinFET based 6T SRAM Cell

4. RESULTS

The simulation of circuits having SVL technique employed FinFET based 6T SRAM as its basic unit cell has been done in cadence virtuoso tool at 45 nm technology. The leakage parameter of SVL technique employed FinFET based 6T SRAM cell has been calculated at different supply voltages of 0.6V, 0.7V, 0.8V and 0.9V. In figures the simulated Leakage Current and Leakage Power waveform of FinFET based 6T SRAM cell and simulation for reduced Leakage Current and Leakage Power waveform through SVL technique are shown.

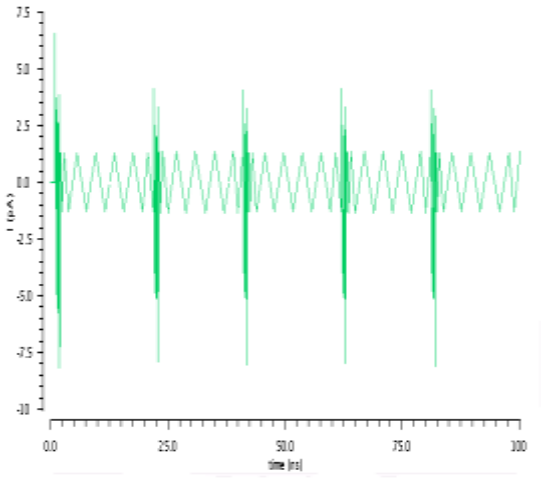

Fig -4: Leakage current of FinFET based 6T SRAM cell

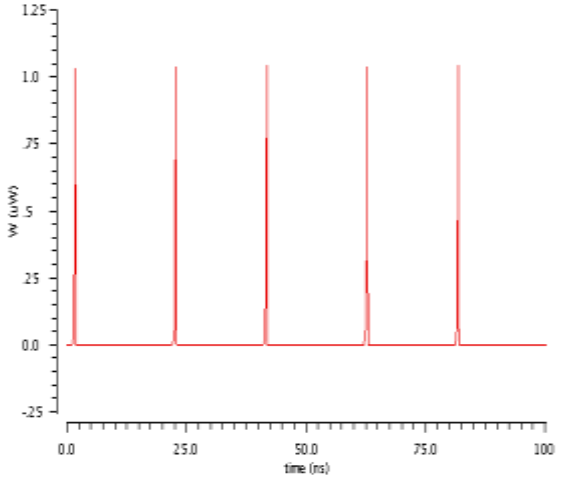

Fig -5: Leakage Power of FinFET based 6T SRAM cell

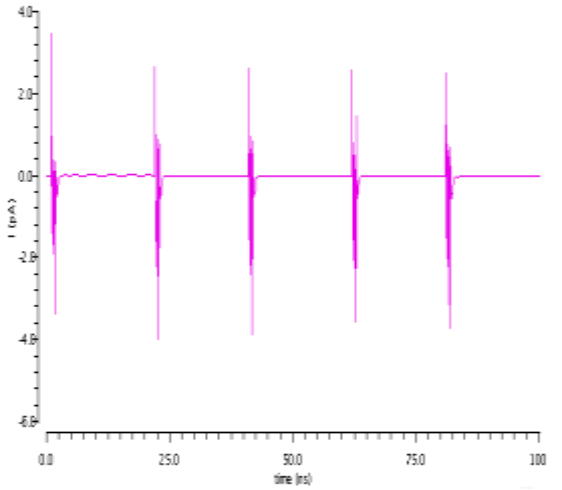

Fig -6: Leakage Current of FinFET based 6T SVL SRAM cell

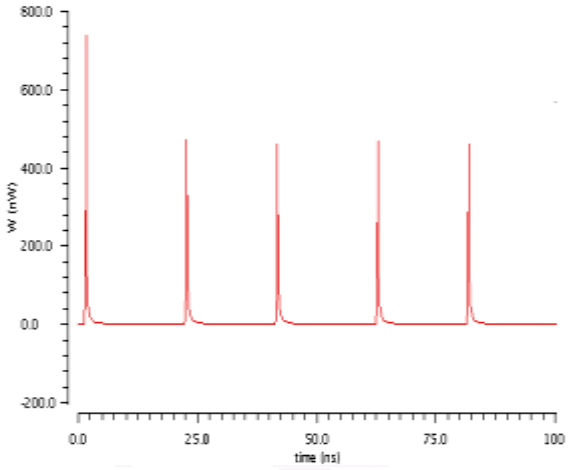

Fig -7: Leakage Power of FinFET based 6T SVL SRAM cell

Table 1 representing parameters of Conventional FinFET based 6T SRAM and SVL Technique employed FinFET based 6T SRAM, we find that SVL based 6T FinFET SRAM has reduced the value of Leakage Current.

Table -1: Comparison of 6T SRAM Leakage Current Parameter

Voltage (v)	6T SRAM (fA)	6T SVL SRAM (fA)
0.6	73.78	56.29
0.7	78.26	60.19
0.8	81.57	66.38
0.9	85.63	71.17

Table 2 representing parameters of Conventional FinFET based 6T SRAM and SVL technique employed FinFET 6T SRAM and find that SVL technique employed FinFET based 6T SRAM has reduced the value of Leakage Power.

Table -2: Comparison of 6T SRAM Leakage Power Parameter

Voltage (v)	6T SRAM (nW)	6T SVL SRAM (nW)
0.6	5.697	6.103
0.7	10.25	7.231
0.8	25.46	15.237
0.9	28.93	19.456

Figure 8 represents a graph of Conventional 6T FinFET SRAM and SVL technique employed FinFET based 6T SRAM at different supply voltages (0.6V, 0.7V,0.8 and 0.9V) and find that SVL technique employed 6T SRAM has a reduced graph of Leakage Current.

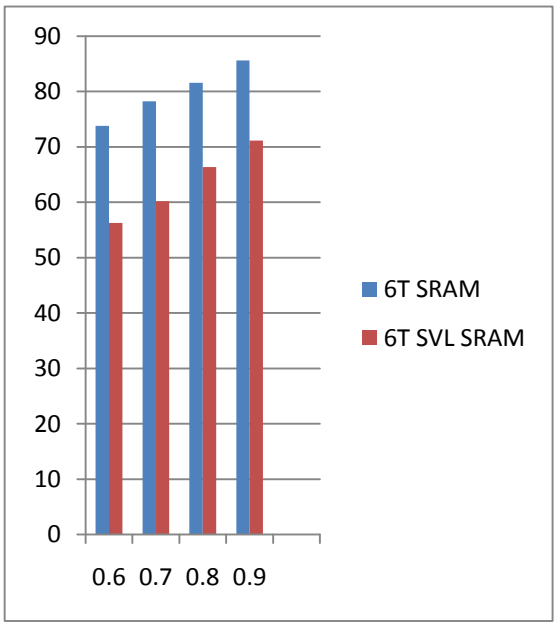

Fig -8: Graphical representation of Table 1

Figure 9 represents a graph of Conventional 6T FinFET SRAM and SVL technique employed FinFET based 6T SRAM at different supply voltages (0.6V, 0.7V,0.8 and 0.9V) and find that SVL based 6T SRAM has a reduced graph of Leakage Power.

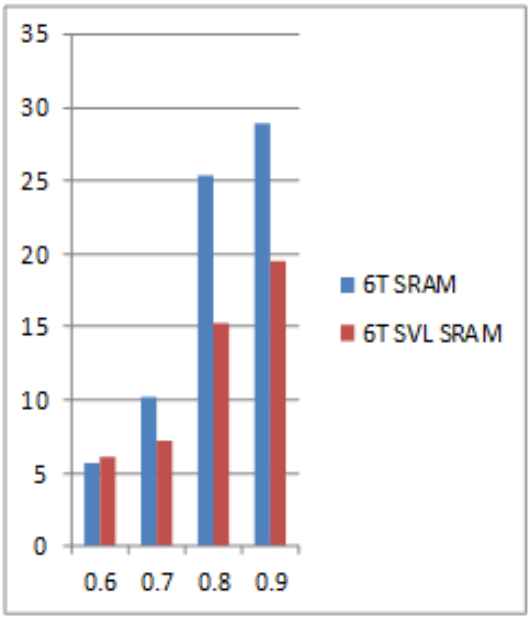

Fig -9: Graphical representation of Table 2

5. CONCLUSIONS

There has become a vicious circle of supply voltage VDD, threshold voltage Vt, power dissipation and sub-threshold current but to judiciously utilize low Vt and high Vt devices so as not to compromise between low leakage and performance. Also, supply voltage plays a key role in estimating the leakage parameters and is clearly depicted in graphs. Analysis of leakage parameters of 6T SRAM Cell with SVL technique has been calculated at 45nm technology using Cadence Virtuoso Tool. Simulation results show that Leakage Current and Leakage Power in SVL technique employed 6T FinFET SRAM cell is reduced up to 23.01% and 29.62% respectively at 0.7V. The comparison shows that the implementation of the FinFET based 6T SRAM using SVL technique would be better at 45nm technology as compared to conventional FinFET based 6T SRAM cell. The results prove that SVL technique decreases the leakage current and leakage power significantly and makes the circuit appropriate for practical applications.

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