A TESTBED FOR REAL TIME WATER LEVEL CONTROL SYSTEM

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ABSTRACT- A testbed for real time process control system that serves as a platform for experimental set up, testing and proving of a process concept has been developed in the course of this research paper work. The idea is to provide a platform where students can quickly test run the algorithm of their real- time process control design and know whether it is workable or not before the detailed implementation. The design approach supported by the testbed starts with an algorithmic state machine which is converted into a state transition table, then fully expanded and burnt into a Read Only Memory (ROM) structure. It was designed to be simple and user friendly such that students need not use an external guide but simply follow the procedures as prompted by the system. The testbed is built with locally available materials and devices with local digital experience. It can serve as a cheap and flexible platform for real–time process control experiments in higher institutions of learning.

Keywords: Process control System, Testbed, Algorithm State Machine (ASM), State Transition Table (STT), fully expanded State Transition Table, and Control Software.

1.1 Background of Study

In Nigeria and most of the developing countries, engineering education is facing unprecedented challenges and opportunities in modern times because engineering students are not adequately exposed to the practical aspects of engineering in higher institutions of learning due to insufficient equipment in school laboratories.
The design and development of a testbed for real time process control system is used to develop a platform where students can quickly test run the algorithm of their real time process control system and know whether it will work or not before the detailed implementation. Many different algorithms are used in the implementation of a process control system. The designed approach used by the testbed starts with an algorithm state machine (ASM), which is converted into State transition Table (STT), then is fully expanded and burnt into a Rom structure. The designed testbed is very simple and user friendly such that students need not use an external guide but simply follow the procedures as prompted by the system. The universal control software was deliberately chosen with the aim of teaching the students on how to use universal single software to control different process.

1.2 Statement of the Problem

Engineering students are not adequately exposed to the practical aspects of engineering in higher institutions of learning in Nigeria due to insufficient equipment in engineering laboratories. Quite often, final year students are faced with equipment–related challenges while developing degree project design. In most cases, students contract out their project development for lack of equipment within their departments and thereby lose the benefits of experience which a "do-it–yourself" approach makes possible. Some who try hard to develop their projects by themselves despite the lack of equipment end up with either a project that does not work at all or one that functions for a short time and fails, all because of under-design or lack of adequate functionality testing. A real–time testbed will definitely mitigate these problems.

1.3 Aims and Objectives:

The aim of this research paper work is to design and develop an affordable testbed for process control experiment using the algorithmic state machine (ASM) chart approach.

The objectives of this research work are to:

- Provide students with a means to rapidly test a process control algorithm before detailed implementation.
- Automate the conversion of a state transition table (STT) which ROM storage requires.

- Expose students to real time process control experiments
- To provide a platform for teaching the undergraduate students in the field of electronic engineering and other related fields.

1.4 Literature review

A testbed is defined as any venue or setup used for experimentation, testing and proving a concept. It is a platform on which assortment of experimental tools and products may be deployed and allowed to interact in real time. Process control is a term used to describe any condition natural or artificial by which a physical quantity such as temperature, pressure, flow rate, water level is regulated. The basic objective in process control is to regulate the value of some quantity which means to maintain that quantity at some desired value regardless of external influence. The desired value is called the reference value or the set point [1]. A Process control system can be a closed loop or an open loop system. A process control is typically a sequential logic system whose control algorithm can be represented in the form of a flow chart called an algorithmic state machine (ASM) chart [2] or in the form of State Transition Diagram (STD) [7].

1.5 Methodology

In this research paper work, the micro-coded ROM-based method is used and the state transition table is fully expanded and instruction codes (program) were developed using a top-down design approach. This gives a lot of flexibilities as well as enough room for further modifications.

1.6 Analysis

The testbed is designed to test liquid level process control system (water) using an ASM chart. The water level control system algorithm operation is as follows:

- When the water level in the upper tank falls to the lower threshold point, a valve is opened to let water into the upper tank. The signal that opens the valve can also be used to turn ON the water pump if anyone is in use.
- The water level lower threshold is monitored after a specified time. If there is no change in the lower threshold level an error message is displayed in the liquid crystal Display (LCD) and it will wait in that state until there is button pressed to return the system to state O. An alarm can also sound to call the attention of the process controller in case he is at a far distance.
- But if after the specified time, the lower threshold has changed, it will be monitored until it is well above the lower threshold, then it will enter state 2.
- At state 2, the water level upper threshold will be monitored until it is reached and the system will automatically return to state 0.

1.7 System design Specifications

The digital integrated circuits used in the design and the development of a testbed for real time process control system include: the AT89C52 microcontroller, the ADC0808CCN, 555 timer, the 74HC245 driver. The voltage requirement for each of them is +5v.This +5v was supplied to each of the ICs from the power supply circuit with a7805 regulator IC. For the solid state relays that are used in the output interface, the voltage required to switch them on is +9v, which is from the battery.

1.8 Hardware Subsystem Design

The hardware subsystem is made up of the following; input interface; the multiplexer, the functional codes and command control which include exit and enter command.

The output interface is the liquid Crystal Display (LCD) and thecontrol system is the brain of the testbed

1.9 Design Calculations of the testbed

Oscillator Calculation

Duty Cycle = 60%

Duty Cycle (D) = $\frac{R_1+R_2}{R_1+2R_2}$ ---- (1)

$\frac{R_1+R_2}{R_1+2R_2}$ = 60% --------- (2)

Therefore, 0.6 ($R1+2R_2$) = R1+R-----(3)

$1.2R_2 - R_2 = R_1 - 0.6R_1$ ----------(4)

$0.2R_2 = 0.4R_1$, ------ (5)

Therefore, $R_2=2R_1$ ---------- (6)

R_1+2R_2 =10k,

Therefore, $R_1+2(2R_1)$ =10k ---- (7) R_1+4R_1 =10k,

Therefore, R=2k

Now,

$R_2=2xR_1$ = 2x2k =4k

Note that the period of the output,

T= 0.693(R_1+R_2) C ---------- (8)

But F = 1/T

Therefore, F = $\frac{1.44}{(R_1+2R_2)\ C}$ ---------- (9)

F = $\frac{1.44}{(R_1+2R_2)\ C}$ = 100 kHz ----- (10)

C = $\frac{1.44}{(R_1+2R_2)\ 100k}$

C =1.44nf

B. Calculation for the output drive transistor and resistors

Load current = 700mA

$\beta > \frac{5 \text{ x load current}}{\text{Max Chip output current}}$

Max chip output current**= 35mA**

Therefore,

$\beta > \frac{5 \text{ x } 700mA}{}$ =100 ----(11)

=35mA Assume β=120

$I_\beta = \frac{I_c}{\beta} = \frac{700mA}{120}$ = 5.83mA

Chip Output Voltage = 5v =V_o

$V_0 = I_B R_B + V_{BE}$; V_{BE} = 0.7V----- (12)

R_B =737.6Ω

Preferred Value = 730Ω

2.0 Discussion

Every ASM chart has an equivalent tabular representation known as a State Transition Table (STT). An ASM chart can be fully described in terms of the link paths comprising it. A state machine such as is represented by an ASM chart attempts to change state (that is transits from the present state to the next) when a clock pulse occurs.

A link path is a path followed from the present state back to itself or to another state when the clock pulse arrives. When there is an input qualifier between the present state and another, the logic level of the qualifier determines the next State the machine goes at the clock pulse. If there is no qualifier between the present state and the next, the machine must conditionally transit from its present state to the adjacent state in the forward direction, when a clock pulse arrives.

Table 1.0: Fully Expanded State Transition Table

Hex Address	Link path	Lth Mth Uth	B A Present State Code	B^1 A^1 Next State Code	H_{V1} H_{V2}	Location Content
00	L1	0 0 0	00	0 0	0 0	0 0
08	L1	0 1 0	00	0 0	0 0	0 0
10	L2	1 0 0	00	0 1	0 0	0 4
14	L2	1 0 1	00	0 1	0 0	0 4
18	L2	1 1 0	00	0 1	0 0	0 4
1C	L2	1 1 1	00	0 1	0 0	0 4
04	L3	0 0 1	00	1 1	0 0	0 C
0C	L3	0 1 1	00	1 1	0 0	0 C
01	L4	0 0 0	01	0 1	1 0	0 6
11	L4	1 0 1	01	0 1	1 0	0 6
05	L4	0 0 1	01	0 1	1 0	0 6
11	L4	1 0 0	01	0 1	1 0	0 6
05	L5	0 1 0	01	0 0	1 0	0 2
15	L5	0 1 1	01	0 0	1 0	0 2
19	L5	1 1 0	01	0 0	1 0	0 2
1D	L5	1 1 1	01	0 0	1 0	0 2
03	L6	0 0 0	11	1 1	0 1	0 D
07	L6	0 0 1	11	1 1	0 1	0 D
13	L6	1 0 0	11	1 1	0 1	0 D
17	L6	1 0 1	11	1 1	0 1	0 D
0B	L7	0 1 0	11	0 0	0 1	0 1
0F	L7	0 1 1	11	0 0	0 1	0 1
1F	L7	1 1 0	11	0 0	0 1	0 1
1B	L7	1 1 1	11	0 0	0 1	0 1

To burn the fully expanded STT into Rom, the qualifiers and present state code together constitute the address bits to the ROM while the next state code and output bits constitute the corresponding ROM content for each location.

2.1 Conclusion

The designed testbed will enable easy learning of process control system in the classroom using algorithms as well as making it possible to transfer theoretical work to practical reality are necessity in higher institutions of learning. Hence, it is an educational tool. When mass produced, it will go a long way to improve the quality and standard of education in higher institution of learning.

REFERENCES

1. Curtis D Johnson, Process Control Instrumentation Technology,8thEdition,2006,Prentice –Hall Inc. pp 1-10
2. Inyiama H.C, Okezie C.C, Designing of microcontroller -based universal process control systems, volume 2 number 2 (electroscope), November 2007. Department of Electronics Engineering, Nnamdi Azikiwe University, Awka.
3. Clare. C.R, Designing logic system using state machines (U.K, Mac Graw-Hill, 1937) pp1-108.
4. Micheal J. Point, Embedded C, 2002, Pearson Education Limited, pp17-34.
5. Atmel Corporation, Microcontrollers MCS - 51 family of product literature 2325 Orchard Parkway ,San Jose, CA 95131,USA.
6. B. Wittenmark, K.J. Astron and K.E Arzen(2003)"Computer Control: An Overview". Department of Automatic Control, Lund Institute of Technology, Sweden. (www.Control .lth.se/kursdr/fac pdf.)
7. Dennis Wixom Roth System Analysis &Design.
8. Mazidi M.A, Mazidi J.C, The microcontroller and Embedded Systems, 2000, Prentice-hall, Inc, Pearson Education, pp 28.
9. Dogan Ibrahim, Microcontroller projects in embedded C for the 8051, 2000, Biddles ltd Guidford and King`s Lynn pp 108.
10. Walter G. Jung IC timer cookbook (4300 west 82nd st .Indianapolis 48258 USA, Howard W. Sams &Co Inc 1977) pp 1-36
11. Thomas L Floyd, Digital Fundamentals Tenth Edition 2009, Prentice –Hall, Inc Pearson Education, pp 390-396.
12. A. Aspinal and E. Dagles, Introduction to Microprocessor (College of Swansea, Department of Electrical/Electronic Engineering, University, 1976) pp 1-50.
13. Bertram J.E: The Concept of state in the analysis of Discrete Time Control System, 1962, Joint AUTOM .Control Conf. New York University (June 27 -29), Paper N0 11-1.
14. Mano, M., M., & Kime, C., R., Logic and computer design fundamentals. 3rded. Upper Saddle River, N.J.: Pearson Education, 2004.
15. Owen. B. Beginner`s Guide to Electronics, 4thEdition, 1995. A Newness Technical Book, McGraw-Hill Companies inc. New York, N.Y USA.
16. Roger L. Tokheim, Digital electronics principles and applications, fifth Edition, 1996, Glencoe/McGraw–Hill Companies pp 158. 17-34
17. Horowitz, P and Winfield, H. The Art of Electronics, 2nd edition2002.CambrigdeUniversty, Press Cambridge, UK, pp 63-66
18. Faissler, B. l, An introduction to modern Electronics, 1991, Willey, New York, NY, USA.