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Design of Capacitor less LDO Regulator by using cascode compensation technique

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Abstract - *This paper discusses two different methodologies to design a Low Dropout Voltage Regulator (LDOVR) with their applications. In the first approach, a basic LDO regulator is designed which uses a compensation capacitor to achieve stability. The dropout voltage of this LDO is 200mV with an output voltage of 1.4V. For worst case stability, bandwidth and phase margin (PM) are 475.67 KHz and 43.85 degrees. Another LDO is also designed with capacitor less approach having high DC loop gain and wide bandwidth. This design having a dropout voltage of 100 mV uses a miller compensation capacitor to achieve stability along with a series resistor to shift the right half plane zero to left half plane which leads to high bandwidth. A total of 80pF capacitor and 50 Kohms resistance are used to achieve proper stability with bandwidth of 2.55 MHz and PM of 63 degrees in worst case stability scenario.*

Key Words: LDO Regulator, cascode compensation, Ahuja compensation, capacitor less LDO, LDOVR

1. INTRODUCTION

The Voltage Regulator is a key part of power management circuitry in integrated circuits. Voltage regulators are used to supply a constant voltage in spite of variations in load and power supply. With the reduction in supply voltage and demand of low power designs, LDO regulators are becoming an obvious choice for design engineers. The market need for portable devices is truly driving the technology of LDO regulators.

The most fundamental requirement of an LDO regulator is a constant output voltage irrespective of supply and load variations. While this is easily achieved for various load currents and supply voltages, the problem arises when there is a sudden change in the line voltage or load current. The output voltage may go through some overshoots and undershoots before settling down to the previous voltage. This is due to the fact that the loop takes some time to regulate. To reduce the loop regulation time, we want high bandwidth. High phase margin is required to reduce the ringing of output voltage during transients. Another very important requirement of the LDO regulator is low load and line regulations. While line regulation is a measure of change in output voltage with respect to change in supply voltage (V/V), load regulation depicts the change in output voltage with load current variations (V/I), which is nothing but output resistance of the circuit. An LDO uses a shunt feedback for the regulation which means a low output resistance (and thus low load regulation) can be achieved by high DC loop gain. Low dropout and low quiescent current (Iq) are required for low power dissipation thus increasing the efficiency of the LDO regulator [1-2]. In short, a good LDO regulator should have high dc loop gain, low load and line regulations, wide bandwidth and low quiescent current. While the circuit requirements are quite obvious, it is difficult to achieve all of them due to a lot of trade-offs between these parameters. The detailed discussion is in subsequent sections.

Section 2 discusses about the basic LDO circuit operation and its main drawback with a basic design example. In section 3, a capacitor less approach of designing LDO regulators is discussed in detail. A capacitor less LDO design using cascode compensation technique is also discussed and presented here with results. Section 4 compares the two design styles to conclude.

2. BASIC LDO REGULATOR

2.1 Circuit operation:

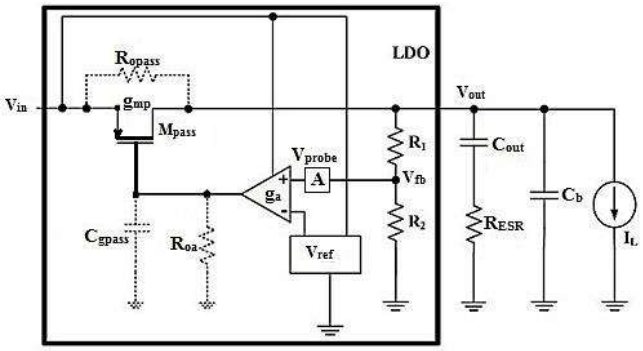

Fig -1: Basic LDO Regulator

A basic LDO regulator (with compensation capacitor) is shown in Fig-1. It generally uses a PMOS transistor as a pass element to achieve low dropout voltage across it. An NMOS transistor can also be used when a higher dropout is allowed. Otherwise, a charge pump circuit is used to provide necessary charge for low dropout. The pass element acts as a voltage varying resistor (here represented by R_{opass}) to maintain a constant output voltage at the output. An error amplifier is used to generate an error signal between the reference voltage and output feedback through resistors R_1 and R_2. The

reference voltage is the most stable voltage in this circuit and it is generally a bandgap reference voltage. The value of V_{ref}, R_1 and R_2 is chosen according to the desired output value e.g. for $R_1 = R_2$, $V_{out} = 2V_{ref}$.

An LDO voltage regulator is a Voltage Controlled, Voltage Source (VCVS), so the output resistance is required to be low. This is achieved by the using shunt feedback which reduces the overall output resistance by a factor of (1 + A_0), where A_0 is the dc loop gain. A large output capacitor C_{out} is used to enhance the transient response, thus also called as compensation capacitor. Whenever the load current changes abruptly, the high current demand is fulfilled by this C_{out} capacitor. As C_{out} is of very high value, it also has a reasonable Electrical Series Resistance (R_{ESR}) also called as Effective Series Resistance. An extra pole and zero is created due to R_{ESR} which sometimes may cause stability issues that must be considered. To reduce the effect of this ESR we may apply a bypass capacitor C_b at the output [1].

2.2 Transfer Function:

For deriving the transfer function of the LDO, the loop can be broken at point A, as shown in Fig 1 and a probe is applied there. The open loop gain is given as [1]

$$\frac{V_{fb}}{V_{ref}} = \frac{V_{out}}{V_{ref}} \cdot \frac{V_{fb}}{V_{out}} = \frac{g_a R_{oa} g_{mp} Z}{[1+sR_{oa}C_{gpass}]} \cdot \frac{R_1}{R_1+R_2} \quad (1)$$

Where, g_a is the transconductance of the error amplifier, g_{mp} is the transconductance of the pass element which is nothing but a transistor, here represented as a transconductance amplifier. R_{oa} is the output resistance of the error amplifier, C_{par} is the parasitic capacitance associated with the gate of pass element, R_1 and R_2 are feedback resistances and Z is the impedance seen at the output V_{out} which is again given by [1]

$$Z = R_{opass} \,||(R_1 + R_2)\, || \frac{1+sR_{esr}C_{out}}{sC_{out}} \,|| \frac{1}{sC_b} \quad (2)$$

Where, C_{out} and R_{esr} are the capacitances and Effective Series Resistance (ESR) of the output capacitor, C_b is the high frequency bypass capacitor having low ESR used to nullify the ESR of output capacitor, R_{opass} is the output resistance of the pass element, which is generally very lower as compared to feedback resistors. So, (R_1+R_2) can be neglected. If C_o is assumed to be considerably larger than C_b (typically), then Z is approximately [1]

$$Z = \frac{R_{opass}[1+sR_{esr}C_{out}]}{[1+s(R_{opass}+R_{esr})C_{out}]\cdot[1+s(R_{opass}||R_{esr})C_b]} \quad (3)$$

It can easily be observed that the open loop transfer function consists of three poles and one zero, and thus is a potentially unstable system. The poles and zeros can be approximated as [1]

$$P_1 = {}^1/_{2\pi R_{o-pass} C_{out}} \quad (4)$$

$$P_2 = {}^1/_{2\pi R_{ESR} C_b} \quad (5)$$

$$P_3 = {}^1/_{2\pi R_{oa} C_{gpass}} \quad (6)$$

$$Z_1 = {}^1/_{2\pi R_{ESR} C_{out}} \quad (7)$$

A typical magnitude plot of the system can be shown as in Fig-2. For the system to be stable and having acceptable transient response, the pole P_3 is required to be as far as possible (to the right side) from the unity gain bandwidth of the system.

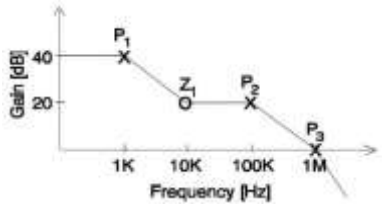

Fig-2: Approximated magnitude plot of an LDOVR [1]

To achieve the stability of this circuit, pole P_3 must be situated after the close loop bandwidth frequency. To achieve this, both R_{oa} and C_{gpass} must be low. But, this is not generally the case. A high R_{oa} is desirable to meet the high dc gain requirements and the pass transistor is large (means high C_{gpass}) to meet the load current requirements. This problem is solved by inserting a buffer between error amplifier and pass transistor. This buffer takes care of the high dc gain of the loop but also reflects a low output resistance to the pass transistor. Though it also increases complexity as now there is one more pole to be taken care of which should be again at higher frequencies. When the load current varies, it affects the pole positions of the system and thus the stability.

2.3 Design and Results:

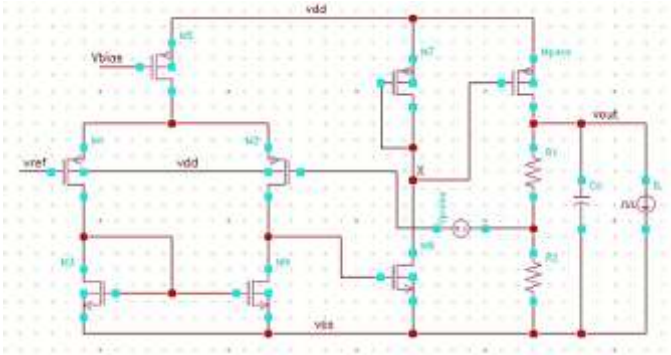

Fig-3: Schematic of basic LDOVR (with output capacitor)

A basic LDO regulator is designed using buffer stage for a maximum load current capability of 5mA and providing a constant V_{out} of 1.4V which is shown in Fig-3. For simplicity purpose, R_{ESR} is ignored and thus C_b. Then, pole P_1 is decided by C_{out} and R_{opass} which is dominant. Output resistance of buffer (R_{obuff}) and C_{gpass} constitutes pole P_2. To make P_2 sufficiently non dominant, a CS stage buffer is used with diode connected load providing low output resistance. The worst case bandwidth of the LDO is 475.67 KHz with a PM of 43.85 degrees. The magnitude and phase plot are shown in Fig-4. The amount of load current highly affects the stability of the system. In no load condition i.e.

when load current is zero, the only current which flows through the M_{pass} is quiescent current (I_q). This I_q current depends upon the value of (R_1 + R_2) and I_q is required to be low. So, R_{opass} is higher moving the dominant pole towards lower frequencies enhancing the stability, though bandwidth is reduced. A larger output capacitor (in μFs) is generally used to supply the current demands during load transients for lower bandwidth systems. In full load condition, the current through the M_{pass} is (I_{load} + I_q) leading to lower R_{opass} which moves the dominant pole towards the bandwidth frequency deteriorating the stability. Thus, full load condition is the worst case stability condition for a basic LDO regulator. The output voltage transients are observed at no load and full load conditions as shown in Fig. 5. When the current switches from zero (no load) to 5 mA (full load), the loop takes some time to regulate. Meanwhile, the output capacitor provides (discharges) the required current to the load which leads to reduction in output voltage. After some time, loop is regulated and the current is provided by pass transistor. This current needs to fulfill the load requirements as well as recharge the output capacitor at the same time. So, we design the pass transistor such that its current capability is greater than full load condition. After, the capacitor get fully charged, the output voltage is back to the required constant value. To minimize the output error, the loop should regulate quickly which means bandwidth of the circuit should be high. In another situation when the output current suddenly falls from 5 mA (full load) to zero (no load), during the loop regulation, the extra current supplied by the pass transistor is taken by the capacitor, which leads to its charging and thus increase in the output voltage. After the loop gets regulated, the extra charge on the capacitor discharges through the feedback resistances and output voltage again

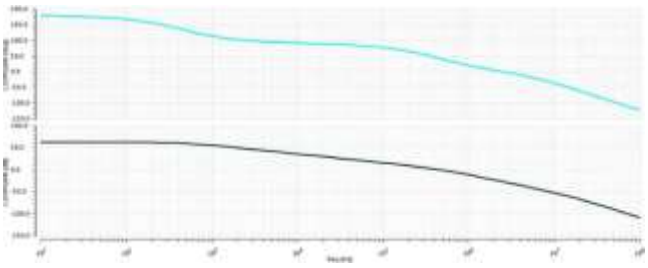

Fig-4: Magnitude and phase plot of basic LDOVR

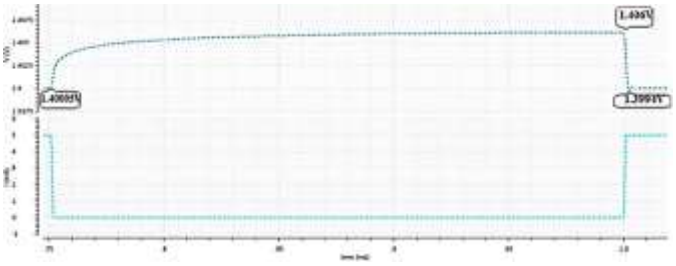

Fig-5: Transient response of basic LDOVR

comes back to the required value of 1.4 V. The output voltage will again come back to 1.4 V only and not any other values, is because the steady state output voltage is only decided by feedback resistances R_1 and R_2 and reference voltage.

2.4 Applications and Drawback

This type of approach leads to very good stability and low ringing due to the presence of a high value output capacitor. This itself limits its application and is only feasible whenever an off chip compensation capacitor is allowed for the circuit to work. A large on chip capacitor is too bulky and costly. Also, the load regulation of this type of LDO is poor due to low dc loop gain. The dc gain may be increased by increasing R_{oa}, which may shift the non-dominant pole inside the bandwidth frequency causing stability issues.

It is okay to apply this output voltage to digital circuits, due to their high noise margins. A small change in voltage may lead to unwanted results in case this LDO provides input to an analog circuit. For a more feasible on-chip LDO with better load regulations, a capacitor less approach is used which is discussed in next section.

3. CAPACITORLESS LDO REGULATOR

3.1 LDO with Miller Compensation

In this approach, a very low value (less than nF) output capacitor is used which constitutes the non-dominant pole of the system [2-6]. This is unlike the basic approach discussed in section II in which the high output capacitor gives the dominant pole. The dominant pole is actually achieved by the R_{oa} and C_{gpass} as in Fig. 1. As for a dominant pole, we want these to be high, so generally there is no need to insert a buffer in this approach. A simplified block level structure of capacitor less LDO regulator is shown in Fig. 6.

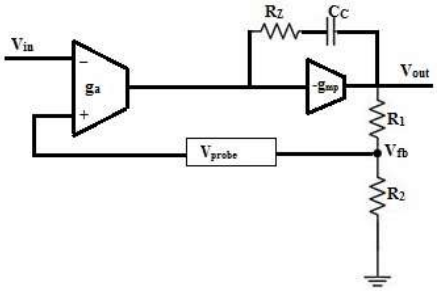

Fig-6: Simple representation of a capcitor less LDOVR

The pole zero equations of the system as explained in [7] are

$$P_1 \approx \frac{1}{R_{oa}C_C g_{mp} R_{opass}} \quad (8)$$

$$P_1 \approx \frac{g_{mp}C_C}{C_{gpass}C_C + C_C C_{out} + C_{out}C_{gpass}} \quad (9)$$

$$Z_1 \approx \frac{1}{\left(\frac{1}{g_{mp}} - R_Z\right)C_C} \quad (10)$$

Though this approach seems to be quite simple and easy, the problem lies in making the output pole P_2 non-dominant. The value of R_{oa} and C_{gpass} is not so high as compared to the output capacitor C_{out} and resistance R_{opass}. So, the distance between P_1 and P_2 is not very large to place the pole P_2 outside the bandwidth. One might think that just by making C_{out} to zero can place P_2 at infinite frequency thus meeting the stability. This solution can surely stabilize the loop but will not work unless we have an infinite bandwidth (meaning loop regulates in no time). Since, this is not achievable, no matter how stable the loop is, there will be no capacitor to provide extra current to the load while abrupt switching, thus hurting the transients.

Another approach is to use a miller compensated capacitor C_c [8] as shown in Fig. 6 which performs pole splitting to achieve loop stability without removing the output capacitor fully. This phenomenon is depicted in Fig-7

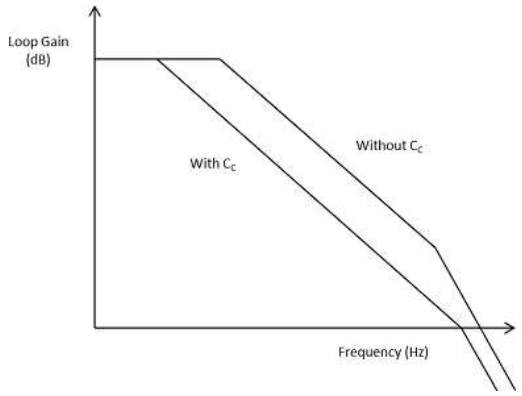

Fig-7: Miller compensation capacitor performing pole splitting (not to scale)

Along with the pole splitting, this C_C also creates a right half plane zero as it creates a feed forward path which degrades the stability of the system. So, a series resistance R_Z is being used to cancel the RHP zero. The value of R_Z can also be chosen in such a way that the RHP zero moves towards the left hand side of the plane which can improve the stability [8].

3.2 LDO with Cascode Compensation

As discussed above, the resistor R_Z is used in series with C_C to cancel RHP zero. This requirement can also be achieved by using a common gate (CG) stage transistor as shown in Fig-8. The equation of zero then becomes

$$Z_1 \approx -\frac{g_{mCG}}{C_C} \quad (11)$$

The main advantage of this technique over the resistive technique lies in the fact that actually no extra transistor is needed to achieve this compensation. The CG stage transistors are internally present in cascode designs like Telescopic and Folded cascode amplifiers so the name cascode compensation. This technique is also popularly known as "Ahuja Compensation" [6].

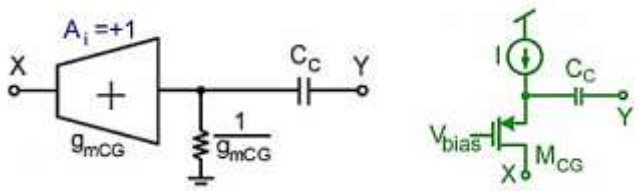

Fig-8: Cascode compenstation technique [7]

3.3 LDO design with Cascode Compensation and Results

A capacitorless LDO regulator using cascode compensation technique is designed in 180nm technology using Cadence Virtuoso tool as shown in Fig-9. Unlike miller compensation, the compensation capacitor C_C is added in feedback from output to the folding node B of the folded cascode stage. Here transistor M_7 is acting as a common gate stage. Though g_{mCG} (here g_{M7}) generates an LHP zero at $-g_{mCG}/C_C$, a proper placemnet of this zero is necessary to achieve stability. Varying g_{mCG} may disturb the gain as well as dc biasing of the circuit. So, a series resistor R_z is added to provide more control over the movement of zero. So, the equation of zero is now

$$Z \approx \frac{-1}{\left(\frac{1}{g_{mCG}}+R_Z\right)C_C} \quad (12)$$

$$Z \approx \frac{-1}{R_Z C_C} \quad for\ R_Z \gg \frac{1}{g_{mCG}} \quad (13)$$

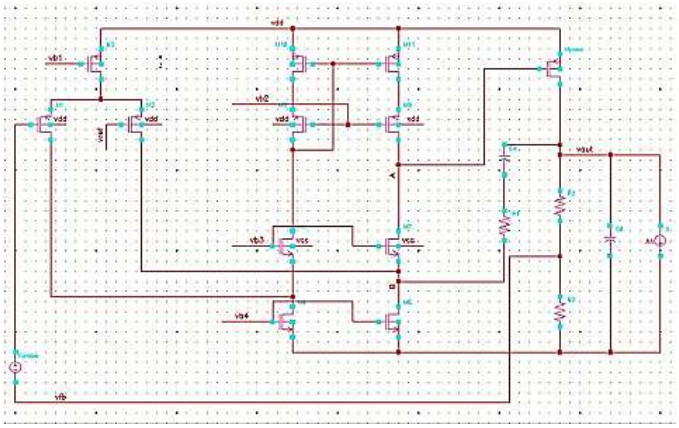

Fig-9: Schematic of LDO regulator using cascode compenstation technique

A total of 80pF is used for compensation of the design which is very less as compared to 1uF used in classic LDO design style. A large pass transistor of size 3500µ/0.18µ is used to drive a full load current of 50mA. Unlike basic LDO design, the worst case is a no load condition. This is because the output pole is now the non-dominant pole. In no load condition, very small amount of quiescent current is flowing through pass transistor making its output resistance high. This moves the non-dominant pole towards the bandwidth frequency and thus may cause instability. The worst case magnitude and phase response is shown in Fig-10. The worst case bandwidth and phase margin are 2.55 MHz and 63 degrees respectively. The dc

loop gain achieved is 82.45 dB. This high dc loop gain is achieved due to high output resistance of folded cascode design. Figure-11 shows the transient analysis of the LDO with a full swing variation in load from 0 to 50mA. The maximum positive variation is 69 mV and maximum negative variation is 72 mV. As compared to the basic LDO design, these results are not so accurate. This is because of a low value capacitor at the output which takes very less time to charge and discharge thus it is unable to source/sink extra current when the loop is regulating. The load regulation is calculated to be 0.74%. The load regulation is better in this case due high dc gain provided by the folded cascode stage. The output voltage is also plotted in Fig-12 with the line voltage switching from 1.5 V to 2 V. The maximum voltage variation is 19 mV above and 18.6 mV below the required output voltage of 1.4 V. Line regulation is calculated as 0.18 %. The PSRR of the design is 88.36 dB at dc, 47 dB at 10 KHz and 12 dB at 1MHz.

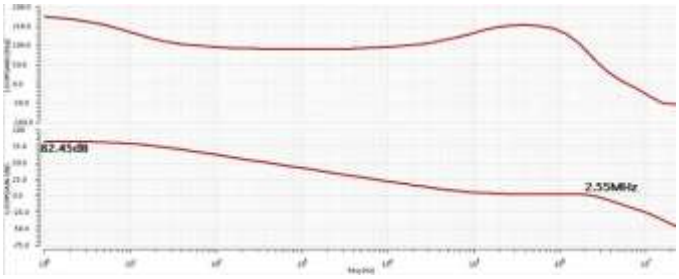

Fig-10: Magnitude and Phase plot of LDO design in Fig-8

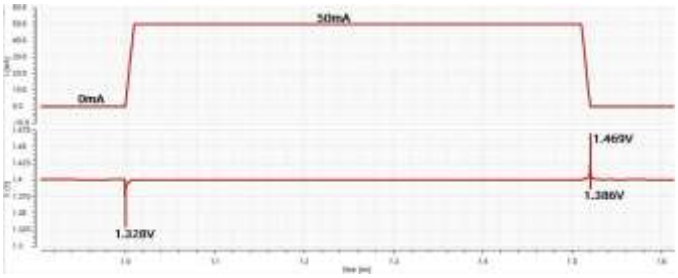

Fig-11: Load transient response of LDO design in Fig-8

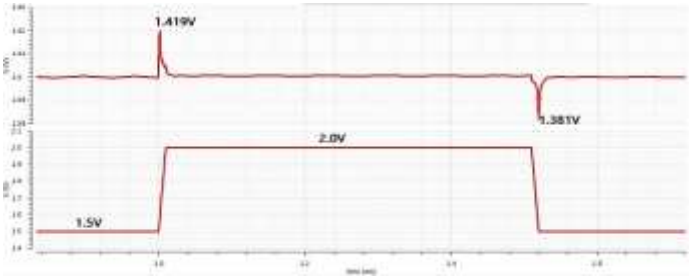

Fig-12: Line transient response of LDO design in Fig-8

4. CONCLUSION

The above discussion clearly explains the two different techniques of designing an LDO regulator with design examples. The key differences clearly evident from this paper are:

a) *Output Capacitor:* The output capacitor of a basic LDO regulator is high (in μF) to make output pole dominant. A very low output capacitor is used in capacitor less approach to make output pole non dominant. So, for on-chip LDOs we always prefer capacitor less LDO regulators.

b) *Worst case stability:* As the output pole is dominant in basic LDO regulator, a full load current will reduce the output resistance thus moving dominant pole towards the bandwidth frequency and degrading stability. In capacitor less approach, the output pole is non-dominant. So, a no load current condition having large output resistance can move the non-dominant pole towards the bandwidth frequency which may cause instability.

c) *Load Regulation:* Load regulation is better when dc loop gain is high. In basic LDO, a high dc loop gain may cause instability by moving the internal pole which is non-dominant towards the bandwidth frequency. Unlike this, a high dc loop gain is favorable in capacitor less approach making the load regulation better in this case.

d) *Transient Response:* Due to the presence of large output capacitor, the transient response of the basic LDO is better than capacitor less LDO. With advancement in analog design blocks, they are becoming more and more robust and prone to minor variations. This has led to the acceptance of capacitor less LDOs apart from having some variations during load switching.

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