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Proportional Resonant Controller with Resonant Harmonic Compensators for Three-Phase Multilevel Inverter

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Abstract - *In this project the design of a proportional resonant controller for three phase 7 level inverter for grid-connected applications. On the other hand, the output voltage waveform is distorted by the negative and zero sequence and current harmonics due to the unbalanced and nonlinear loads. The aim of this controller is to produce inverter output sinusoidal voltage with low Total Harmonic Distortion (THD) even with nonlinear loads and provide the good transient response for the sudden change in load in order to meet the international standards IEEE519. The system is simulated using MATLAB/SIMULINK software program*

Key words: *Nonlinear Load; Harmonic Compensation; Proportional-Resonant (PR) Controller*, Resonant Controller, Grid Voltage Harmonics

I. INTRODUCTION

In last few years focus on renewable energy sources like wind, solar and hydro and their use in power generation has led to develop new techniques to control and synchronize them with the grid. Many inverter topologies have been discovered to reduce current ripples in grid connected systems with these renewable power sources as their input.

These grid connected renewable sources improves stability of the grid by supplying active power during peak demand. But these have some disadvantages like introduction of harmonics in the grid current; power generation completely depends upon environmental condition etc.

In grid, current harmonics should be limited up to 5% as per IEEE-519 standard. Control of feeding active and reactive power to the grid is a big deal. Simple PI controllers are used commonly but they have certain drawbacks like steady sate error in stationary reference frame and necessity to decouple phase dependency in three phase system etc.

They are easy to implement. Newly developed PR controller (proportional resonant controller) and harmonic compensator is absolutely free from above mentions problems and can be implemented in a cheap fixed-point DSP along with filter in the common coupling point to reduce current harmonics.

LC filter has great harmonics suppression capability but it sometime makes the system response oscillatory. Instead of that in this paper L filter has been used.

To improve the quality of the output different PWM methods and different inverter topologies have been adopted. Here, thin phase disposition (IPD)' PWM technique has been adopted for 7 level diode clamped multilevel inverter.

2 PROPORTIONAL RESONANT

Resonant Controllers are based on the Internal Model Principle (IMP) [16], which states that a very good tracking for a reference or a rejection for disturbances signals is ensured if the closed-loop system is stable.

Its main characteristic is to introduce infinite gain at certain resonant frequency that should equal to the periodic reference signal frequency.

The transfer function of this controller with sinusoidal internal model is

The PR current controller *GPR(s)* is represented by:

$$G_r(s) = \frac{\omega_r^2}{s^2 + \omega_r^2} \qquad (1)$$

According to IMP, if the closed-loop stability is guaranteed, then the resonant controller defined in (1) ensures zero steady state error for sinusoidal tracking (disturbance rejection) at frequency w_r.This PR controller described by is considered an ideal controller and as shown from Bode diagram that it has a theoretically infinite gain at the frequency w_r which enables it to ensure zero steady-state error at this frequency only and introduces no gain or phase shift at other frequencies.

This infinite gain of the ideal controller may lead to difficulty in the implementation with either analogue or digital system .Furthermore in this ideal controller it is not possible to select proper gain and width for the controller which reduces the controller design flexibility and may lead to stability problems. So instead of using this ideal controller described above, it is better to use the non-ideal form of the controller which has a finite gain that is still relatively high for good tracking performance to ensure zero steady state error. The Bode plot of non-ideal PR control

$$G_{pr}(s) = k_p + \frac{2k_i \omega_c s}{s^2 + 2\omega_c s + \omega_r^2}$$

2.1 HARMONIC COMPENSATORS DESIGN

Harmonic compensators were designed for the 3rd, 5th and 7th harmonics. The PR harmonic Compensators were designed using SISO Tool in Matlab with the resonant frequency set to the particular frequency to be compensated, i.e. 150Hz for the 3rd harmonic, 250Hz for the 5th harmonic and 350Hz for the 7th harmonic. Similarly to the fundamental PR current control design, the Root Locus, Open Loop and Closed Loop Bode diagrams plotted by SISO Tool were used to achieve the optimal design for each harmonic compensator. Each harmonic compensator was designed on its own and then combined together with the fundamental PR controller at the end in SISO Tool. Ultimately fine tuning of the compensators was performed to obtain the optimum operation of the compensators by varying ω_c and KI of the corresponding compensator. Care was taken that the system remains stable, by using the gain margin and phase margin stability criteria.

The 3rd harmonic compensator at a resonant frequency $3\omega_0$ of 942.48rad/s (150Hz) was designed with a ω_c of 0.3 rad/s and a K_I of 1. Open Loop and Closed Loop Bode diagrams plotted by SISO Tool matlab shown in fig.4.2.

$$G_h(s) = \frac{0.6s}{s^2+0.6s+942*942}$$

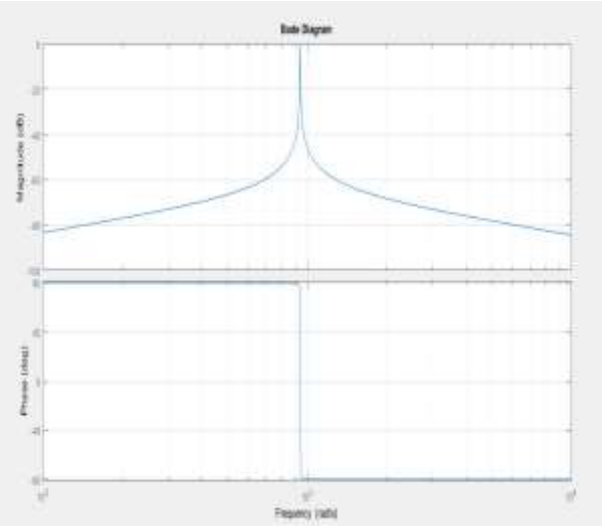

Figure 1 Non-ideal proportional resonant 3rd harmonic compensator controller Bode diagram

The 5th harmonic compensator at a resonant frequency $5\omega_0$ of 1570rad/s (250Hz) was designed with a ω_c of 4.2 rad/s and a K_I of 1. . Open Loop and Closed Loop Bode diagrams plotted by SISO Tool matlab shown in fig.4.3.

$$G_h(s) = \frac{8.2s}{s^2+8.2s+1570*1570}$$

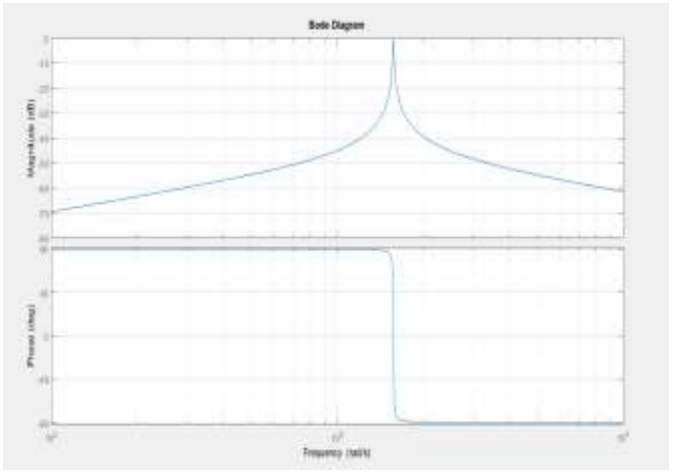

Figure 2 Non-ideal proportional resonant 5rd harmonic compensator controller Bode diagram

The 7th harmonic compensator at a resonant frequency $7\omega_0$ of 2199rad/s (350Hz) was designed with a ω_c of 2 rad/s and a K_I of 1. Open Loop and Closed Loop Bode diagrams plotted by SISO Tool matlab shown in fig.4.4.

$$G_h(s) = \frac{4s}{s^2+4s+2199*2199}$$

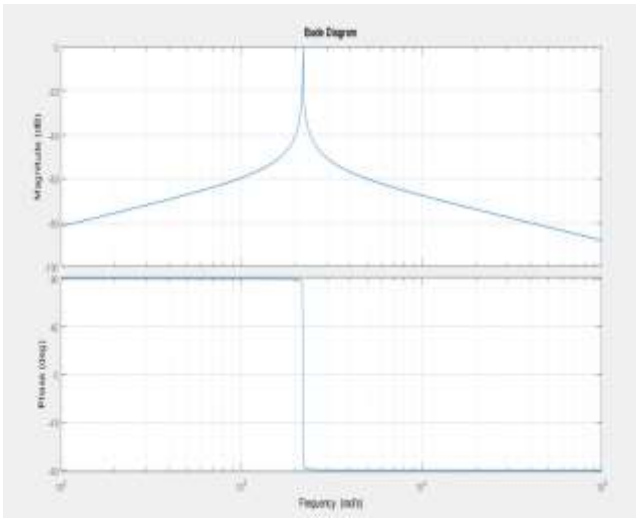

Figure 3 Non-ideal proportional resonant 7rd harmonic compensator controller Bode diagram

The transfer function of the complete controller $GC(s)$ is shown in

$$G_c(s) = G_{PR}(s) + G_{PR}(s) + G_{PR}(s) = \frac{0.6s}{s^2+0.6s+942*942} + \frac{8.2s}{s^2+8.2s+1570*1570} + \frac{4s}{s^2+4s+2199*2199}$$

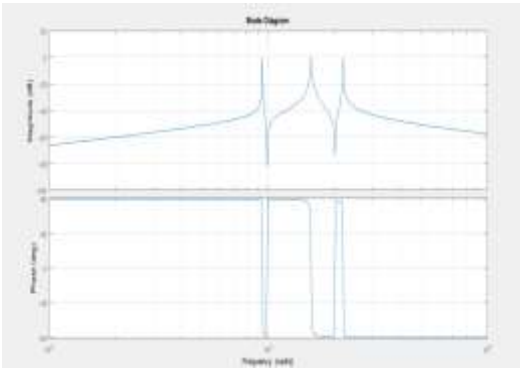

Figure 4 Non-ideal proportional resonant *GC(s)* harmonic compensator controller Bode diagram

The block diagram of the complete system used to design the selective harmonic compensators is shown in Fig. 3.

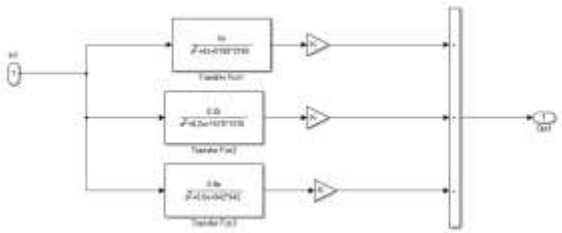

Figure 5 the selective harmonic compensators

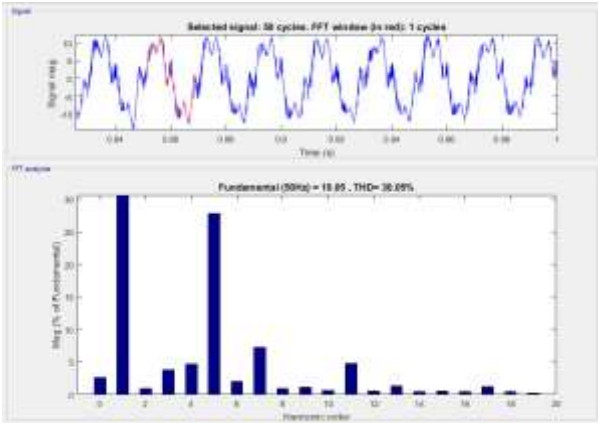

Figure 6 FFT ANALYSIS INPUT TO PR CONTROLLER

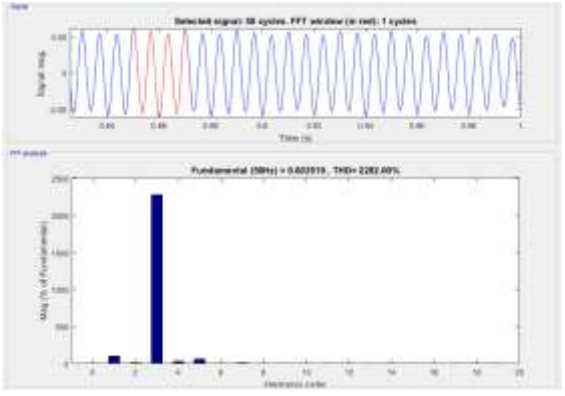

Figure 7 proportional resonant 3rd harmonic compensator output

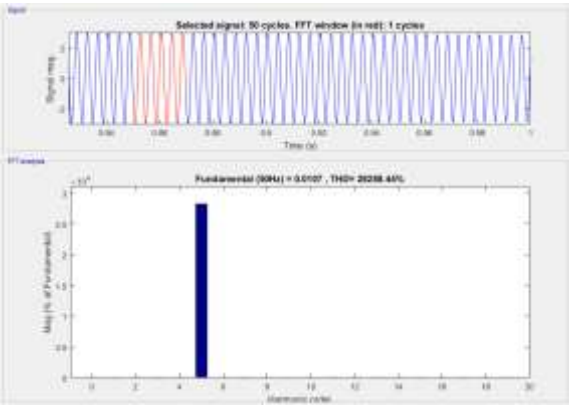

Figure 8 proportional resonant 5th harmonic compensator output

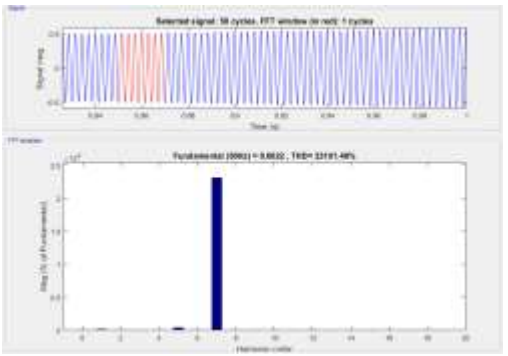

Figure 9 proportional resonant 7th harmonic compensator output

3.DIODE CLAMPED MULTI LEVEL INVERTER

The first invention in multilevel converters was the so-called neutral point clamped inverter. It was initially proposed as a three level inverter. It has been shown that the principle of diode clamping can Extended to any level. A diode clamped leg circuit is shown in Figure.

The main advantages and disadvantages of this topology are:

Advantages:

• High efficiency for the fundamental switching frequency.

• The capacitors can be pre-charged together at the desired voltage level.

• The capacitance requirement of the inverter is minimized due to all phases sharing a Common DC link.

3.1 Neutral Point-Clamped Inverter: A seven-level diode- Clamped inverter

In this circuit, the dc-bus voltage is split into seven levels by six series-connected bulk capacitors, C1,C2,C3,C4,C5 and C6. The middle point of the two capacitors n can be defined as the neutral point. The output voltage van has seven states: Vdc, 2Vdc/3 ,Vdc/3 0, - Vdc/3 , -2Vdc/3, -Vdc. For voltage level Vdc/2, switches S1 and S2 need to be turned on; for -Vdc/2, switches S1' and S2' need to be turned on;

and for the 0 level, S2 and S1' need to be turned on. The key components that distinguish this circuit from a conventional two-level inverter are D1 and D1'. These two diodes clamp the switch voltage to half the level of the dc-bus voltage. When both S1 and S2 turn on, the voltage across a and 0 is Vdc i.e., va0 =Vdc. In this case, D1' balances out the voltage sharing between S1' and S2' with S1' blocking the voltage across C1 and S2' blocking the voltage across C2. Notice that output voltage van is ac, and va0 is dc. The difference between van and va0 is the voltage across C2, which is Vdc /2. If the output is removed out between a and 0, then the circuit becomes a dc/dc converter, which has three output voltage levels: Vdc ,Vdc/2, and 0.Considering that m is the number of steps of the phase voltage with respect to the negative terminal of the inverter, then the number of steps in the voltage between two phases of the load k is k = 2m+1 (1) and the number of steps p in the phase voltage of a three-phase load in wye connection is p = 2k – 1. By increasing the number of levels in the inverter, the output voltages have more steps generating a staircase waveform, which has a reduced harmonic distortion. However, a high number of levels increases the control complexity and introduces voltage imbalance problems.

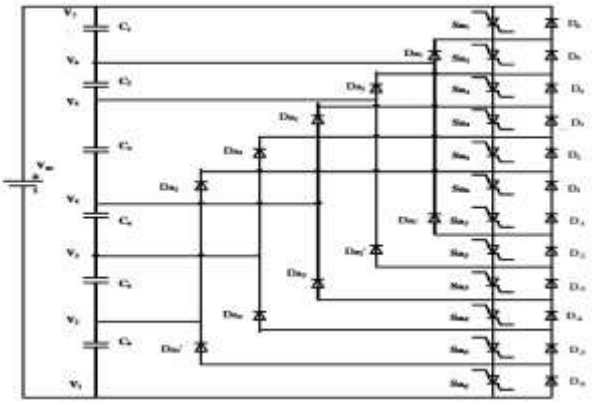

Figure 10 a seven-level diode-clamped converter

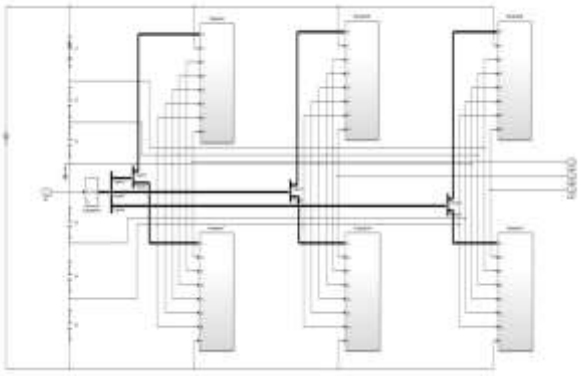

Figure 11 a Three phase seven-level diode-clamped inverter

Fig. 1(a) shows a seven-level diode-clamped converter in which the dc bus consists of four capacitors, C1, C2, C3, C4,C5 and C6. For dc-bus voltage Vdc, the voltage across each capacitor is Vdc/6, and each device voltage stress will be limited to one capacitor voltage level Vdc/6 through clamping To explain how the staircase voltage is synthesized, the neutral point n is considered as the output phase voltage reference point

Table I. Switching States of the Seven Level Inverter

Voltage (Vo)	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12
0	0	1	0	1	0	1	0	1	0	1	0	1
V_{dc}	1	1	0	0	0	1	0	1	0	1	0	1
$2V_{dc}$	1	1	0	0	1	1	0	0	0	1	0	1
$3V_{dc}$	1	1	0	0	1	1	0	0	1	1	0	0
$-V_{dc}$	0	1	0	1	0	1	0	1	1	1	0	0
$-2V_{dc}$	0	1	0	1	0	0	1	1	0	0	1	1
$-3V_{dc}$	0	0	1	1	0	0	1	1	0	0	1	1

There are seven types of voltage level in seven level inverter. i.e. 0v, Vdc/3, -Vdc/3, 2Vdc/3, -2Vdc/3,-Vdc and Vdc. Now for a particular voltage level there will be certain switch which will remain on and specific capacitors will discharge.

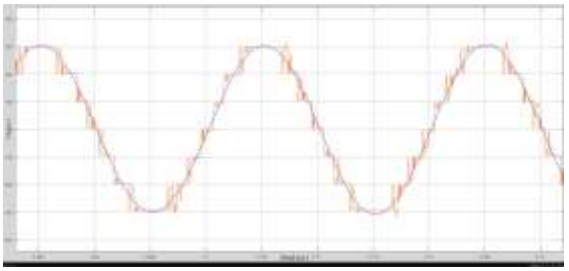

Figure 12 voltage level in seven level inverter

4 PROPOSED PR BASED CONTROL SCHEME

Here essential coordinate conversions are abc to αβ0 (Clarke transformation) and αβ0 to dq0(park's transformation)

$$\begin{bmatrix}0\\ \alpha\\ \beta\end{bmatrix} = \sqrt{\frac{2}{3}}\begin{bmatrix}\frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}}\\ 1 & -\frac{1}{2} & -\frac{1}{2}\\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2}\end{bmatrix}\begin{bmatrix}a\\ b\\ c\end{bmatrix}$$

$$\begin{bmatrix}d\\ q\\ 0\end{bmatrix} = \begin{bmatrix}\cos wt & \sin wt & 0\\ -\sin wt & \cos wt & 0\\ 0 & 0 & 1\end{bmatrix}\begin{bmatrix}\alpha\\ \beta\\ 0\end{bmatrix}$$

The reference current/voltage has been given in dq0 frame and converted in αβ0 frame.

$$\begin{bmatrix}v_\alpha\\ v_\beta\end{bmatrix} = \sqrt{\frac{2}{3}}\begin{bmatrix}1 & \frac{1}{2} & \frac{1}{2}\\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2}\end{bmatrix}\begin{bmatrix}v_a\\ v_b\\ v_c\end{bmatrix}$$

$$\begin{bmatrix}v_d\\ v_q\end{bmatrix} = \begin{bmatrix}\cos wt & \sin wt\\ -\sin wt & \cos wt\end{bmatrix}\begin{bmatrix}v_\alpha\\ v_\beta\end{bmatrix}$$

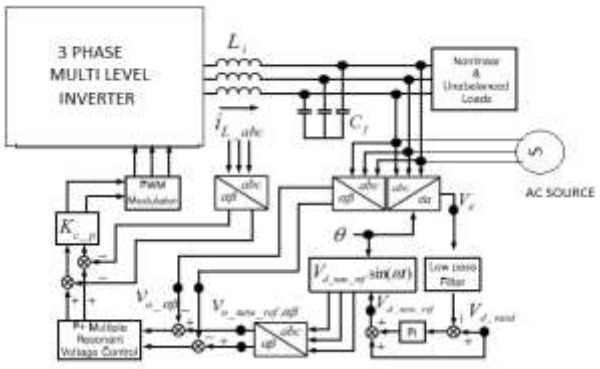

Figure 13 Proposed PR based output voltage control scheme.

Grid voltage v_a,v_b,v_c converted into v_α ,v_β using Clarke transformation. For generation ideal voltage $v_{ref\,abc}$ (with out harmonics) park's transformation is used abc to dq0 to get magnitude of voltage and noise reduced by low pass filter .pll is responsible wt in sin function as shown in fig.5.1. reference voltage $v_{ref\,abc}$ is converted in $v_{new\,.ref\,\alpha\beta}$ using Clarke transformation. Now Grid voltage v_α ,v_β is subtracting from reference voltage $v_{new\,.ref\,\alpha\beta}$ output is given to pr controller as shown in fig.5.1. inverter currrnt i_{labc} is converted in $l_{\alpha\beta}$ subtracting from pr controller output to get pure sinusoidal wave for PWM modulator

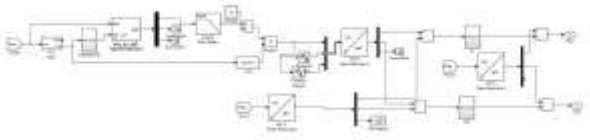

Figure 14 Proposed PR based in MATLAB.

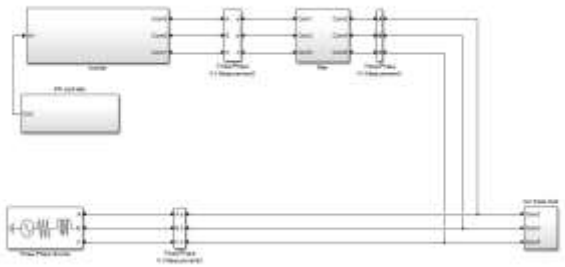

Figure15 proposed pr based inverter in matlab

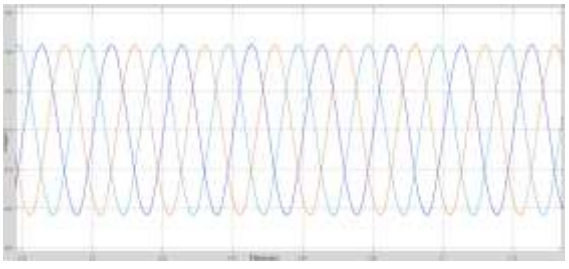

Figure 16 inverter output in matlab

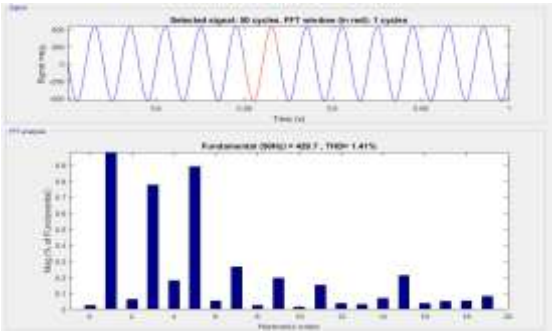

Figure 17 FFT analysis inverter output in matlab

5. CONCLUSION

The design of a proportional resonant controller for three phase 7 level inverter for grid connected applications. First the theoretical analysis has been done in the paper and the same is verified by the simulation results which is further validated by the experimental results. It can be observed that the THD is very minimal and follows the IEEE standards. The simulation results show that the proposed controller has good performance, steady state and transient, under nonlinear.

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