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Three Phase Interleaved Boost Converter

Prachi Shinde[1], Pradnya Ravindra Narvekar[2], Mahesh Manik Kumbhar[3]

[1,2]Assistant Professor, Department of E&TC, SGI, Institutes, Atigre, Maharashtra, India
[3]Assistant Professor, Department of E&TC, ADCET, Ashta, Maharashtra, India

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Abstract -*Step-up converter is proposed to achieve high voltage conversion ratio and high efficiency. This converter with an interleaved structure. The conventional interleaved boost converter for reducing input current ripples and output voltage ripples. Efficiency is increased by using the capacitance, inductor switches.*

Key Words: Interleaved boost converter, PWM.

1. INTRODUCTION

There are many industrial applications where DC–DC converter require high step-up voltage gain, like in the auxiliary power sup-plies, uninterruptible power supplies (UPS) for computers, portable electronic devices, and renewable energy systems [1–3].Furthermore, non-conventional and renewable energy sources, like photovoltaic (PV) panels and fuel cells (FC), generally require a high step-up converter due to their low DC output voltages. A conventional boost converter cannot provide such high voltage gains because of the narrow duty cycle available to them. Boost converters with higher voltage gains can theoretically be realized with an extreme duty-cycle design and application. Such high voltage gains, however are hard to achieve for many reasons, like the voltage stress on the power switches, large current ripples of inductance.

2. INTERLEAVED BOOST CONVERTER

Interleaved boost converter is used in high power application. The challenge of designing boost converter is to handle high current and voltage at input and output. 2 Phase Interleaved Boost Converter. The input current and output voltage ripple of interleaved boost dc-dc converter can be minimized by virtue of interleaving operation.

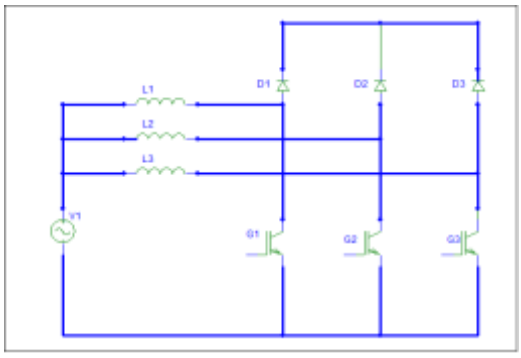

Fig.1 Interleaved boost converter

Input current can be shared among the two phases. The interleaved boost dc-dc converter consists of two parallel connected boost converter units, which are controlled by a phase-shifted switching function (interleaved operation). This converter has two parallel units; the duty cycle for each unit is equal to (Vout-Vin)/Vout. A phase shift should be implemented between the timing signals of three switches. Since there are three units parallel in this converter, the phase shift value is 180^0.

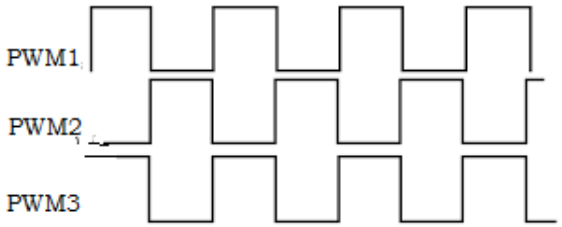

Fig.2 Timing Diagram of Control Signal

3. MODES OF OPERATION

1) STATE A: At time t0; M1 is closed and M2 are open. The current through inductor L1 starts to rise while L2 will continuously discharge.

2) STATE B: At time t1; M1 is closed and M2 is open. The current of inductor L1, starts to rise and L2 will continuously discharge.

3) STATE C: At time t2; M1, M2 is close. The current of inductor L1, L2 will rise.

4) STATE D: At time t3;M2 is close and M1 is open. The current of inductor L2, starts to rise and L1 will flow through the capacitor and capacitor will be charged.

5) STATE E: At time t5; M1, M2, are open. The current of inductor L1, L2, will continuously discharge and the capacitor will be charged.

Due to the symmetry of the circuit, the next state is similar to the previous state.

4. DESIGN CONSIDERATIONSDESIGN

The related equation between the duty cycle and the input/output volt-age gain for cascade boost converter. In the proposed converter, the gate signal duration applied to main switch is less than that of cascade boost converter

due to the delay at the start of the signal. This delay duration equals to the signal duration applied to auxiliary switch. Therefore, there is an effective duty cycle "Deff" for the proposed soft switched cascade boost converter as shown in Fig. 3. This effective duty cycle is equal to the sum of duty cycles of the main and the auxiliary switches. The equation between the input and output current of the proposed converter, which is assumed to be lossless in terms of effective duty cycle, can be expressed as;

$$\text{Deff} = 1 - (Vin/Vo)^{1/2} \qquad (1)$$

where, Io is the average value of the output current and I_{L1}, which is equal to input current value of L1.Determining passive components and delay time for the pro-posed auxiliary circuit was the key point of the study.

$$\text{Io} = (1 - D_{\text{eff}})^2 \cdot I_{L1} \qquad (2)$$

The aim was to obtain soft-switching at wide load ranges and at high switching frequencies. Eq. (3) shows that there is a relationship between the passive components' values, delay time td, output voltage Vo and second inductor current iL2. The minimum required delay time for proper ZVT operation can be obtained from

$$\text{td} \geq \frac{il2.Lr}{\text{Vo}} + \frac{\pi}{2} \cdot \sqrt{\text{Lr} \cdot \text{Cs}} \qquad (3)$$

It is clear that the minimum value for delay time needed to achieve proper ZVT operation depends on active-snubber circuit parameters, the lowest output voltage and the highest value of second inductor current. The proposed soft switching cascade boost converter draws maximum inductor current at rated power, and at the lowest input voltage. Furthermore, the passive elements of auxiliary circuit had to be chosen according to proper ZVT operation delay time, which lies somewhere at 5–10% of main switching period. To determine the proper delay time value, a small value inductor for Lr was chosen which also helps keep converter in a small physical volume. It is evident that the delay time value does not get affected from the capacitance Cr, which is used to transfer energy from auxiliary circuit to the output. The input inductor value L1 does not dominate the ZVT operation for the proposed converter. Under CCM operation, the inductor values L1 and L2 affect the input current ripple amplitude, along with current stress on the switches. Heir steady-state average currents can be expressed as follows

$$\text{Il1} = \frac{\text{Io}}{(1-\text{Deff})2} = \frac{\text{Io}}{(1-\text{Deff})4}$$

the current stress on the main switch is the sum of maximum values of currents through inductances, while the current stress on the auxiliary switch is the sum of min-imum values of (a) currents through inductances and (b) current through resonant impedance. The current stresses on D1 and D2 are related to maximum current value of L1 and the current stress on Do occurs at maximum current value of L2. These current stresses can be expressed as follows;

$$\text{IM,max} = I_{L1}\text{max} + I_{L2}\text{max}$$

$$\text{I,max} = I_{\text{Lr,max}} = I_{\text{L1min}} + I_{\text{L2,min}} + \frac{Vo}{Z1}$$

$$D1_{\text{max}} = ID2_{\text{max}} = IL1_{\text{max}}$$

$$IDo,_{\text{max}} = IL2_{,\text{max}}$$

4. SIMULATION RESULTS

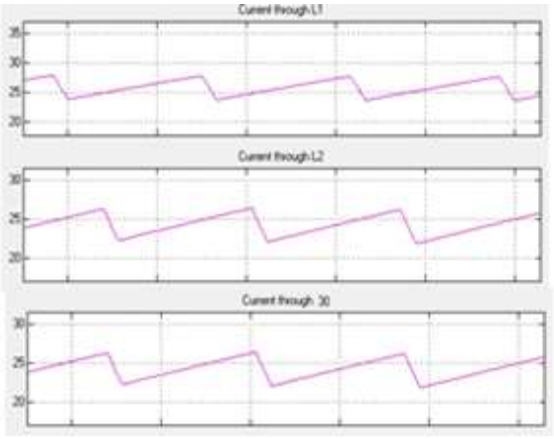

Fig.3 Current through Inductor

Simulation studies based on matlab were also carried out to verify the converter modes. The components and parameters used in the simulations, and experimental prototype itself with the above mentioned design considerations. The proposed soft-switching cascade converter was operated for several different conditions in order to fully display the performance of the controller and soft-switching conditions. The gate signals of the switches applied, which were obtained via DSP and powered with drive circuit, are given in Figs. 2 and 3 shows the output voltage of the converter under various input voltage values when the closed loop voltage controller was active.

5. CONCLUSION

In this study, design considerations and simulation results of an soft-switching cascade boost converter are presented. This converter has a wider turn-off period, higher voltage gain and lower switching losses compared to classical boost converters. Not only the main switch of the proposed converter turns on under ZVT and off under ZVS conditions, Furthermore, the diodes used in the proposed converter turn on and turn off under soft-switching without any voltage stress. The operation principles and design considerations of the proposed soft

switching cascade boost converter are demonstrated within the paper as well.

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