SEVEN LEVEL REVERSING VOLTAGE INVERTER

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Abstract - Multilevel inverters are an essential part of high-power high-voltage applications. They have highly superior performance when compared to conventional inverters in terms of reduced harmonic distortion, lower electromagnetic interference, and higher dc link voltages. At the same time, they have certain disadvantages such as increased number of components, complex pulse width modulation control method, and voltage-balancing problem. A new topology that compensates the above-mentioned disadvantages is proposed in this paper. This topology with a reversing-voltage component requires fewer components (particularly in higher levels), fewer carrier signals and gate drives. Hence, the overall cost and complexity are greatly reduced particularly for higher output voltage levels.

***KeyWords:* multilevel; switches; topology; reversing-voltage; polarity; SPWM**

1.INTRODUCTION

Multilevel converters, which began with the three-level converter was first introduced in 1975[3]. Subsequently, numerous multilevel topologies were proposed. The elementary concept involves using a high number of active semiconductor switches with several low voltage dc sources to produce a staircase voltage waveform in small voltage steps. This has several advantages such as low voltage stress(dv/dt) on the load, production of quality waveform and reduced electromagnetic compatibility problems. Series connection of several power semiconductor switches give rise to overvoltage which is eliminated by using clamping diodes. Furthermore, the switching can be staggered as the switches are not truly series connected. This reduces the switching frequency which leads to lower switching losses [1].

One of the main disadvantage of multilevel power conversion is that a higher number of semiconductor switches are required. But since lower voltage rated switches are used in the multilevel converter, the active semiconductor cost is not appreciably increased. However, the converter mechanical layout is very complex as each active semiconductor added requires associated gate drive circuits. Another disadvantage of multilevel power converters is that isolated voltage sources may not always be readily available, and series capacitors require voltage balancing.

Although multilevel conversion presents a great deal of challenges, they offer a wide range of possibilities. Researches are going on to improve energy efficiency, reliability, power density, simplicity, cost, and to broaden the application field.

In recent years, there has been a substantial increase in interest to multilevel power conversion. This has led to the introduction of novel converter topologies such as cascade converter, neutral-point clamped (NPC) inverter, and flying capacitor inverter. Combinations of these topologies such as cascade 3/2 multilevel inverter which is a series combination of a two-level converter with a three-level NPC converter and cascade 5/3 multilevel inverter which is a series combination of a three-level cascade converter with a five-level NPC converter have also been proposed.

These converters find numerous applications in industrial drives, flexible ac transmission systems (FACTS) and vehicle propulsion. One particularly suitable area for multilevel is that of renewable photovoltaic energy where efficiency and power quality are of great concerns for the researchers.

Train traction power conversion systems is another interesting field of application for multilevel converters. Traction drives are in the medium-voltage high-power range and require very high performance over a wide range of frequencies up to high speed. High switching frequencies are necessary to achieve high speed. High frequency switched output waveform is produced by multilevel power converters without increasing the average switching frequency. The switching frequency is further reduced as the additional levels intrinsically improve the voltage THD.

Recently some topology utilizing low-switching-frequency high-power devices have also been suggested. Though the modifications made reduces the output voltage distortion, it has significant low-order current harmonics. The pulse width modulation (PWM) method employed also makes it difficult to manipulate the magnitude of output voltage.

A new multilevel inverter topology named reversing voltage (RV) which requires less number of components when compared to conventional topologies is presented in this paper. In this topology, the power conversion is divided into two parts of which one operates at line frequency thereby leading to reduced number of high frequency switches. Hence it has simpler and more reliable control. Switching sequences in this converter are easier than its counter parts. This paper describes a seven-level inverter based on reversing voltage topology. The inverter is driven by the general method of multilevel modulation phase disposition SPWM.

2. WORKING DESCRIPTION

2.1 Circuit Description

Conventional multilevel inverters use power semiconductor switches to produce the bipolar levels of the output waveform. However, the positive and negative polarity of the output waveform can be produced without using all the switches. This is done by separating the power conversion in two parts.

One part is responsible for generating the positive polarity of the output waveform and is known as level generation part while the other part is responsible for generating the polarity of the output waveform and hence, is called polarity generating part. The level generating part requires high frequency switching operation, therefore the switches used in this part must have high switching frequency capability. The polarity generating part is a low frequency part which operates at line frequency.

The high frequency and low frequency parts are combined to form the complete multilevel voltage output. The polarity generating part is a full bridge inverter which inverts the positive level to generate the required polarity for the output. In doing so, many of the semiconductor switches required to produce output levels can be eliminated.

The RV topology to produce seven levels requires ten switches and three isolated sources as shown in Fig. 1.

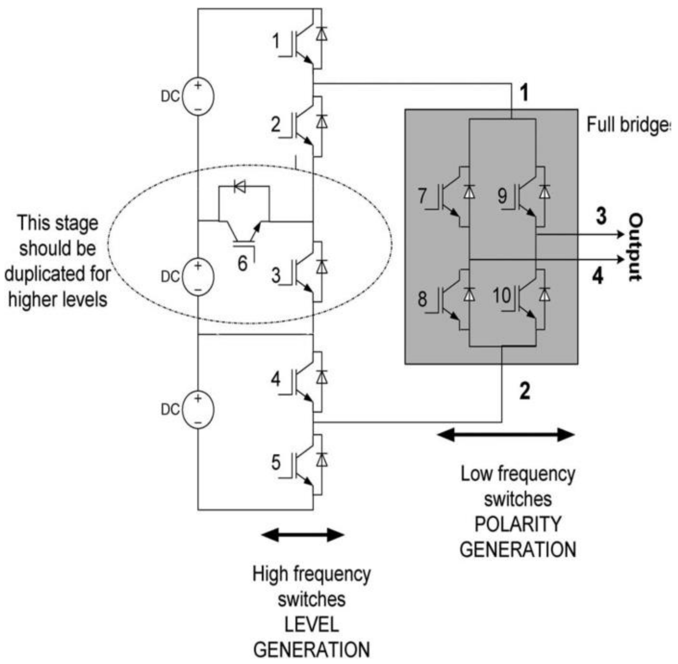

Fig -1: Schematic diagram of seven level inverter

The left stage in Fig. 1 is the level generating part which generates the required output levels without polarity. The right stage of the circuit is a full bridge converter which decides the polarity off the output voltage. This stage transfers the output level to the output with same or opposite direction based on the required output polarity.

2.2 Switching Sequences

This topology has easier switching sequences compares to other converter topologies. Generation of negative pulses for negative cycle control is eliminated. Instead, the required level is produced by the level generating part which is the translated to the required polarity according to output voltage requirements.

The switching sequence in this topology is redundant and flexible. The various switching modes in generating the required levels is shown below.

Levels	Switching Sequences
Level 0	2-3-4
Level 1	2-3-5
Level 2	2-3-6
Level 3	1-5

As shown above, the sequence sequences of switches (2–3-4), (2-3-5), (2-6-5), and (1, 5) are chosen for levels 0 up to 3, respectively. These sequences are shown in Fig. 2. As can be observed, this part generates the output voltage levels by appropriate switching sequences. The output voltage is the sum of the voltage sources which are includes in the current path.

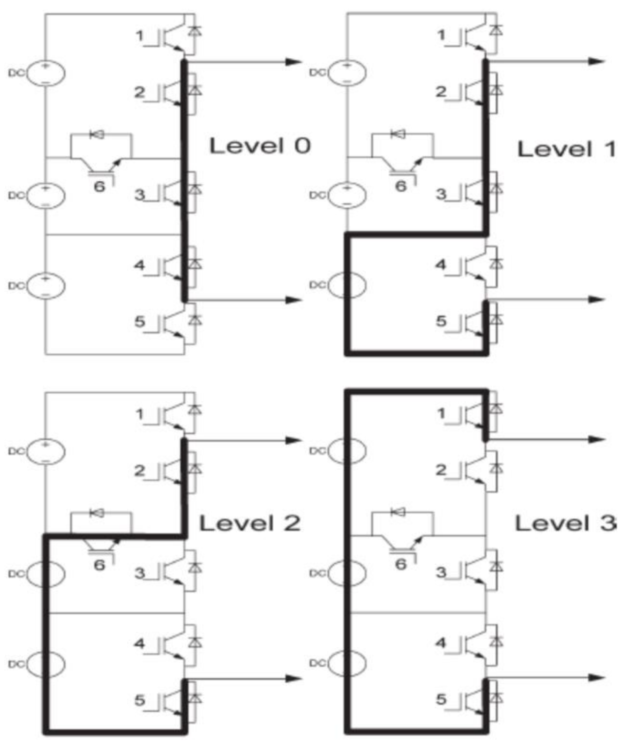

Fig -2: Switching sequence for various level generation

3. CIRCUIT IMPLEMENTATION

SPWM is adopted for switching due to its simplicity. An Arduino UNO is programmed to generate the necessary gate pulses for the switches. The Arduino provides an output signal that typically is limited to a few milliamperes of current. Hence, the transistor will take quite some time to switch leading to power loss. Also, the gate capacitor of transistor causes a current overdraw during switching as it draws current quickly. This causes overheating which leads to permanent damage or even complete destruction of the chip. A gate driver is used to prevent this from happening.

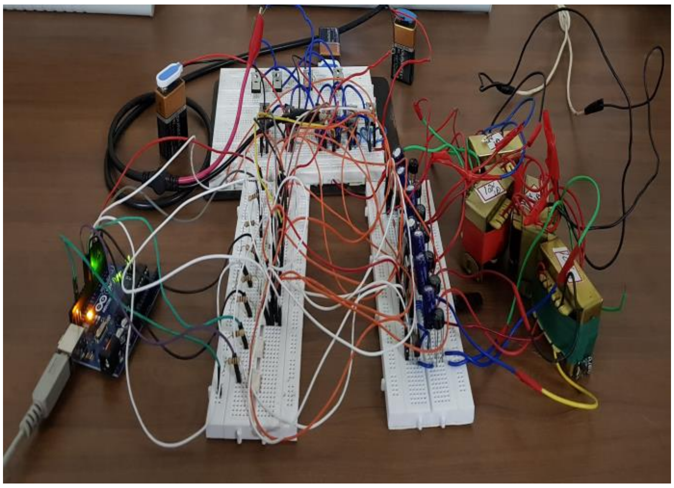

Fig-4: Seven level reversing voltage inverter prototype

4. CONCLUSIONS

In recent years, there has been a substantial increase in interest to multilevel power conversion. Various topologies and combinations of these topologies have been proposed. The reversing voltage topology is based on the principle idea of generating the output waveform in the positive polarity and then feeding it to a full bridge inverter to produce the output waveform in both positive and negative polarity. By doing so, the required number power switches are reduced. Also, this topology has superior features in terms of isolated supply, control requirements, cost, and reliability. Since the switching is divided into high frequency and low frequency, the efficiency is improved, and its cost is reduced.

5. REFERENCES

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