Reconfigurable Architecture for QAM Modulators

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Abstract: Quadrature modulation (QAM) is employed in each analog and digital communication. During this technique, each amplitude and phase variation of the carrier with regard to digital information or data. It provides a high rate of transmission. QAM is employed in several application like color TV, Wi-Max, OFDM (Orthogonal Frequency Division Multiplexing), and in digital satellite communication system. FPGAs give an impressive platform for implementation of any kind of algorithms. The FPGA technology has been playing a significant role in transportable and mobile communication owing to the feature of configurability in planning and implementation. The main objective of this work is to discuss the effectiveness of FPGA based QAM modulators. Availableness of additional modulators in DSM demands additional FPGA resources, but within the testing set up only one form of a modulator of DSM is needed for any purpose in time. Thus the resources used by different modulation techniques become overhead. In order to scale back, this overhead reconfiguration is a perfect answer. This paper presents an approach for the implementation of two modulators mainly 4-QAM and 16-QAM in VHDL by means that of Xilinx 14.7 and simulation in Modelsim. The same modulators have conjointly been developed in MATLAB.

Keywords*:* QAM, FPGA, MATLAB, VHDL

I. INTRODUCTION

Digital communication is widely used recently. The development of digital communications desires not an exclusively high performance of hardware systems but to add flexibility in style and implementation. FPGA offer flexibility for implementing fully totally different communication techniques. To add, area and power improvement could also be done by using HDL (Hardware Description Language). A system-level style that has been developed recently, like System Generator, makes style tasks lots of easier than it's ever been before. Designers can merely check algorithms, perform the total system or modify and update diagram shortly. For this reason, system level style is participating in a very extensive role in implementation and improvement.

Quadrature modulation offers higher rate transmission as compared to the BPSK and QPSK modulation technique. QAM is mixtures of both ASK and PSK modulation technique as a result of that additional variety of subchannel are often used to transmit over one channel. Field programmable gate array made of semiconductor material that contains programmable logic elements (LEs) and reconfigurable interconnects to make any combinational or sequential logic functions. Hardware-enforced in an FPGA is often reconfigured by programming the logic components and interconnections for specific applications. Reconfiguration is that the feature provided by the FPGA through that functionality of the FPGA will change on the fly whereas device is performing any task or specific application. The advantage of this feature is, it offers the additional flexibility to vary the appliance using the same hardware and since of partial reconfiguration time need to change from one modulation technique to a different is reduced. As a result of that rate are often adjusted as per the need.

II. LITERATURE SURVEY

In paper [2] author implemented the digital modulator such as QAM, BASK, BFSK, BPSK which are used in modern wireless technique such as software-defined radio and cognitive radio. In this, the input signal and carrier signals are generated using the CO-ordinate Rotation Digital Computer (CORDIC) algorithm. These modulations techniques develop in VHDL and then implemented individually on Spartan 3 FPGA board.

In paper [3] author gives the simulation of QAM in Simulink. In this paper using the Simulink block set, implemented the QAM modulation and demodulation and parameter setting for different blocks such as QAM modulator/demodulator, random integer, AWGN channel, Error rate calculation are given.

In paper [4] authors explained basics of QAM and its variants with constellation diagram very properly. This paper concluded that QAM is the most appropriate modulation scheme for an OFDM based wireless broadband communication system because it contains higher data rate with less bandwidth.

In paper [5], authors had given a brief introduction to FPGA and its topology. Dynamic partial reconfiguration and its three design methodology are explained. The design flow of partial reconfiguration for the vertex 5 board is explained with the flow chart method. Using above five important papers concept and methodology of the QAM implementation on FPGA using the reconfiguration is achieved.

III. PROPOSED METHOD

A. Implementation of QAM Modulators

In QAM, the amplitude of two carrier waves is dynamically based on the incoming bits stream. The primary carrier may be a cosine wave whereas the second one is a sine. These two carriers have a similar frequency. QAM is taken into account as a mixture of ASK and PSK since the output modulated signal has amplitude and phase variations. Fig.1 may be a general lager block diagram of QAM generator. In QAM, higher spectral efficiency is often achieved however with a higher chance of error.

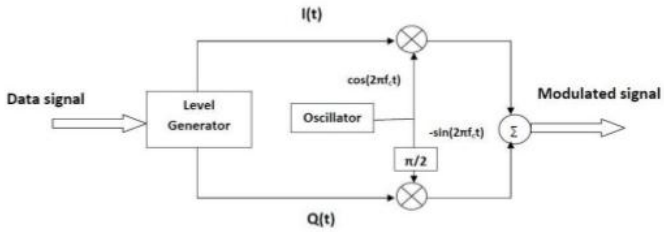

Fig. 1. Block diagram of QAM generation

The simplest kind of QAM modulation is 4QAM that has the constellation diagram shown in Fig. 2. So as to implement this type of modulation, two sinusoidal waves were needed. These two waves have 90-degree phase distinction. The best way to do this in VHDL is by using LUT.

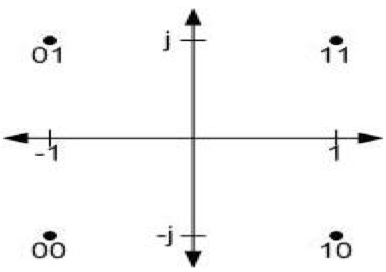

Fig. 2. Constellation diagram

The diagram of the 4QAM implementation in VHDL is shown in Fig. 3. The diagram appearance almost like our QPSK one with some variations. The most distinction here is: we have a tendency to need two carriers only in 4QAM whereas in QPSK four carriers were required. The adder circuit provides 4 QAM wave combinations of the I-signal and Q-signal supported the incoming information signal.

The second step in the QAM implementation is implementing 16QAM that has the constellation diagram shown in Fig. 3. As in 4QAM, two carrier waves were required for the implementation as illustrated within the block shown in Fig. 1. Currently, the serial to parallel device circuit converts the incoming information into four parallel outputs instead of two as in 4QAM.

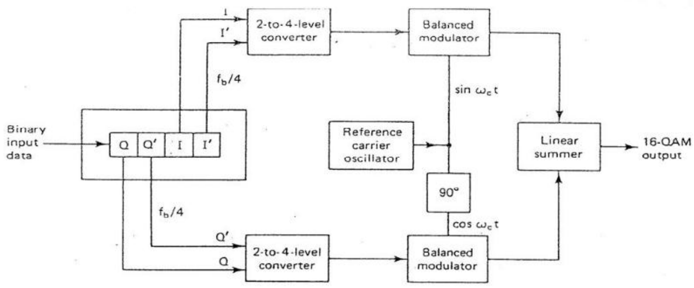

Fig. 3. Block diagram of the 16-QAM generation

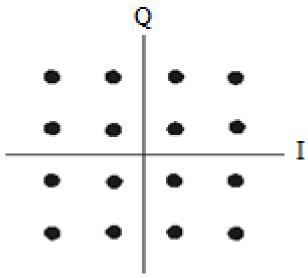

Fig. 4. Constellation diagram

in FPGA implementation of digital modulation techniques like QAM, QPSK, BPSK etc., the most task is to come up with periodic waveforms like sin and cosine. Look up table technique is most proven and widely used technique to generate such periodic waveforms in FPGA. It involves reading a series of stored information values that represent the waveform. Upon feeding these digital values to DAC, DAC outputs analog waveform as shown in

For 4-QAM and 16-QAM two tables each are required to store the I-phase and Q-phase signals. In QAM the stored values generate the waveform of varied amplitude. Different look-up tables are the only difference between the two modulation implementations. In DSM, only one type of modulation technique needs to be active at any point in time. It means that though 4-QAM and 16-QAM lookup tables are present on FPGA only one will be used at a time. It means the requirement of look-up tables is mutually exclusive in modulation techniques.

The look-up table (LUT) is used to store the sample points for the generation of I-phase and Q- phase signals. The proposed system requires four looks up tables. Among these lookup tables, two of them consist of I-phase and Q- phase signals of a 4-QAM. Similarly, the rest consists of I-phase and Q- phase signal of 16 QAM.

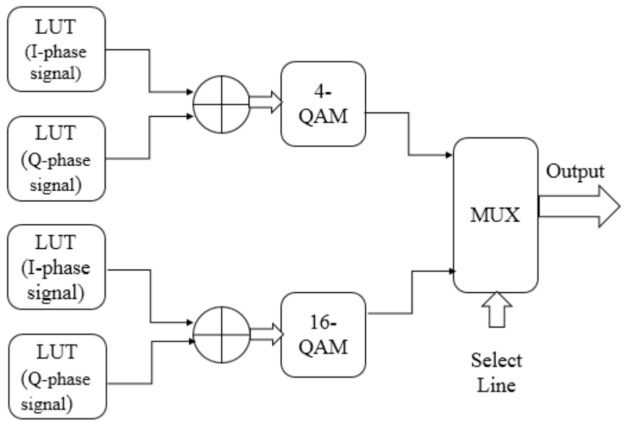

Fig.5 Proposed Block Diagram

The sample points are calculated based on an input digital data and stored in a look-up table for further processing. 4 LUT is used for the QAM generation. A 2:1 mux is used to facilitate the switching of the QAM signals to the output. The only select line will be sufficient if the contents of LUTs can be changed on the fly to change the modulation technique.

The steps used to implement 4-QAM and 16-QAM techniques on FPGA is shown in Fig. 6.

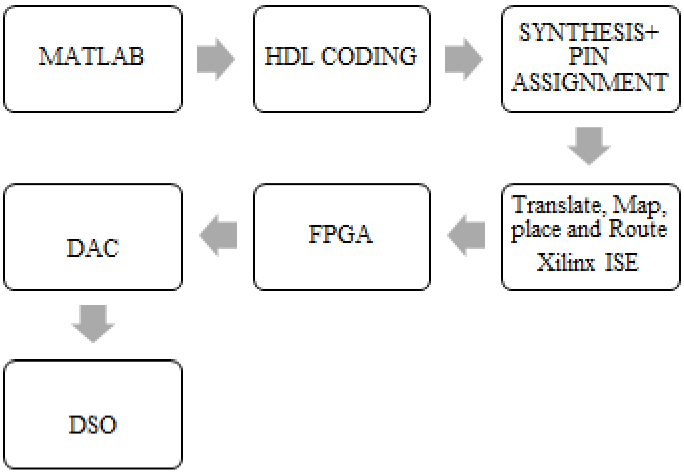

Fig.6 Design Flow for Proposed System

IV. IMPLEMENTATION

The implementation can be divided into 3 phases. Phases I and II consists of generating and synthesizing 4-QAM and 16-QAM modulators and implementing each modulator. Reconfiguration generation and implementation can be carried out in phase III. Initially, both techniques can be simulated using Matlab R2013a. Modulators can be simulated and synthesized using ISE web-pack 14.7. Simulation results of QAM and 16-QAM are shown in Fig. 7 and Fig. 8 respectively.

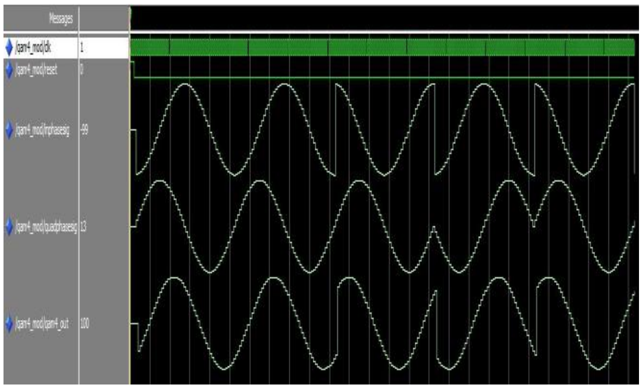

Fig.7 Simulation results of QAM

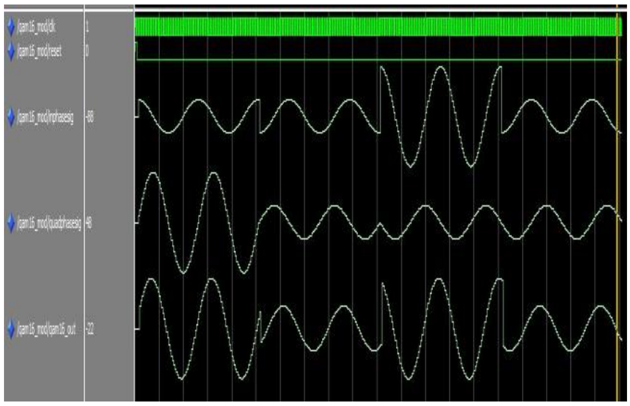

Fig.8 Simulation results of 16-QAM

In phase I and II, to generate the QAM and 16-QAM random input bits can be used. Generated I-phase and Q-phase signal for both system using MATLAB. Sample values for I-phase signal and Q-phase signal are stored in LUTs then VHDL coding is used for generation of QAM signal.

In phase III, Multiplexer can be used to change the System contents. A bitstream is generated that programs only the difference between the two versions of a design. The implementation is testable on Spartan 3E FPGA board. The FPGA crystal frequency is 50 MHz. The bit files are downloaded on the FPGA using Boundary Scan mode with USB.

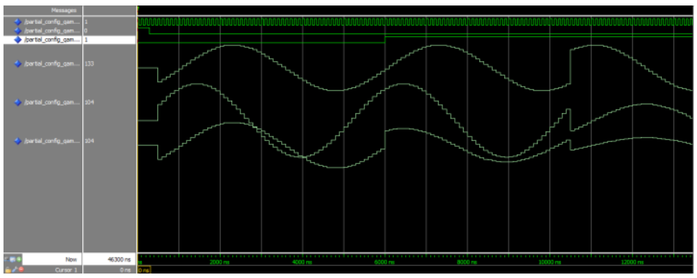

Fig.9 Simulation results of reconfiguration QAM system

The DAC is connected to digital storage oscilloscope in order to display real-time results in an analog domain

V. RESULT

The modulator was coded in Verilog HDL and was implemented on Spartan-3E FPGA with all the two above designs. The Xilinx synthesis tool which generates synthesis report mentioning the area utilized by the entire implementation of both design is described in Table 1.

Table.1 Device Utilization for FPGA

Logic Utilization	4-QAM	16-QAM	Configured System
Number of Slice Flip Flops	44	48	98
Number of 4 input LUTs	292	573	904
Number of occupied slices	158	435	584
Number of Slices containing only related logic	158	435	584
Number of Slices containing unrelated logic	0	0	0
Total Number of 4 input LUTs	307	592	913
Total Number of 4 input LUTs	292	573	876
A number used as a route-thru	15	19	37
Number of bonded IOBs	11	11	12
Number of BUFGMUXs	1	1	1
Average Fanout of Non-Clock Nets	5.30	4.24	4.44

VI. CONCLUSIONS

A case study of QAM modulators using difference based on the fly system for DSM is presented. The system consists of two modulation techniques 4-QAM and 16-QAM. This can easily be extended to other modulation techniques without increasing the resource requirement. Though only two modulation techniques are taken as the case study the observed benefits are independent of this number. Hence the feature permits incorporating a virtually infinite number of LUT based modulation techniques without extra resource requirement. Good amount saving in resource utilization is observed by using reconfiguration feature. reconfiguration is the right choice for the applications where resources are not enough on the device or big application is to fit on the small device.

Use of reconfiguration feature also makes the system easy and quick to adapt to the change in environment or as per need. Hence it is a promising solution to the challenge raised by testing of communication receivers supporting multiple channels and multiple modulation techniques

B. Applications

QAM is widely used in applications

1. IEEE 802.11 (Wi-Fi),
2. IEEE 802.16 (Wi-MAX),
3. Digital Video Broadcast (DVB),
4. MODEMs,
5. 3G wireless technologies.

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