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An FPGA implementation of 2D filter using Vedic multiplier

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Abstract -*In the modern world of digitization, processing of data in real time requires an increase in the operating speed of a system. Multiplication operation forms the core of many extensively used techniques like correlation, convolution filtering etc. and which is time consuming in many DSP applications. Convolution filters perform convolution of the images using multiplication operation. The incorporation of the Vedic multiplier in the convolution filter enhances the speed of the multiplication operation. The Vedic multiplier uses Urdhva-Tiryabhyam sutra i.e., vertically and crosswise multiplication to implement 32x32 Bit Vedic multiplier to generate partial products reducing the number of iterations and reduce time consumption. A conventional way of performing multiplication between two numbers can be adopted using Vedic mathematics. MATLAB is used to design the convolution filter. The Vedic multiplier design is coded in VHDL.*

Keywords- **Convolution, Gaussian filter, Image processing, Urdhva-Tiryabhyam sutra, Vedic multiplier**

1. INTRODUCTION

The Smoothing and edge detection are the techniques used to reduce noise in images for further processing. In convolution filters the Gaussian filters are used for smoothing the image.

1.1 Gaussian filter

A Gaussian filters in electronics and signal processing is a filter whose impulse response is a Gaussian function with no overshoot to a step function input while minimizing the rise and fall time. The effect of Smoothing results in blur image. In weighted smoothing, depending on the convolution kernel matrix, weighted smoothing can be adopted, which implies that the contribution of particular pixels to the resulting brightness is weighted. Convolution kernels are often chosen to be small-scale, such as 3x3, 5x5 or 7x7, since enlarging the size of a convolution kernel results in the increased level of blur. The rectangular uniform convolution kernel 3x3 matrix with σ=0.6,

$$\frac{1}{16}\begin{bmatrix}1 & 2 & 1\\ 2 & 4 & 2\\ 1 & 2 & 1\end{bmatrix} \quad \ldots\ldots\ldots\ldots\ldots (1)$$

The Gaussian convolution kernel can be generated using

$$G(x,y) = \frac{1}{2\pi\sigma^2} e^{-\frac{-(x^2+y^2)}{2\sigma^2}} \quad \ldots (2)$$

The image is convolved with the above matrix using convolution. Convolution involves multiplication. In the proposed design, a 32-bit Vedic multiplier is incorporated to perform multiplication operation.

1.2 Vedic multiplier

In the early twentieth century, the rediscovery of the ancient Indian system of mathematics was given the name Vedic mathematics which enhances the computational speed from ancient Indian sculptures (Vedas). In Microprocessors, DSP and communication applications, multiplication play an important role. Almost all the operations are based on multiplication. The demand for processor with high speed and low power consumption multipliers is also increasing. The Vedic multipliers are very fast and require less hardware to improve computational speed. Vedic mathematics is a methodology of arithmetic rules and with some effective algorithms for speed improvement.

The proposed design uses 32bit Vedic multiplier for multiplication operation in binary number system. The multiplier uses Urdhvatiryagbhyam sutra literally means "vertically and crosswise" generating partial products with concurrent addition of partial products, the area increase slowly with increased number of bits in comparison to conventional multipliers. The block diagram of a 32x32 Vedic multiplier is shown in figure1

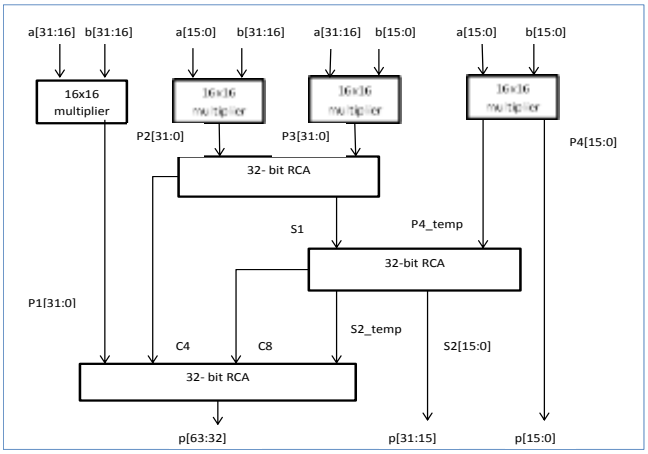

Fig -1: 32x32-bit Vedic multiplier

2. Results and Analysis

The Gaussian filter is designed in MATLAB, the 32-bit Vedic multiplier is designed in VHDL on Xilinx 14.5 and simulated with the image in figure2 shown below. Figure2a represents the input image and the figure2b represents the reconstructed filter image. The block diagram of convolution filter is shown in the figure2.

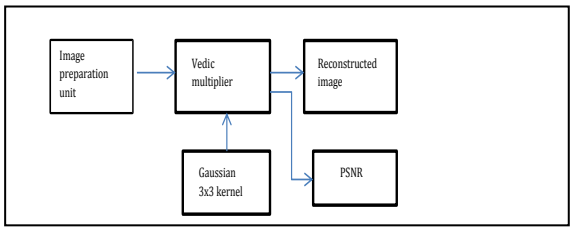

Fig -2: Block diagram of convolution filter

Fig -2a: Input image

Fig -2b: Reconstructed filter image

Table-1: Comparison of different Gaussian Filter design

Design	MA-GSF	GF_LASCAS	GF_VEDIC
Delay(ns)	3.64	4.38	2.371
PSNR	23.4	7.14	15.5

It can be observed from the table the Vedic multiplier computes multiplication faster compared to other existing filter architecture [1]. The PSNR is between the MA-GSF and GF_LASCAS architectures

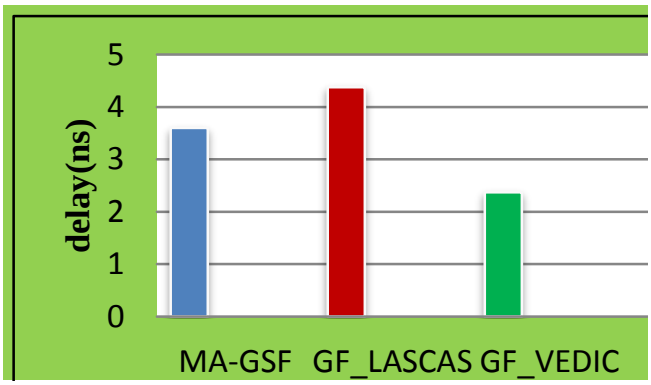

Chart -1: Delay of different architectures

3. CONCLUSIONS

This paper presents an implementation of the Gaussian Filter architecture with 32-bit Vedic multiplier for image processing. The multiplier performs faster multiplication compared to other architectures as in table1 with reduced delay. The filter design is implemented in MATLAB and the 32-bit Vedic multiplier is designed in Xilinx 14.5. The design operates at maximum frequency of 421.852MHz with a delay of 2.371ns.

REFERENCES

[1].Mrinal Dubey and Shweta Agarwal,"An analysis of Energy Efficient Gaussian Filter Architectures", International Research Journal of Engineering and Technology (IRJET), 2017.

[2]. Mr. S.S.Mohanasundaram, A.Nirmal kumar, T.Arul prakash," Design of Floating Point Multiplier Using Vedic Mathematics", International Journal of Innovative Science, Engineering & Technology, Vol. 2 Issue 1, January 2015.

[3]. V. S. S. Prasad, J. Mathews, and N. Naganathan, "Low power design strategies for mobile computing, in VLSI Design, 19th Int. Conf. on, pp. 2, Jan 2006.

[4]. J. Canny, A computational approach to edge detection, IEEE Trans. Pattern Anal. Mach. Intell. PAMI-8 (November 1986) 679–698

[5]. Leila kabbai, Anissa Sghaier, Ali Douik and Mohsen Machhout," FPGA implementation of filtered image using 2D Gaussian filter", 2016.

[6]. L. Rao, B. Zhang, J. Zhao, Hardware Implementation of Reconfigurable 1D Convolution, Journal of Signal Processing Systems, 82(1), pp. 1-16, 2016.

[7]. S. Khorbotly, F. Hassan, A modified approximation of 2D Gaussian smoothing filters for fixed-point platforms, in: IEEE 43rd Southeastern Symposium on Sys- tem Theory (SSST), March 2011, pp. 151–159.

[8]. P.Y. Hsiao, C.H. Chen, S.S. Chou, L.T. Li, S.J. Chen, A parameterizable digital- approximated 2D Gaussian smoothing filter for edge detection in noisy image, in: Proceedings IEEE International Symposium on Circuits and Systems, May 2006, 4, pp. 3189–3192.

[9]. Jaiswal, B. Garg, V. Kaushal, G. Sharma, SPAA-aware 2D Gaussian smoothing filter design using efficient approximation techniques, in: Proceedings of 2015 28th International Conference on VLSI Design (VLSID), 2015, pp. 333–338. IEEE.

[10]. Sunil Kumar Kopparapu and M Satish," Identifying Optimal Gaussian Filter for Gaussian Noise Removal" Third National Conference on Computer Vision, Pattern Recognition, Image Processing and Graphics 2011.