International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395-0056
Volume: 05 Issue: 05 | May-2018 www.irjet.net p-ISSN: 2395-0072

High Efficiency Soft Switching isolated AC-DC Converter with FUZZY Controller

N.Keerthana[1], SP.Umayal[2]

[1] *Student, Dept. of Electrical and Electronics Engineering, Muthayammal Engineering College, Tamilnadu, India*
[2] *Professor/ Dean, Dept. of Electrical and Electronics Engineering, Muthayammal Engineering College, Tamilnadu, India*

Abstract - *A high efficiency isolated AC-DC converter topology is proposed. The proposed converter consists of a full bridge diode rectifier, an isolated resonant dc-dc converter, and a controller. By using the novel control algorithm that control both power factor and output power, the converter performs AC-DC conversion in a single power processing step. The converter regulates the input current and output power by adjusting the PWM of switches. To obtain high power density, the proposed converter provides soft switching for all components. The converter provides high power quality, producing a high power factor and low total harmonic distortion without requiring a power factor correction circuit. It employs an active-clamp circuit and a series resonant circuit. The active clamp circuit increases conversion efficiency by reducing the switching losses on the switches and by recycling energy stored in the leakage inductance. Moreover, this circuit limits voltage stresses across the switches and avoids damage caused by the surge voltage. A series resonant of the output voltage doubler circuit removes the reverse recovery problem of the output diodes. These features enable the proposed converter to provide high efficiency, high power density and a high power factor.*

Key Words: **power factor correction (PFC), total harmonic distortion (THD), zero current switching (ZCS) and zero voltage switching (ZVS).**

1. INTRODUCTION

With an increase in the use of ac–dc converters in various industrial fields, demand for the development of an AC–DC converter with high efficiency and high power density has increased.

Traditionally, AC–DC converters with a two-stage circuit configuration have been widely used [1]-[3]; they consist of an AC–DC converter with power factor correction (PFC) [4], [5] followed by an isolated DC–DC converter [6]-[9] and provide nearly unity power factor and reliable output regulation. The single-stage converter which is simple and cost effective is developed based on various converter topologies like fly-back, forward converter, and a full bridge converter. But it contains a complex circuit structure and causes additional power loss.

This paper presents an AC–DC converter with high efficiency and high power density. The proposed converter consists of a full-bridge diode rectifier, an isolated resonant dc–dc converter, and only one controller. Series resonance is used to increase efficiency and soft switching technique is used to obtain high power density. Therefore, the converter provides high power quality, producing a high power factor and low total harmonic distortion (THD) without requiring a PFC circuit.

2. PROPOSED SOFT SWITCHING AC-DC CONVERTER

The proposed circuit represents the circuit diagram of AC-DC converter using Fuzzy Logic Controller.

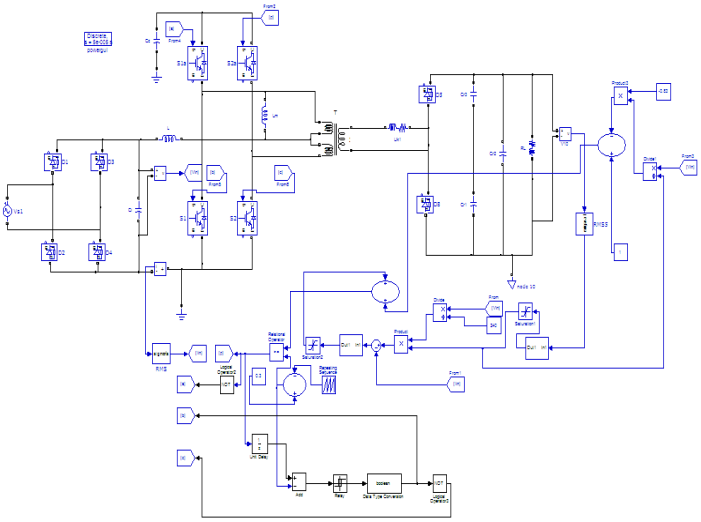

Fig -1: Circuit configuration and control block diagram of the proposed converter

It consists of a full-bridge diode rectifier, an isolated resonant DC–DC converter, and a controller. As shown in Fig-1, the proposed converter controls both the input current and the output voltage with only one controller; this is different from conventional single-stage AC–DC converters, which perform only output regulation.

The dc–dc converter is derived from a current-fed push–pull converter. It employs an active-clamp circuit and a series resonant circuit. The active-clamp circuit is composed of the auxiliary switches S_{1a}, S_{2a} and the clamping capacitor C_c. The active-clamp circuit increases conversion efficiency by reducing the switching losses on the switches and by recycling energy stored in the leakage inductance L_{lk}.

Moreover, this circuit limits voltage stresses across the switches and avoids damage caused by surge voltage. The series resonant circuit consists of the leakage inductance L_{lk} and a voltage doubler rectifier circuit. This resonant circuit alleviates the reverse recovery problem on the rectifier

diodes D_1 and D_2 by providing zero-current switching (ZCS) turn-off for the diodes.

2.1 OPERATION PRINCIPLE

The proposed converter regulates the input current and output power by adjusting the pulse width modulation signals of the switches. The circuit operates in six modes of operation.

Mode 1a [t_0, t_1]:

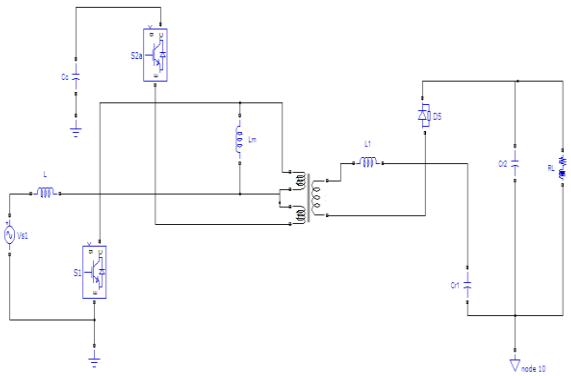

Fig -2: Mode1a

At t_0, the switch S_1 is turned on. At that time, i_{p1} flows through the body diode of S_1, so that S_1 is turned on in the zero-voltage state.

In this mode, the power is transferred to the output across the transformer. The secondary current *is* flows through D_1.

The angular resonant frequency ω_r and the characteristic impedance Z_r of the resonant circuit is given by

$$\omega_r = \frac{1}{\sqrt{L_{lk} C_r}}, Z_r = \sqrt{\frac{L_{lk}}{C_r}} \quad (1)$$

At the end of this mode, the resonance is complete and secondary current i_s becomes zero.

Mode 2a [t_1, t_2]:

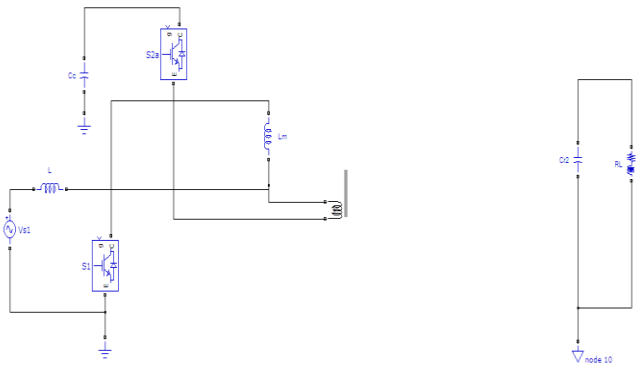

Fig -3: Mode 2a

At t_1, the diode current i_{d1} becomes zero and diode D_1 is turned off with zero current switching (ZCS); this means that D_1 does not incur reverse recovery loss. In this mode, i_m still increases linearly and is equal to i_{p1} because no current flows on the secondary side.

Mode 3a [t_2, t_3]:

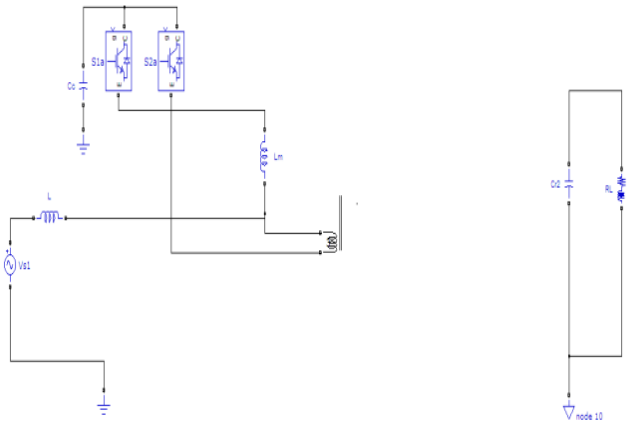

Fig -4: Mode 3a

In this mode, the switches S_{1a} and S_{2a} conduct. During this interval, voltages v_{p1} and v_{p2} are zero and current i_m is held constant.

Mode 3b:

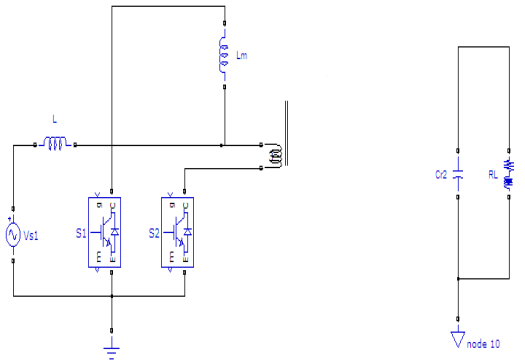

Fig -5: Mode 3b

The gate signals of the switches S_1 and S_2 are overlapped during this mode when D≥0.5. During this interval, voltages v_{p1} and v_{p2} are zero and current i_m is held constant, as in *Mode 3a* for $D < 0.5$.

From the volt-second balance for L, the clamp capacitor V_c can be derived as,

$$V_c = \frac{V_i}{1-D} \quad (2)$$

The relationship between the input voltage and the output voltage is represented as,

$$\frac{V_0}{V_i} = \frac{N_s}{N_p}\frac{1}{1-D} \quad (3)$$

2.3 CONTROL ALGORITHM FOR SINGLE-POWER-CONVERSION METHOD

The proposed converter does not include an additional circuit for PFC. Thus, a control algorithm for both input current and output voltage regulation with only one power-conversion process needs to be incorporated.

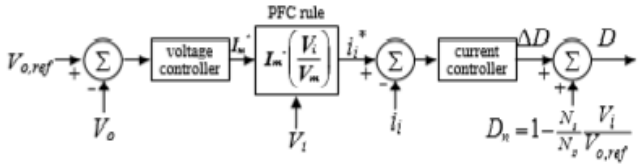

Fig -6: Control block diagram for single power conversion

The input current reference i_{i_ref} is derived using the input voltage V_i as

$$i_{i_{ref}} = I_m^*\left(\frac{V_i}{V_m}\right) \quad (4)$$

where I_m^* is the amplitude of the input current reference.

According to the power difference between the input power and output power, the output voltage is decided. If the input power is excessed than the power required from the load, the output voltage increases. On the other hand, the output voltage decreases if the input power is lower than the power required from the load. In the proposed control system, the voltage controller is easily implemented with an adaptive Fuzzy Logic Controller. To obtain a high power factor, it is necessary to match the phase of the grid current i_g with that of the input voltage v_g. Because the input voltage V_i includes information about the phase of v_g, synchronization with v_g can be achieved using V_i.

The current controller is simply implanted with the Fuzzy Logic Controller because its output value ΔD has a linear first-order relation with Δ_i. The duty ratio D is obtained by adding the nominal duty D_n and the feedback control duty ΔD.

The nominal duty D_n and the feedback control duty ΔD are defined as

$$D_n = 1 - \frac{N_s}{N_p}\frac{V_i}{V_{bat,ref}}, \Delta D = 2L\frac{\Delta i_i}{nT_s V_{bat,ref}} \quad (5)$$

2.4 DESIGN GUIDELINE FOR SOFT-SWITCHING TECHNIQUE

The soft-switching technique allows the proposed converter to obtain high efficiency and high power density. The zero-voltage switching (ZVS) turn-on for S_{1a} and S_{2a} is naturally obtained from the stored energy in L_m and L_{lk}.

However, to achieve the soft-switching of the main switches S_1 and S_2, a specific converter design is required. To achieve the ZVS turn-on of S_1 and S_2, the switch currents i_{s1} and i_{s2} should be in the negative direction before each gate signal is transferred to the corresponding switch.

Because the average secondary current i_{s_avg} is zero, the average magnetizing current i_{m_avg} is the same as the average current i_{p1_avg} of i_{p1}.

Furthermore, because the proposed converter has symmetrical circuit design and operation, the relationship between i_{m_avg} and i_i can be represented as

$$i_{m\_avg} = \frac{i_i}{2} \quad (6)$$

Assuming that there is no power loss, the instantaneous input power is equal to the instantaneous output power p_o as

$$p_{in} = v_i i_i = V_0 i_0 = p_0 \quad (7)$$

where i_o is the output current.

Then, the average current i_{m_avg} in (3) can be re-expressed from (6) and (7) as follows:

$$i_{m\_avg} = \frac{ni_0}{1-D} \quad (8)$$

At t_0, the current i_{s1} flowing through the main switch S_1 is the magnetizing current i_m. From (3), (7), (8), i_{s1} at t_0 can be derived as

$$i_{s1(t_0)} = i_{m_{avg}} - \frac{\Delta i_m}{2}$$

$$= \frac{ni_0}{1-D} - \frac{V_0 D T_s}{4nL_m}, \text{ for } D<0.5$$

$$\frac{ni_0}{1-D} - \frac{V_0(1-D)T_s}{4nL_m}, \text{ for } D\geq 0.5 \quad (9)$$

To satisfy the ZVS condition of S_1 in (9), the switch current i_{s1} should be negative at t_0. Then, L_m can be designed to meet all operating points within the grid period as

$$L_m \leq \frac{V_0^2 D_{min}(1-D_{min})}{n^2 f_s p_{0,peak}} \quad (10)$$

where D_{min} is the minimum duty, f_s is the switching frequency, and $p_{o,peak}$ is the peak instantaneous output power at a certain average power level. Due to the symmetrical operation, the ZVS condition for S_2 is equal to that of S_1 as (10).

To achieve the ZCS turn-off of D_1 and D_2, the half resonant period should meet the following conditions as

$$\frac{\pi}{\omega_r} < DT_s, \text{ for } D<0.5$$

$$\frac{\pi}{\omega_r} < (1-D)T_s, \text{ for } D \geq 0.5 \quad (11)$$

Equation (11) indicates that D_1 and D_2 are turned off with the zero current at all operating points for D<0.5 if the resonant frequency is greater than the switching frequency.

On the other hand, the ZCS region for D>0.5 is determined according to the design of the equivalent resonant capacitor C_r as

$$C_r < \frac{1}{\omega_{rc}^2 L_{lk}} \quad (12)$$

where the critical angular resonant frequency ω_{rc} is defined as $\pi f_s/D_{cri}$, where the critical duty D_{cri} is the maximum duty in the ZCS region.

Table -1: Parameters

Parameters	Symbols	Values
Input Voltage	V_{in}	240Vrms
Grid Frequency	f_g	50Hz
Output Voltage	V_{out}	4500V
Switching frequency	f_s	70kHz
Primary Winding Turns	N_p	24turns
Secondary Winding Turns	N_s	20turns
Magnetizing Inductance	L_m	88µH
Leakage Inductance	L_{lk}	0.5µH
Input Inductor	L	0.8mH
Input Capacitor	C_i	1µF
Clamp Capacitor	C_c	4.4µF
Resonant Capacitors	C_{r1}, C_{r2}	2µF (each)
Output Capacitor	C_o	10µF

Table -2: FUZZY RULES

Input	NB	NS	ZE	PS	PB
NB	NB	NB	NB	NS	ZE
NS	NB	NB	NS	ZE	PS
ZE	NB	NS	ZE	PS	PB
PS	NS	ZE	PB	PB	PB
PB	ZE	PS	PB	PB	PB

3. RESULTS AND DISCUSSIONS

A 5kW prototype is built and tested to evaluate the feasibility of the proposed converter. The supply voltage ranges from 120V to 240V. To satisfy the ZVS condition, the magnetizing inductance value is set to be 0.8mH. By considering the ZCS condition, the resonant capacitors C_{r1} and C_{r3} value is set to be 2µF each.

Fig.7 shows the experimental waveforms of input voltage, input current, voltage and current across switches S_1 and S_{1a}. It is seen that i_i is a nearly perfectly sinusoidal and in phase with v_i. In this case, the power factor is measured to be 0.999.

Fig.8 shows the gate pulse of switches in which S_1 and S_{2a} conduct in one period while the switches S_2 and S_{1a} conduct in another period.

Fig.9 shows the output voltage and output current obtained from the variation of load. The voltage obtained is twice the input voltage. Thus, the converter provides high voltage at the output.

Fig. 10 shows the measured power factor as a function of the input voltage level. The power factor is greater than 0.99 over the entire voltage range from 120V to 240V, which indicates that the proposed converter can achieve a high power factor without requiring an additional PFC circuit.

Fig. 11 shows an efficiency of the proposed converter. It is seen that it has higher efficiency than the other converter topologies over the entire range of load conditions. In the proposed converter, the maximum efficiency is measured to be 98%.

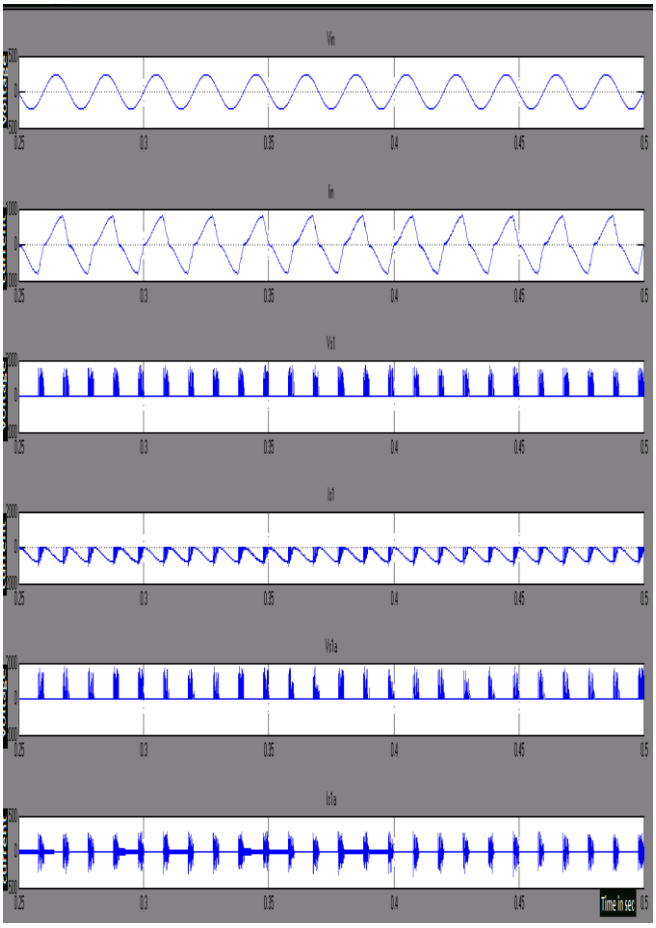

Fig -7: Waveforms of input voltage, input current, voltage and current across the switches S_1 and S_{1a}

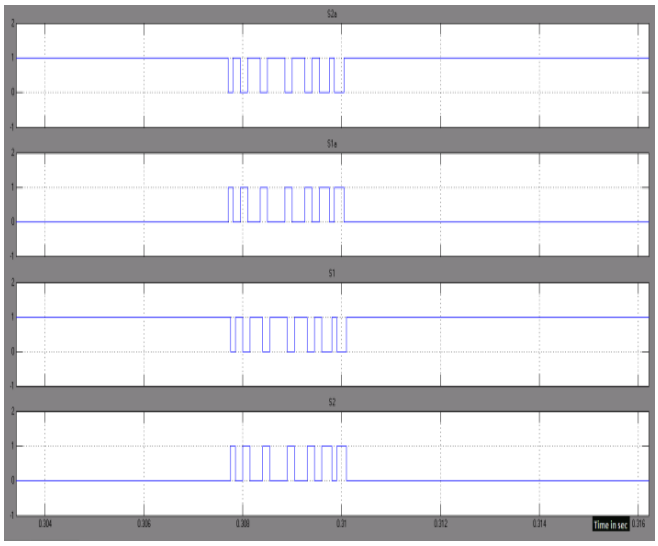

Fig -8: Gate pulse of switches

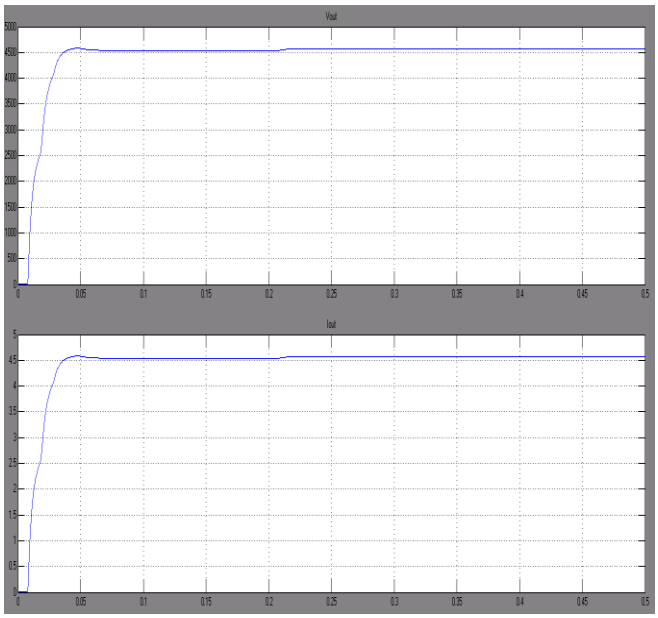

Fig -9: Output voltage and output current

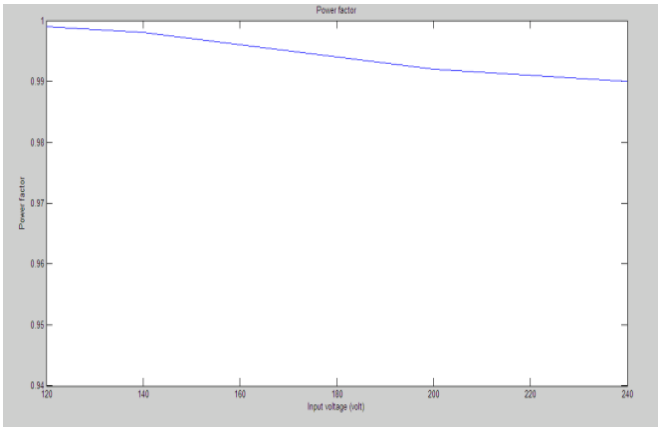

Fig -10: Power factor

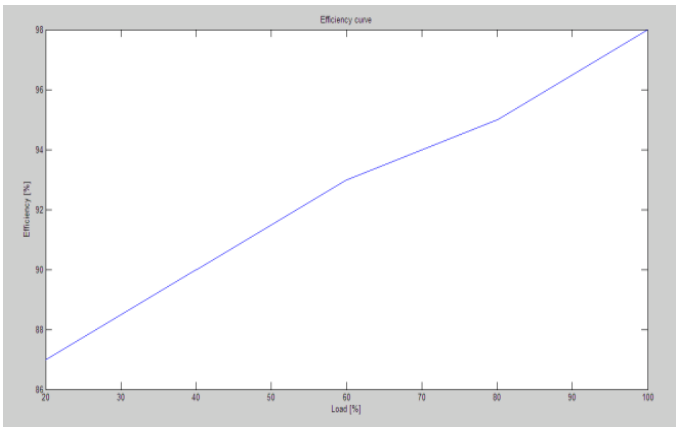

Fig -11: Efficiency

4. CONCLUSION

A high efficiency AC-DC converter is introduced and analyzed. The proposed converter consists of series resonance and soft switching technique. These techniques improve the efficiency and power density in the proposed converter. To obtain the experimental results a 5kW prototype is built and tested. This indicates that it provides high efficiency of 98% by using series resonance of the circuit. The power factor is maintained above 0.99 for the entire voltage range of 120V-240V. This indicates that the proposed converter can provide high power factor without requiring an additional PFC circuit.

REFERENCES

[1] Dylan Dah-Chuan Lu, Member, IEEE, Herbert Ho-ChingIu, Senior Member, IEEE, and Velibor Pjevalica, "Single-Stage AC/DC Boost–Forward Converter with High Power Factor and Regulated Bus and Output Voltages," IEEE Trans. Ind. Electron., vol. 56, no. 6, pp. 2128–2132, Jun. 2009.

[2] Klaus Raggl, Member, IEEE, Thomas Nussbaumer, Member, IEEE, Gregor Doerig, Juergen Biela, Member, IEEE, and Johann W. Kolar, Senior Member, IEEE, "Comprehensive Design and Optimization of a High-Power-Density Single-Phase Boost PFC," IEEE Trans. Ind. Electron., vol. 56, no. 7, pp. 2574-2587, Jul. 2009.

[3] Carlos Alberto Gallo, Fernando Lessa Tofoli, and João Antonio Corrêa Pinto, "Two Stage Isolated Switch-Mode Power Supply with High Efficiency and High Input Power Factor," IEEE Trans. Ind. Electron., vol. 57, no. 11, pp. 3754-3766, Nov. 2010.

[4] Il-Oun Lee, Student Member, IEEE, and Gun-Woo Moon, Member, IEEE, "A New Asymmetrical Half-Bridge Converter with Zero DC-Offset Current in Transformer," IEEE Trans. Power. Electron., vol. 28, no. 5, pp. 2297-2306 May. 2013.

[5] Pritam Das, Member, IEEE, Majid Pahlevaninezhad, Member, IEEE, Gerry Moschopoulos, Senior Member, IEEE, "Analysis and Design of a New AC-DC Single-Stage Full-Bridge PWM Converter with Two Controllers,"IEEE Trans. Ind. Electron., vol. 60, no. 11, pp. 4930-4946, Nov. 2013.

[6] Jun-Ho Kim, Moon-Young Kim, Cheol-O Yeon, and Gun-Woo Moon, "Analysis and Design of Boost-LLC Converter for High Power Density AC-DC Adapter,"Proc. IEEE Energy Conversion Congress and Exposition (ECCE) Asia, 2013, pp. 6-11.

[7] Tiesheng Yan, Jianping Xu, Member, IEEE, Fei Zhang, Jin Sha, and Zheng Dong, "Variable On-Time Controlled Critical Conduction Mode Fly-back PFC Converter,"IEEE Trans. Ind. Electron., vol. 61, no. 11, pp. 6091-6099, Nov. 2014.

[8] Hugo Santos Ribeiro and Beatriz Vieira Borges, Senior Member, IEEE, "Solving Technical Problems on the Full-Bridge Single-Stage PFCs,"IEEE Trans. Ind. Electron., vol. 61, no. 5, pp. 2264-2277, May. 2014.

[9] Sung-Ho Lee, Chun-Yoon Park, Jung-Min Kwon, Member, IEEE, and Bong-Hwan Kwon, Member, IEEE, "Hybrid-type Full-bridge DC/DC Converter with High Efficiency,"IEEE Trans. Power. Electron., vol. 30, no. 8, pp. 4156-4164, Aug. 2015.

[10] Tao Meng, Shuai Yu, Hongqi Ben, and Guo Wei, "A Family of Multilevel Passive Clamp Circuits With Coupled Inductor Suitable for Single-Phase Isolated Full-Bridge Boost PFC Converter," IEEE Trans. Power Electron., vol. 29, no. 8, pp. 4348-4356, Aug. 2014.

[11] Xiaogao Xie, member IEEE, Jiangsong Li, Kunsheng Peng, Chen Zhao, Qiang Lu, "Study On the Single-stage Forward, fly-back PFC Converter with QR Control," IEEE Trans. Power. Electron., vol. 31, no. 1, pp. 430-442, Jan. 2016.

[12] Jun-Young Lee, Member, IEEE, Young-Doo Yoon, Member, IEEE, and Jung-Won Kang, "A Single-Phase Battery Charger Design for LEV Based on DC-SRC with Resonant Valley-Fill Circuit," IEEE Trans. Ind. Electron., vol. 62, no. 4, pp. 2195-2205, Apr. 2015.

[13] Jeongpyo Park, Young-Jin Moon, Min-Gyu Jeong, Jin-Gyu Kang, Sang-Hyun Kim, Jung-Chul Gong and Changsik Yoo, Member, IEEE, "Quasi-Resonant (QR) Controller with Adaptive Switching Frequency Reduction Scheme for Flyback Converter," IEEE Trans. Ind. Electron., vol. 63, no. 6, pp. 3571-3581, Jun. 2016.

[14] Sheng Zong, Haoze Luo, Wuhua Li, Member, IEEE, Xiangning He, Fellow, IEEE, and Changliang Xia, Senior Member, IEEE, "Theoretical Evaluation of Stability Improvement Brought by Resonant Current Loop for Paralleled LLC Converters," IEEE Trans. Ind. Electron., vol. 62, no. 7, pp. 4170-4180, Jul. 2015.

[15] Mustapha DEBBOU and Francois Colet, "Interleaved DC/DC Charger for Wireless Power Transfer," Proc. IEEE Transportation Electrification Conference and Expo (ITEC), 2013, pp. 1-8.

BIOGRAPHIES

N.Keerthana received her BE (Electrical and Electronics Engineering) from Kongu Engineering College, Perundurai, Erode, TamilNadu, India. Now she is pursuing Master of Engineering (Power Electronics and Drives) in Muthayammal Engineering College, Rasipuram, Namakkal, India. Her areas of interest include Special Electrical Machines, Power Electronic Devices and Power Converters. She presented papers on Industrial Drives.

SP. Umayal was born in Chennai India. She received her B.E.(EEE) and M.E.(Power system) degrees from Thiagarajar college of Engineering, Madurai, India, in 1990 and 1999, respectively. She received her Ph.D. degree in Electrical Engineering from Anna University, Chennai, India, in 2008. In 1996 she joined Sethu Institute of Technology, Virudhunagar, India, as a Lecturer in the Department of Electrical and Electronics Engineering, where she was an Assistant Professor from 2001 to 2007, and Professor & Head of the Department from 2008 to 2013. She is presently working as Professor &Dean at Muthayammal Engineering College, Namakkal, India. Her current research interests include intelligent control techniques, power quality monitoring, power electronic converters and AC drives. She has published more than 20 technical papers in national and international journals.