International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395-0056
Volume: 05 Issue: 05 | May-2018 www.irjet.net p-ISSN: 2395-0072

An 8-bit 1 KS/s Successive Approximation Register Analog-To-Digital Converter for Low-Power Application

Abdul Khalid[1], Mahaveera K[2]

[1]*Student, Dept. of E&C Engineering, N.M.A.M Institute of Technology, Karnataka, India,*
[2]*Assistant Professor, Dept. of E&C Engineering, N.M.A.M Institute of Technology, Karnataka, India.*

Abstract - *This paper presents an 8-bit Successive Approximation Register Analog to Digital Converter (SAR-ADC) for portable medical devices namely artificial pacemaker. At 1K samples/s, the proposed SAR-ADC consumes 1.8µW from a 1V power supply. The circuit is simulated using Cadence virtuoso tool under 90 nm CMOS technology. According to the simulation results, the SAR-ADC has a signal-to-noise ratio of 40.1 dB, peak spurious-free dynamic range of 44.35 dB, and a signal-to-noise-and distortion ratio of 43.6 dB for a 250Hz–500mVpp input sine wave. These results show that the proposed SAR-ADC in 90 nm technology is a good candidate for low-power medical application.*

Key Words: Analog-to-Digital Converter, Successive Approximation Register, Bio-signals and systems

1. INTRODUCTION

There are different architectures of ADC are available. These architectures have different kinds of features such as pipelined ADC whose bandwidth is usually above tens of megahertz, flash ADC which can operate in high sampling rate, sigma delta modulator has the ability to achieve high precision, and SAR ADC which owns qualities of low-power dissipation and lower chip area hence low cost; thus it is best suitable for devices, especially in wireless transmission sensor networks and medical application which requires low power dissipation, speed required is not high and resolution requirement is medium. Therefore, the SAR ADC architecture is considered in this study. In [1], the traditional SAR ADC is not suitable for lower supply voltage applications since low voltage causes high on-resistance of the on-off switch circuit and limits the ADC's input bandwidth. Clock boosting can solve this problem; however, the power consumption is high [2]. Reducing the power consumption of the SAR ADC becomes an important issue if the ADC is utilized in sensor networks or biomedical portable devices. Research approaches on reducing the power consumption of digital circuits has recently become the target in [3] and [4]. LITERATURE, [5] uses an energy-saving method to save power consumption. Nevertheless, previous mentioned methods may enhance the SAR control logic complexity, and thus increases power dissipation. Hence, a 1V 8-bit 1 K Samples/s SAR ADC is presented.

The rest of the paper is organized as follows. Section 2 explains the architecture and the design of the SAR ADC. Section 3 discusses each circuit's operation principle. Measured results are presented in Section 4. Finally, Section 5 draws our conclusion.

2. ARCHITECTURE OF THE ADC

The proposed SAR ADC design targets on a moderate resolution and low power consumption, therefore all the circuit components except the comparator possess single-ended structures in order to reduce power dissipation. Although a fully-differential circuit structure achieves better common mode noise rejection and less distortion. As illustrated in Figure 1, the proposed ADC consists of a Sample-and-Hold (S/H) circuit, a charge redistribution Digital-to-Analog Converter (DAC), a comparator and a SAR control logic circuit. It is found that adjusting the reference voltage also influences the performance of the ADC while conducting measurement. When designing the binary weighted capacitor array of the DAC, delay constant is taken into consideration so that switches coping with different values of capacitors are designed with certain proportion. The value of unit capacitor is set to be larger enough to overcome the noise of kT/C where k is Boltzmann constant, T is temperature in oK, and C is the total capacitance of the capacitor array in Farad. Since the total capacitors' value is large enough to suppress kT/C noise, how to overcome the mismatch issue of the capacitor array becomes significant.

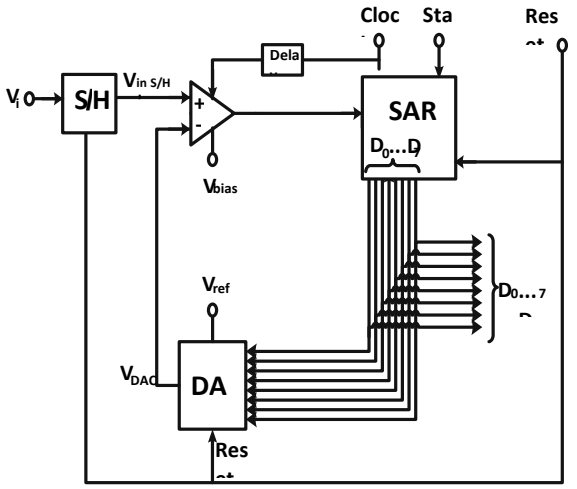

Fig. -1: Schematic of the proposed 8-bit SAR ADC

The proposed ADC has lower circuit complexity so it can achieve low power consumption for medical application.

3. CIRCUIT DESIGN

3.1 Sample and Hold (S/H) circuit

The proposed successive approximation ADC uses a simple Sample and Hold (S/H) circuit at the input stage to sample the input sine wave. The simple S/H circuit consists of a transistor switch (M1) and a sampling capacitor (Cs). But this circuit suffers from charge injection and clock feed through effect. To overcome the charge injection and clock feed through effect a dummy switch is used at the output as shown in Fig. 2. The drain and source of the dummy switch is shorted and connected to the output. The dummy switch is controlled by the negative clock. The width of the dummy switch should be half the width of the transistor M1 so that the induced charge is absorbed by the dummy switch.

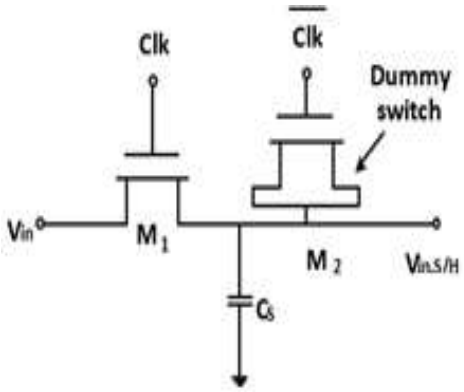

Fig. -2: Schematic of Sample and Hold circuit

The charge injection and clock-feed-through are issues that mainly occur when using transistors as switches in switched-capacitor circuits. When the clock at the NMOS gate goes high (VDD), the transistor turns ON, and the input voltage (Vin) is sampled by the capacitor CS. The channel charge under the gate oxide is given as follows:

$$Qch = WLCox(VDD - Vin - Vtn) \quad (1)$$

Then, when the clock goes low, the transistor turns OFF, and its channel charge flows out from its gate into the source and the drain creating an error in the sampled voltage [7]. The charge injection produces different errors that affect the accuracy of the sampler. In the clock-feed-through issue, the MOS switch couples the clock transitions to the sampling capacitor through its gate drain or gate source overlap capacitances. When the clock signal goes high, an overlap capacitance is fed through the gate source, the gate drain, or both. On the other hand, when the clock goes low, the transistor turns OFF, and a capacitive divider is created. Fig.3 shows the output of the S/H circuit.

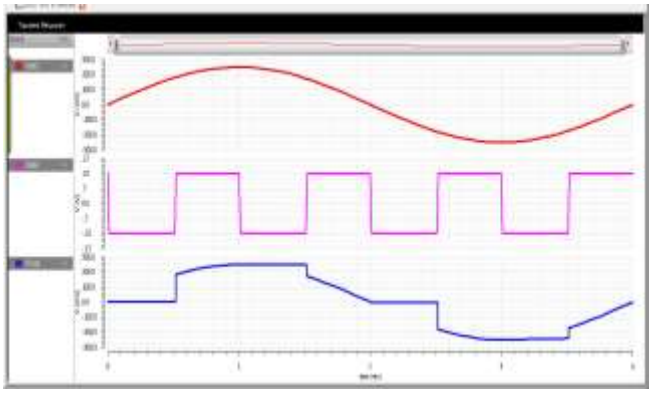

Fig. -3: Output of Sample and Hold circuit

3.2 Comparator circuit

Fig 3 shows the circuit schematic of the double tail dynamic latch comparator. This comparator is a fully differential-in and differential-out circuit without any static power dissipation. Its power consumption varies with the clock signal. It can also operate with a lower supply voltage and has a more stable offset of the comparator. It consists of two_tails, one for the input_stage and other for the latching_stage as shown in Fig 4. This configuration has less loading and therefore can operate at lower supply voltages. The double tail enables large current for fast latching independent of the common mode voltage at the latching stage and a small current for low offset and noise at the input stage.

Fig. 5 shows the output of the comparator. During the reset phase transistors M9 and M10 pre-charge the gate of M11 and M12 to VDD. Accordingly, Vout+ and Vout− will be high. After the reset phase, the tail transistors M3 and M13 turned ON. At the drains of the differential pair nodes, the common mode voltage drops monotonically and an input dependent differential voltage ΔVDi will build up.

The intermediate stage formed by M11 and M12 passes ΔVDi to the cross coupled inverters and also provides additional shielding between the inputs and output which results in less kickback noise. As soon as the common mode voltage at the drains of the differential pair nodes is not enough for M11 and M12 to clamp its drain to ground, the inverters starts to regenerate the voltage difference. The ideal operating point VCM and the timing of various phases can be tuned with the transistor sizes. As a result, the advantages of the double tail topology, it has better optimization of the balance between speed and offset independently, power and common mode voltage. In addition to that, it has a better isolation between the input and output of the comparator which results in less kickback noise and is well suited to operate under low supply voltages with low power consumption.

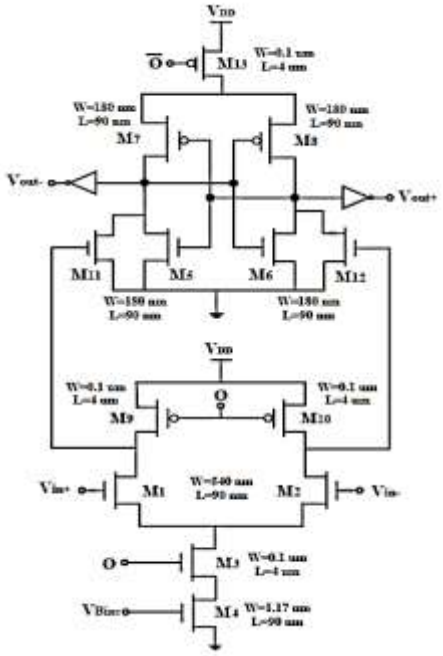

Fig. -4: Schematic of Double Tail Dynamic Latch Comparator

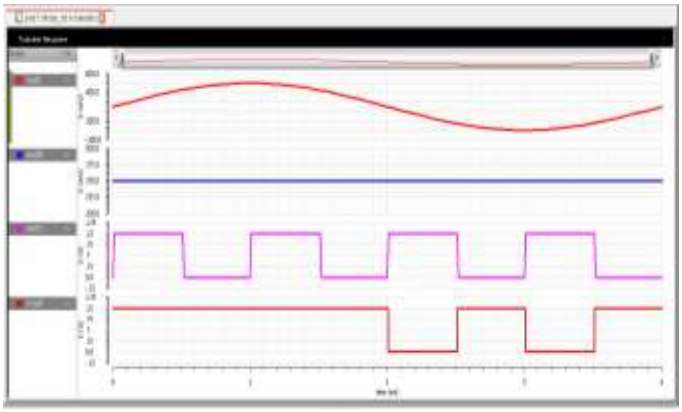

Fig. -5: Output of Double Tail Dynamic Latch Comparator

3.3 SAR control logic

The Successive Approximation Register (SAR) is the digital controller circuit which is responsible for executing the binary search algorithm technique. The SAR logic is the last block of the ADC components in which the output of the SAR-ADC circuit will be determined according to the comparator output. Therefore, it has a significant effect on the whole ADC performance which in turns will affect the overall system. The Successive Approximation register contains N bit for an N-bit ADC. Fig 6 and Fig. 7 shows the schematic of the SAR control logic and output of SAR logic.

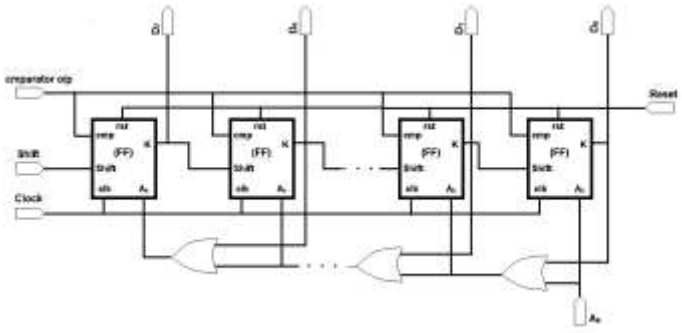

Fig. -6: Schematic of SAR control logic

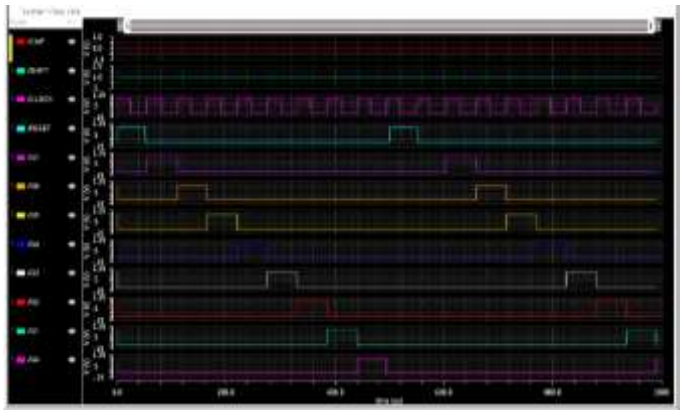

Fig.-7: Output of 8-bit SAR control logic with comparator output as '0'

3.4 Digital to Analog Converter (DAC)

In order to achieve low power dissipation and relatively small area of the SA-ADC, a DAC that is based on a binary weighted switched-capacitor array is implemented. Fig 8 shows the schematic of the capacitor-based DAC. The switches are realized by using NMOS and PMOS transistors with each capacitor in the array. The DAC circuit accepts an 8-input bits that are coming from the SAR control logic.

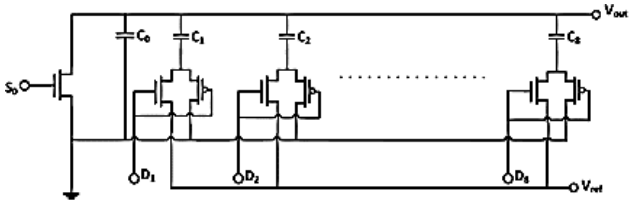

Fig. -8: Schematic of binary weighted switched capacitor array DAC

3.5 SAR-ADC

The overall SAR_ADC including the S/H circuit, the comparator circuit, the capacitor based DAC circuit, and the SAR controller circuit is shown in Fig.9. The SAR-ADC has been designed, extracted, and simulated in 90 nm CMOS technology using Cadence Virtuoso tool. The key performance parameters are tabulated and compared with

other literature in Table 1. The presented SAR ADC shows better results.

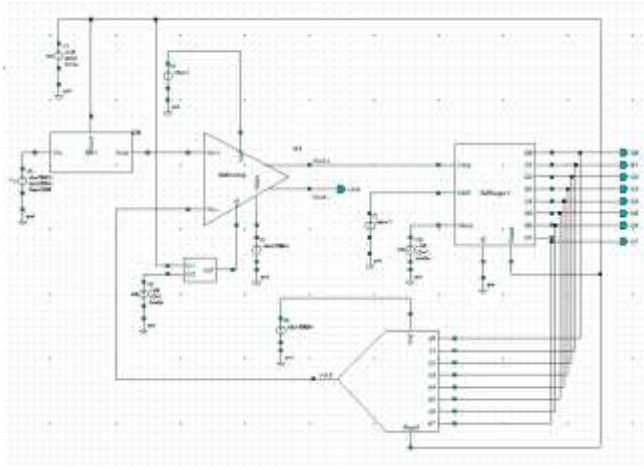

Fig. -9: Schematic of the SAR ADC

Table -1: Performance Comparison of 8-bit 10KS/s ADC with Previously Reported Papers

Parameters	[1]	[7]	[5]	This work
Technology (nm)	130	130	180	90
Resolution (bits)	8	10	12	8
Sampling Rate (KS/s)	10	1000	50	10
ENOB	6.39	9.6	11.4	6.023
DNL/INL	-	1.2/4.5	.56/.38	0.6/0.51
Power (µW)	147.6	3000	1	1.8
FoM (J/conv.)	786.1f	6.81 p	40.2 f	69.3 f

4. CONCLUSION

In this paper, a 8-bit 1-KS/s SAR ADC with a control logic circuit implemented in 90 nm CMOS process is presented. Since the comparator and digital circuits operate only during the hold mode of the S/H circuit, it reduces half the power dissipation of comparator and digital circuits.

REFERENCES

[1] E. Culurciello and A. Andreou, "An 8-bit, 1 mW Successive Approximation ADC in SOI CMOS," IEEE Trans. Circuits Syst. II, Expr.Briefs, vol. 53, no. 9, pp. 858–861, Sep. 2006.

[2] T. Cho and P. R. Gray, "A 10-bit, 20 Msamples/s, 35 mW pipeline A/D converter," IEEE J. Solid-State Circuits, vol. 30, no. 3, pp. 166–172, Mar. 1995.

[3] B. P. Ginsburg and A. P. Chandrakasan, "A 500-MS/s 5-bit ADC in 65nm CMOS," IEEE Symp. VLSI Circuits, pp. 174–175, Jun. 2007.

[4] Y. K. Chang, C. S. Wang, and C. K. Wang, "A 8-bit 500-kS/s Lowpower SAR ADC for Bio-medical Application," IEEE ASSCC Dig. Tech. Papers, pp. 228–231, Nov. 2007.

[5] J. Sauerbrey, D. Schmitt-Landsiedel and R. Thewes, "A 0.5-V 1-µW successive approximation ADC," IEEE J. Solid-State Circuits, vol.38, no.7, pp. 1261-1265, Jul. 2003.

[6] S. Jiang, M. A. Do, K. S. Yeo, and W. M. Lim, "An 8-bit 200MSample/s pipelined ADC with mixed-mode front-end S/H circuit," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 55, no. 6, pp. 1430–1440, Jul. 2008.

[7] Z. Zeng, C.-S. Dong, and X. Tan, "A 10-bit 1MS/s Low Power SAR ADC for RSSI application," IEEE Intl. Conf. on Solid-State and Integrated Circuit Technology (ICSICT), pp.569-571, Nov. 2010.

[8] H.-W. Chen, Y.-H. Liu, Y.-H. Lin, and H.-S. Chen, "A 3 mW 12-bit 10MS/s Sub-range SAR ADC," IEEE Asian Solid-State Circuits Conf., pp.153-156, Nov. 2009.

[9] B. P. Hershberg, S. T. Weaver, U-K. Moon, "A 1.4V Signal Swing Hybrid CLS-Opamp/ZCBC Pipelined ADC Using a 300mV Output Swing Opamp," IEEE ISSCC Dig. Tech. Papers, pp. 302–303, Feb. 2010.