# ASIC IMPLEMENTATION OF EFFICIENT ERROR DETECTION FOR FLOATING POINT ADDITION

K.Kowsalya[1], A.Janaki[2], D.Haripriya[3], V.Nandhini[4] , J.Jayasudha[5]

[1,2,3,4]*UG Scholar, Dept. of ECE, Tejaa Shakthi Institute of Technology for Women, Coimbatore, India.*
[5]*Assistant Professor, Dept. of ECE, Tejaa Shakthi Institute of Technology for Women, Coimbatore, India.*

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**Abstract -** *Floating point operations are used in large dynamic range applications. In a floating point unit addition is one of the most complex operation. An area efficient floating point addition unit with error detection logic is proposed in this paper. Existing error detection logics and leading zero anticipators helps to decrease the delay of the general floating point unit, but they are not area efficient. An area efficient carry select adder with error detection logic is designed by replacing RCA. Here binary to excess-1 converter is used in carry select adder(CSLA) instead of ripple carry adder for carry in = 1. The proposed design is tested on XILINX simulator.*

***Key Words*: CSLA, BEC, IEEE754, ASIC, XILINX.**

## 1. INTRODUCTION

The growth of electronic components are rapidly increasing because of their portability. In VLSI industry the low power arithmetic circuits are essential for fast computation and to be efficient. Delay is high when performing arithmetic operation for large bit size. Hence we are using fast adders such as carry lookahead adder and carry select adder to minimize the delay. Carry propagation delay can be avoided by using CSLA as they produce carry independently. The Numerical computation involving floating point operands are fundamental in many scientific applications. Due to their high dynamic range and good precision, floating point operations are used in various fields. The standard floating point format(IEEE754) have three values sign, exponent and mantissa. Single precision binary format representation for IEEE754 is shown in fig.1. The most significant bit is sign bit, next 8 bits are exponent and last 23 bits are mantissa. Its value is calculated by using the formula:

$$r = (-1)^{sign} \times 1.\text{mantissa} \times 2^{exponent}$$

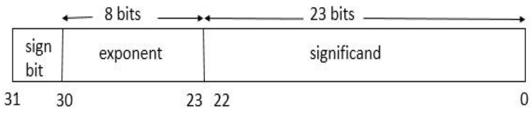

Fig 1. IEEE single precision binary format representation

The result of the operation should be in the normalized form. And for this reason the result must be shifted left in order to make MSB 1. A leading zero anticipator(LZA) is used to calculate the shift amount that is needed for the normalization operation. LZA increases the performance of floating point processor. It reduces the delay produced by normalization process as it works parallel with the adder. An error detection logic is used to avoid the error.

## 2. REGULAR CARRY SELECT ADDER

Generally carry select adder consist of two ripple carry adders and a multiplexer. Fig 2. Shows the general carry select adder structure. Since the CSLA have dual ripple carry adder(RCA), it consumes more area and it is proved by calculating the gate count of carry select adder. The gate count is obtained by basic blocks of carry select adder. Table 1. shows the gate count of the basic blocks of carry select adder(CSLA).

Table 1. Delay and gate count of the basic blocks of carry select adder

| Adder blocks | Delay | Area count |
|---|---|---|
| XOR | 3 | 5 |
| 2:1 mux | 3 | 3 |
| Half adder | 3 | 6 |
| Full adder | 6 | 13 |

In general carry select adder the group 2 have two sets of 4 bit ripple carry adder. Hence group 2 has a gate count of 117 and it is calculated as follows:

Gate count=177( Number of Full adders + Number of Half adders + Number of Multiplexers )

Number of Full adders = 91 (7 * 13)

Number of Half adders = 6(1 * 6)

Number of multiplexers = 20(5 * 4)

As Group 2, 3 and 4 have uniform structure the gate count is same for them. The group 1 consist of four full adders hence it has gate count of 52. The general carry select adder area count for all the groups are evaluated and listed in table 2.

Table 2. Area count of CSLA groups

| Group | Area count |
|---|---|
| Group1 | 52 |
| Group2 | 117 |
| Group3 | 117 |
| Group4 | 117 |

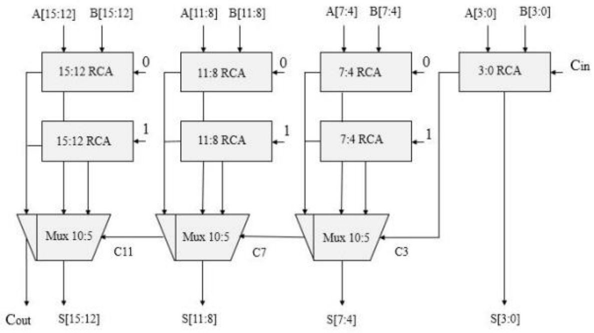

Fig 2. 16 bit general carry select adder

## 3. CARRY SELECT ADDER WITH BEC

In order to reduce the area of the general carry select adder and make it work efficiently, single ripple carry adder should be used instead of dual ripple carry adder. Since the binary to excess-1 converter(BEC) have less gate count it is used in carry select adder(CSLA) instead of ripple carry adder for cin = 1. The structure of BEC and CSLA with BEC is shown in Fig 3(a) and 3(b).

The modified carry select adder has 4 groups. Each groups contains one ripple carry adder(RCA), one binary to excess-1 converter(BEC) and a multiplexer. In the modified CSLA, the group 2 consist of one 4 bit RCA which has 3 full adder and 1 half adder for carry in = 0. A 5 bit BEC is used instead of another 4 bit RCA for carry in = 1. The group 2 area count is calculated as follows:

Gate count = 89 ( Full adder + Half adder + Multiplexer + BEC )

Full adder = 39 (3 * 13)

Half adder = 6 (1 * 6)

Multiplexer = 20 (5 * 4)

NOT = 1

AND = 3 (3 * 1)

XOR = 20 (4 * 5)

Group 2, 3 and 4 have the same gate count. The group 1 has gate count of 52 as it consist of 4 full adders. The gate count of the modified structure is given in table 3. By comparing the gate count of the general and modified carry select adder it is proved that the modified structure is area efficient.

Table 3. Area count of modified CSLA

| Group | Area count |
|---|---|
| Group1 | 52 |
| Group2 | 89 |
| Group3 | 89 |
| Group4 | 89 |

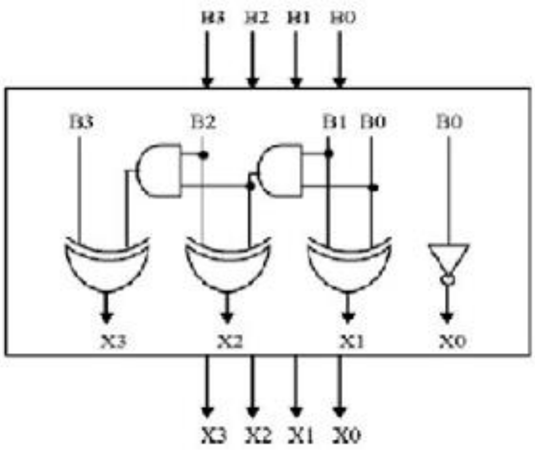

Fig 3(a). 4-bit BEC

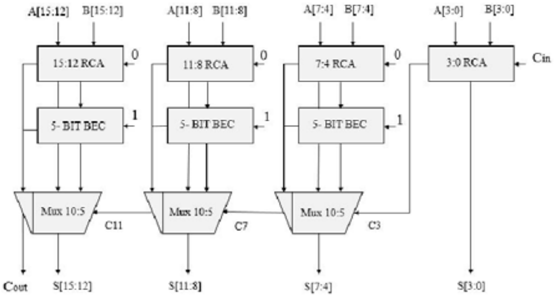

Fig 3(b). carry select adder with BEC

Table 4. 4-bit BEC function table

| B[3:0] | X[3:0] |
|---|---|
| 0000 | 0001 |
| 0001 | 0010 |
| . | . |
| . | . |
| 1110 | 1111 |
| 1111 | 0000 |

## 4. FLOATING POINT UNIT WITH ERROR DETECTION LOGIC

The leading zero anticipator with proposed architecture utilizes the modified CSLA. There are various error detection logics available, among them the one which uses the carry select circuit to detect the error in leading zero anticipator and check for the carry at leading digit position is selected for the modification. The coarse shifter is used to shift the adder output in accordance with shift amount given by LZA. And fine shifter is used to compensate the one bit error produced by leading zero anticipator.

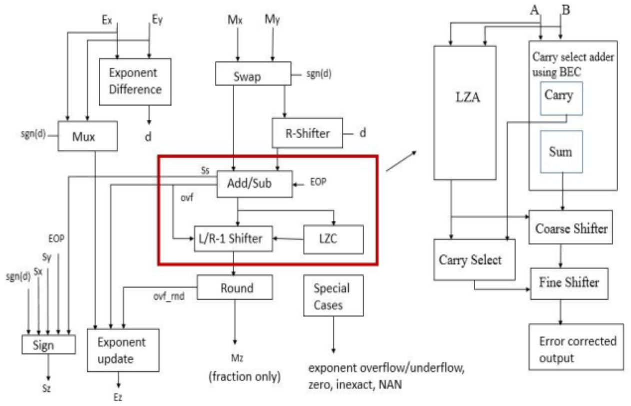

Fig 4. Error detection logic using modified CSLA

## 5. SIMULATION RESULTS

The efficient floating point addition unit is implemented using VHDL(Very high speed integrated circuit hardware description language) in XILINX ISE 10.1 simulator. Table 5 shows the comparison of area, power and delay of general and modified architectures and the simulation output of modified carry select adder(CSLA) is shown in fig 6.

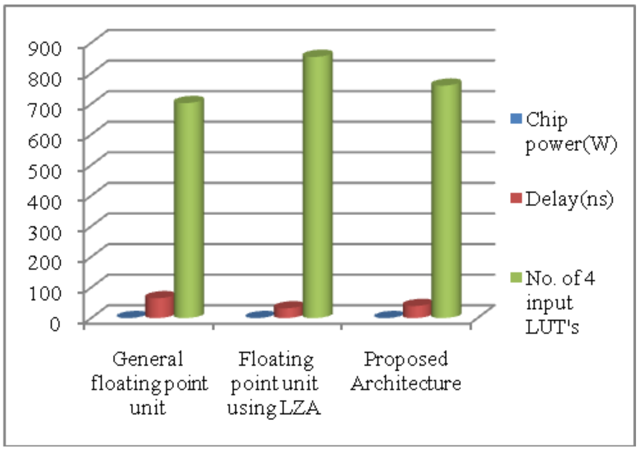

Fig 5. Comparison of different architectures

Table 5. comparison of area, power and delay of general and modified architectures

| Topology | General floating point unit | Floating point unit with LZA | Proposed architecture |
|---|---|---|---|
| No . of 4 input LUT's | 703 | 854 | 760 |
| Occupied slices | 367 | 471 | 415 |
| Delay | 64.93 | 31.989 | 39.522 |
| Total on chip power | .063 | .07 | .069 |

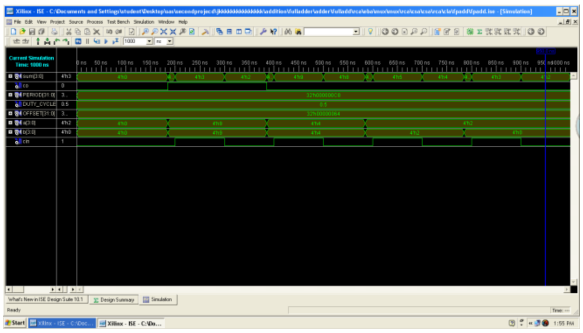

Fig 6. Simulation result of modified CSLA

## 6. CONCLUTION

In this paper an efficient approach is proposed to reduce the area and power of the carry select adder with BEC for floating point unit with error detection logic. The architecture using LZA is efficient in terms of delay, but they are not area efficient. Comparing the proposed architecture with general architecture it has reduced area and power with slight increase in delay. Hence it is proven that the proposed architecture is efficient in terms of area and power, therefore it leads to a better alternative for implementing adders for fast arithmetic functions in data processors. The result is tested and simulated on XILINX simulator. In order to reduce the area, power and delay further, the binary to excess-1 converter can be replaced by D latch. We can observe the further optimization of area, power and delay by using D latch instead of BEC.

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## BIOGRAPHIES

K. Kowsalya, Currently pursuing Bachelor's degree in Electronics and Communication Engineering at Tejaa shakthi institute of technology for women, Coimbatore.

A. Janaki, Currently pursuing Bachelor's degree in Electronics and Communication Engineering at Tejaa shakthi institute of technology for women, Coimbatore.

D. Haripriya, Currently pursuing Bachelor's degree in Electronics and Communication Engineering at Tejaa shakthi institute of technology for women, Coimbatore.

V. Nandhini, Currently pursuing Bachelor's degree in Electronics and Communication Engineering at Tejaa shakthi institute of technology for women, Coimbatore.