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Review on the dual use of Power line - A CMOS Receiver Design

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Abstract - *Today there are many designs are available for a CMOS receiver. Not only their effectively work and circuit complexity increases. They also proportionally increase the number of internal nodes, and individual internal nodes are less accessible due to the limited number of I/O pins present in the PDN. To overcome all the problems, author suggested power line communications (PLCs) at the chip of the circuit, specifically the dual use of power lines of the chip and power distribution networks for the application and the observation of test data and the delivery of power. In this paper we explain and proposed the PLC receiver the transmission of data through power lines. The main objective of the suggested PLC receiver is the robust operation under variations and droops of the supply voltage rather than high data speed. The suggested PLC receiver is going to design with the 0.18 um CMOS design technology under the supply voltage 1.8 V.*

Key Words*: *Design-for-testability (DFT), PLC at ICs, NMOS Design, PLC receiver, power line communications (PLCs).

1. INTRODUCTION

As the new generation of deep sub micrometer VLSI technologies, testing, debugging, and diagnosis of VLSI circuits become more difficult and expensive. In virtue of higher circuit complexity for this technology, larger process variations, larger interconnection delays relative to transistor switching time, larger leakage current makes the testing more challenging. It is a general consent among test engineers that accessibility, i.e., controllability and observability, to internal nodes for both 2-D and 3-D ICs is essential to address the testing problems. As the circuit complexity increases simultaneously the number of internal nodes increases, and individual internal nodes are less accessible due to the limited number of available I/O pins.

According to our knowledge best approach to provide ubiquitous accessibility to internal nodes is the dual use of power pins and power distribution networks (PDNs) for data communications as well as power supply. The PLC at the IC level would be useful for low data rate communications such as scan design, system debugging, and fault diagnosis. The approach also eliminates the need to route a data path from the node to an external data pin.

2. LITERATURE REVIEW

In this paper[1] the proposed power line communications (PLCs) at the IC level, basically the dual use of power pins and PDN for application and observation of test and also delivery of power. A PLC receiver presented in this paper intends to demonstrate the proof of concept, mainly the transmission of data through power lines. The special concern of this receiver is to achieve the robust operation under the applied voltage and the variations in the supply. The PLC receiver is designed and fabricated in CMOS 0.18-μm technology under a supply voltage of 1.8 V. The results of the receiver can tolerate a voltage drop of up to 0.423 V for a data rate of 10 Mb/s. The power dissipation of the receiver is 3.26 mW and the core area of the receiver is 74.9 μm × 72.2 μm.

This paper [2] proposes a various signaling method for efficient scanning based on the dual use of power lines. The preferred signaling scheme to increase the channel capacity for the multiple parallel scan design, and suggested adoption of the UWB (Ultra Wideband) and direct sequence - code division multiple access (DSCDMA) communication technologies. Because of the wide bandwidth, a UWB signal can reduce its average power level practically to the noise level. The DS-CDMA further mitigates the noise and allows multiple scan inputs to share the connectivity power lines. We studied the feasibility of the proposed scheme through SPICE tool and show the simulation results.

In this analysis [4] speed or even faster speed testing of VLSI circuits aims for high-quality checking of the circuits through testing the performance of related faults. On one side, a compact test set with highly effective to checking the each and every delay faults and also desirable for lower test costs. On the other side, this process increases switching activity during launch and capture operations. This process enhance the quality and cost may thus end up violating peak-power constraints which shows the yield loss, while working on this process generation of pattern under less switching constraints may lead to loss in test quality as well as pattern count inflation. In this paper, they given the design for testability (DfT) support for enabling the use of a set of patterns optimized for cost and quality as is, yet in a low power manner; they developed three different DfT mechanisms,(1) launch-off shift,(2) launch-off capture, and (3) mixed at-speed testing. The given DfT support enables a design partitioning approach, where any given set of patterns, generated in a power-unaware manner, it can be used to test the design regions one by one, it reduces both launch and capture power in a design-flow compatible manner. This is the way to the test pattern count and quality, while lowering the launch/capture power.

Analysis [5] designers use third-party intellectual property

(IP) cores and outsource various steps in their integrated circuit design flow, also fabrication. As a result, security exposure have been emerging, forcing IC designers and end-users to re-evaluate their trust in hardware. Whether an attacker got control over an unprotected design, attacks such as reverse engineering, insertion of infected circuits, and IP address piracy are possible. In this paper, they tourched on the vulnerabilities in very large scale integration (VLSI) design and fabrication process, and analysis design-for-trust (DfTr) techniques that points at regaining trust in IC design. We worked on four DfTr techniques: logic encryption, split manufacturing, IC camouflaging, and Trojan activation. These techniques have been developed by reusing VLSI test principles.

This paper [7] presents a technique for characterizing the statistical properties and supply noise spectrum using only two on-chip low-throughput samplers. As a sample we uses a voltage-controlled oscillator to perform high-resolution analog-to-digital conversion with lesser hardware components. The proposed circuit is implemented in a 0.13um technique with a high-speed link transceiver. Final results from this chip confirm the accuracy of the proposed system and elucidate several aspects of power supply noise, including its cyclostationary nature.

In PLC [9] power pins and the power distribution networks of ICs are used for data communication and power delivery. To extract the data signals from this power lines, so many receivers are in need at each and every nodes of the ICs. For this problem, PLC receivers are already designed. But all of them consume very high power. This paper suggested a Launch On Capture (LOC) And Launch On Shift (LOS) CMOS power line communication receiver is designed in Tanner tool and 0.18um CMOS technology is used. To achieve this much extreme low power, so many CMOS low power techniques are successfully employed like the stacking method, resistor less approach but this method shows the best result.

This paper [10] proposes the use of PDN of a microprocessor of internal nodes for test and debug shows the genuineness of impulse for ultra wide band communication. In this paper author presents design of data recovery block to recover data from ultra wide band impulse superimposed of power lines of microprocessors. Considerations for data recovery block design based on measured PDN structure have been discussed. This circuit was implemented in TSMC 0.18 um technology and simulation shows that the consumption of the power is 4.42 mW under 1.8 V supply voltage and the pulse repetition rate is 200 MHz.

3. PROBLEM STATEMENT

Performance factors like power dissipation, voltage fluctuation and droops, noise immunity and layout space were evaluated with the prevailing style of using CMOS 0.18um technology under 1.8V supply voltage. In all the receiver design basic building blocks is three, which are level shifter, signal extractor and logic restorer. The main concern in all receiver is to achieve robust operation under variation of supply voltage and droops. Through all this analysis we get that the basic work of level shifter is to maintain a particular dc level, signal extractor amplifies the signal and convert it to a differential amplifier, logic restorer recovers logic value from the differential signal. The most area in that they work are area efficient, power dissipation and noise immunity. In our work we employed the nmos in place of the pmos in the differential amplifier in order to reduce the area of the circuit. Thus planned style can have:

- How circuit elements get integrated?
- How to style and implement the nmos and pmos in the circuit in order to reduce the area?
- We uses the microwind tool in order to perform the function?
- From the microwind we shows the waveform and the simulation result of the circuit?
- Calculate all the parameters with the help of given data in the microwind?

4. CONCLUSION

A receiver for Power line communication, which can be applicable to high data rate communications, such as UWB applications, scan design, system debugging, and fault diagnosis. The expected PLC system adopts a binary Amplitude shift key modulation scheme, and the receiver consists of three basic building blocks. In that the level shifter shifts the dc level of the data signal. The signal extractor, based of a mixer and differential amplifier, removes the dc voltage from the data signal, The logic restorer, based on a differential Schmitt trigger, extracts logic values from the data signal while improving the noise immunity and and circuit has low power and less area circuit and also mitigates supply voltage fluctuations and sinks. All these things we expect in our process and make CMOS based PLC system more effective and reliable.

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