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A REVIEW: TO DESIGN EFFICIENT 32 BITS CARRY SELECT ADDER BY USING BRENT KUNG ADDER

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Abstract – *In the type of structure of any adder greatly affects the speed of the circuit. The logarithm structure is considered to be one of the fastest structures and the Brent Kung structure, use this logarithmic concept. Brent Kung is a low power adder and it is most effective technique which is used for implementing to reduced low power and low delay. In this paper, for high performance and low power 32 bits carry select adder is implemented by using Brent Kung adder. Power and delay of all these adder architectures are calculated at different input voltages. Instead of using dual ripple carry adders, Brent Kung is used to design carry select adder. The results analysis shows that Modified 32-bits CSA is better than all the other adder architectures. The designs have been* implemented *by using Tanner EDA tool.*

Key Words: *Brent Kung adder, carry select adder, delay and power.*

1. INTRODUCTION

The human world is exciting, emerging and probable being driven and transformed by technology, and by digital ICTs, in particular. World is fastly transforming into digital world and ready to except new technology which are been introduce. We are surrounded by digital gadgets and technology. Day by day technology becomes more advance and powerful, in just seconds we can send data from one place to other; while in early days it took more than two days to deliver a single massage. If we talk about old version computer system they are in large size and need high power and delay. Technology creates new computer system which not only movable but also in small size, required less power and gives high speed. Computer play a huge role in industry, and now almost 85% company becomes digital. Computer industry introduces advance technology for us that are been used in everyday life; it's actually become our lifestyle. The advances Integrated Circuits (ICs) technology, increase capacity of system, speed functionality, decrease cost and these features help integrated computer system to expand its portfolio of solution and service to enable customers to achieve their business goals . Day by day chips are getting better, modified and fabricated, due to which design techniques are available and used to create advance technology. The advance system components work on different temperature, voltage, silicon die, and so on, these improvements are major challenges. An adder is a digital circuit that performs addition of number. In many computers and other kinds of processors adders are used in the arithmetic logic units or ALU. They are also utilized in other parts of the processor, and used to calculate addresses, table indices, and also used in increment and decrement, and similar operations. Although adders can be constructed for much number representation, such as binary coded decimal, binary number is mostly operated by common adder. High performance and accuracy is dependents on adder. There are some adders which are easy to implement and easy to understand but they required time for execution, so adder architecture introduce carry select adder for fast execution. In electronics, a carry select adder is a particular way to implement an adder, which is a logic element that computes the bit sum of two bit numbers. The carry select adder is simple but rather fast, having a gate level depth of. The logarithm structure is considered to be one of the fastest structures and there is such adder which uses this concept. In adder architecture Brent Kung use this concept, which is low power, gives fast execution.

2. LITERATURE REVIEW

2.1 Research on Carry Select Adder by using Brent Kung:

Brent-Kung Adder:
Brent-Kung adder is a parallel prefix adder which gives fast result and save power, it is considered to be one of the most flexible adders. The execution speed of Brent Kung is higher as compare to other. In this paper, Modified Square Root Carry select Adder proposed architecture by using Brent Kung adder instead of dual RCAs in give high speed and low power. Brent Kung is a combination of processing and network.

As show in the fig: 4 bit Brent Kung adder, it consist three steps:

1. Pre- processing stage
2. Carry generation network
3. Post processing stage

1. Pre- processing stage

Block diagram represent the n-bit parallel prefix adder. Singles are generated and propagate in each pair of inputs A and B. These signals are given by the following equations:
Pi=Ai xor Bi (1)
Gi=Ai and Bi (2)

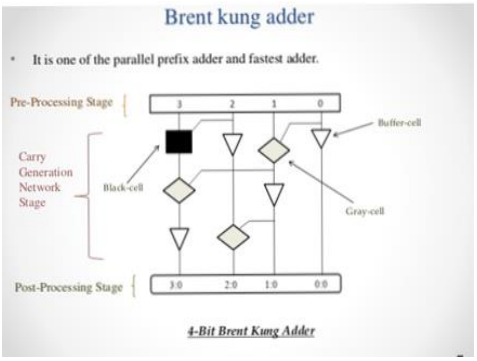

Fig: 4-bits Brent Kung adder

Carry generation network

Carry generation network is a middle stage of Brent Kung adder in which signal from the first stage will proceed with the next stage. Implementation of these operations is carried out in parallel, and then signal are carried out and converted into small pieces.

Post processing Stage

These is the last stage where, carry bits produced from second stage given next stage and that last stage is known as post processing .

2.2 Modified BEC-1 converter:

Carry select adder is fastest adder used to perform arithmetic function. In this paper, carry select adder introduce the design of simple and efficient transistor. And this modification is design to save power and area in carry select adder but delay will be not control. There are two square root carry select adder is used one with modified BEC-1 converter and another with ordinary BEC-1 converter. And 16 bit square root carry select adder modified BEC-1 converter with is compare and developed with significant square root carry select adder ordinary BEC-1 converter.

When carry select adder design for large number of bit there is a possibility of large area but BEC-1 logic have ability to reduce area. Ripple carry adder gives low power and lead to increase in area, so carry select adder prefer to use Binary to Excess-1 Converter (BEC) instant of RCA. The basic idea of this work is to use transistor level modified Binary to Excess-1 Converter (BEC) instead of Ordinary BEC (gate level) with Cin = 1 in the CSLA to achieve lower area and power consumption. The main advantage of this transistor level modified BEC-1 comes from the lesser number of MOS transistor than the Ordinary BEC-1. For simple and efficient output in VLSI hardware implementation, carry select adder architecture is design with the modified Binary to Excess-1 Converter (BEC) instant of ordinary Binary to Excess-1 Converter (BEC) to achieve low power and area.

2.3 CSLA Design is obtained using optimized logic units:

Mobile is a mini computer in VLSI hardware, which is modified and converted to smart mobile which is equally smart as computer. Now technologies become wireless and send data from one place to another place without data cables. In VLSI, system should be low power, high speed, less area. Some device like smart mobile device, wireless receivers and biomedical instrument need all these efficient parameter, which is provided by VLSI system. VLSI is a wireless system; where most of the wireless technology is been develop under VLSI system. In this paper, carry select adder study the data dependent parameter and also identify logic operation. The logic operations which are present in conventional carry select adder (CSLA) and binary to excess-1 converter (BEC) are analysed under carry select adder. We have eliminated all the redundant logic operations present in the conventional CSLA and proposed a new logic formulation for CSLA. In the proposed scheme, the carry select (CS) operation is scheduled before the calculation of final-sum, which is different from the conventional approach. Bit patterns of two anticipating carry words (corresponding to Cin = 0 and 1) and fixed Cin bits are used for logic optimization of CS and generation units. An efficient CSLA design is obtained using optimized logic units.

Carry select adder identify and analyse logic parameter, in which simulation to create a new logic optimizer for carry select adder. In which the CS operation is scheduled before the calculation of final-sum, which is different from the conventional approach. Carry words corresponding to input-carry '0' and '1' generated by the CSLA based on the proposed scheme follow a specific bit pattern, which is used for logic optimization of the CS unit. Fixed input bits of the CG unit are also used for logic optimization. Based on this, an optimized design for CS and CG units are obtained. The proposed CSLA design involves significantly less area and delay than the recently proposed BEC-based CSLA. Due to the small carry output delay, the proposed CSLA design is a good candidate for the SQRT adder.

3. PROBLEM FORMULATION

In previous time, there are no digital technologies, so all work is depend on manpower which required more time but these thing never disturb that time. Every time technology, machines become much better and become a part of our lifestyle due to which manpower reduced. According to report 75% company is digitalized and 20% is in processing, and the technology use by them should be advance. In this generation, speed is most important. Some device able to give high speed but need more energy, some satisfied both these term but they may be expensive. Taking care of all these terms carry select adder design architecture with the help of Brent Kung which not only give speed but also save power.

CONCLUSION

In this work, combination of multiplexer, Brent Kung adder, and ripple carry adder with 32 bit carry select adder form an advance design; which not only give high speed but also work on low power. Carry select adder proposed architecture with the help of Brent Kung adder which is consider being one of the fastest adder. The motive of this work is to give fastest technology to this transforming world. With changing world, techniques also need to be more advance and fast. These can be more modified by increasing number of N bits.

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REFERENCES

[1] Pallavi Saxena in paper entitled "Design of Low Power and High Speed Carry Select Adder Using Brent Kung Adder". In 2015 International Conference on VLSI Systems, Architecture, Technology and Applications (VLSI-SATA).

[2] B. Ramkumar, Harish M Kittur in paper entitled "Low power and Area efficient carry select adder". In 2012 IEEE Transactions on Very Large Scale Integration (VLSI) Systems.

[3] Basant Kumar Mohanty and Sujit Kumar Patel in paper entitled "Area–Delay– Power Efficient Carry Select Adder". In June 2014 IEEE Transactions on Circuits and Systems II .

[4] L. Mugilvannan and S. Ramasamy in paper entitled "LowPower and AreaEfficient Carry Select Adder Using Modified BEC-1 Converter" In 2013 fourth International Conference on Computer, Communication and Networking Technologies (ICCCNT).

[5] Samiappa Sakthikumaran , S.Salivahanan , and V. S. Kanchana in paper entitled "A Very Fast and Low Power Carry Select Adder Circuit". In 2011 3rd International Conference on Electronics Computer Technology (ICECT).

[6] SANJAY SINGH, K.SRINIVASARAO in paper entitled "Implementation of 4-bit carry select adder using Diode free Adiabatic Logic (DFAL)". In 2015 IEEE 2nd International Conference on Recent Trends in Information Systems (ReTIS).

[7] Govind Prasad, V Shiva Prasad Nayak , S Sachin, K Lava Kumar ,Soma Saikumar in paper entitled "Area and power efficient carry-select adder". In IEEE International Conference on Recent Trends in Electronics, Information & Communication Technology (RTEICT) .

[8] Krishnendu Dhar, Aanan Chatterjee, Sayan Chatterjee in paper entitled "Design of an Energy Efficient, High Speed, Low Power Full Subtractor Using GDI Technique" In 2014 IEEE .