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DESIGN AND SIMULATION OF POWER SUPPLY CIRCUIT FOR TR MODULES AND CONTROLLING THE POWER SUPPLY USING SPI PROTOCOL

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Abstract - *Radar is a device (Aircraft, ships etc...) that illustrates a detection mechanism and uses radio waves to determine various parameters like range, angle and velocity of the objects. The fundamental block of active phased array radar is a TR module (Transmission and Receiving). In general, active phased array radar consists of about 4000 TR modules or more based on the range and resolution requirements. A TR module receives the input supply voltage of 50+/-5V through the mother board. This power supply circuit is essential to regulate high voltage level and bring it down to the typical ±5V and 4A current. This type of voltage regulation is achieved by DC-DC convertors [3]. This paper is divided into three phases, Firstly, the simulation of power supply circuits used for powering up the TR modules.*

The next phase of the paper is using an FPGA chip to fetch data with respect to the operating temperature, voltage and current of a TR module from an ADC7927 IC through SPI. The control signals are generated by the FPGA chip only when abnormal current and voltage values are observed, or the TR module dissipates excessive heat and may affect the functioning of other TR modules within its close proximity. This paper eliminates the conventional method of switching of the power supply of the entire system when a cooling machine fails, but instead remotely monitors and controls the power supply of individual TR modules.

Key Words: TR modules, Power supply circuit, AD7927, FPGA Vertex 5, Remote ON/OFF

1. INTRODUCTION

This paper focuses on providing a thermal stable environment and an alternative solution in case the coolant system fails. There have been earlier attempts to solve the TR module failure correction but no feasible solutions were obtained especially in airborne antennas as accessibility is an issue. Hence a power supply circuit was designed (Fig 2.1) that generates 5V output from 50V input. The enable pin of the DC-DC convertor [3] is able to control the power supply.

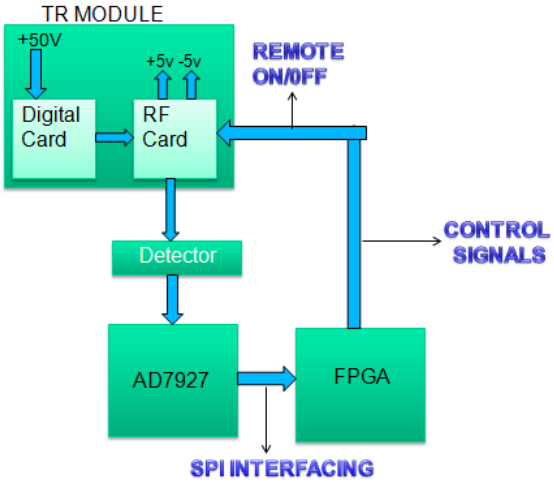

Fig 1 .1 Block Diagram of TR modules with SPI interfacing

To achieve this, a SPI protocol is designed(Fig 1.1), where the ADC7927[8] obtains real time status monitoring parameters

from the TR modules and compares it with a pre-determined parameter, if there are abnormal values, a control signal is generated that is sent as a DC pulse to the enable pin of the DC-DC convertor. This pulse indicates the IC to switch off, under such circumstances, an individual TR module[2] switched Off instead of the conventional methods of switching off the entire Radar system, Hence the parameters for thermal design of the TR modules during design process is relaxed as there is an alternative in case of harsh environments.

As the remote ON/OFF of the TR modules [2]is achieved, this paper also focuses on a increasing the ability of graceful degradation of the Radar system, this is achieved by increasing the duty cycle of the neighbouring TR modules, in such a scenario the power of the switched off modules is utilized and the affect on the Radar's performance is significantly reduced.

2. POWER SUPPLY CIRCUIT

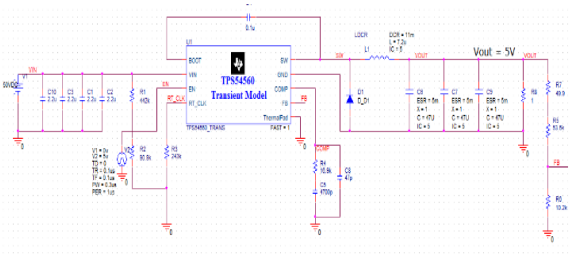

Fig 2.1 Power supply circuit

2.2 DESIGN PARAMETERS VALUES

- Output Voltage= 5 V
- Transient Response =1.25 A to 3.75
- A load step ΔVOUT = 4 %
- Maximum Output Current= 5 A
- Input Voltage 12 V nom.= 7 V to 60 V
- Output Voltage Ripple= 0.5% of VOUT
- Input Voltage (rising VIN) = 50 V

2.3 WORKING

TPS54560[7] is a step down, DC\DC convertor. It is a 16-bit 8 channel integrated chip. TPS54560[7] has static frequency, peak current mode with adjustable switching frequency. The throughput voltage i.e., 5V obtained is compared with the ferrite bead terminal with the internal resistors by using error amplifier. Current reduction takes place by comparing the COMP terminal voltage to a minimum level. In-built bootstrap voltage regulation is reset when the high side MOSFET is low. The High side MOSFET is obtained by placing 0.1Uf capacitor between BOOT and SW pins.

The potential divider circuit at output side is used to compare and set the output voltage. Efficiency of the current is increased by using layer value resistor. Noise should be avoided for greater efficiency.

3. REMOTE ON/OFF

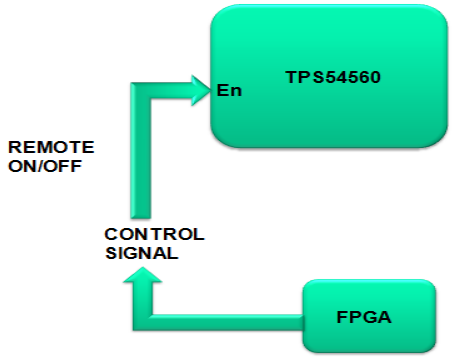

FIG 3.1 Block Diagram of Remote On/Off

3.2 EXPLANATION

REMOTE ON/OFF is one such extensive ability that can be realized in radar systems which enables the user to control the power supply to ensure no further damage is dealt to the remaining portion of the radar system and the performance of the system remains intact.

The ADC obtains real time status monitoring parameters from the TR modules, and when the module behaves in an abnormal fashion or is performing functions in a harsh environment, these modules are switched off before they may harm the functioning of other key components.

4. SPI PROTOCOL

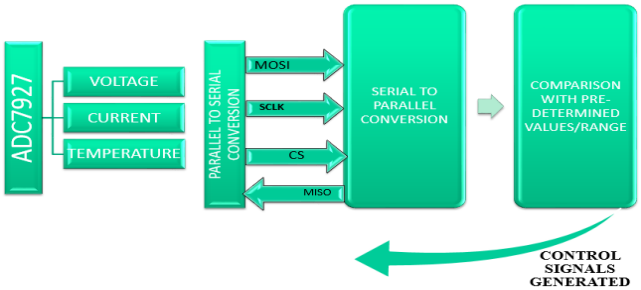

Fig 5.2 Fetching data from AD7927

ADC interacts with TR modules to obtain real time values of status monitoring parameters such as voltage, current and temperature, and constantly updates these values at a rate of 1ms (User defined). These values are converted into a serial bit stream format for communication with the FPGA via SPI. The FPGA in turn converts these values on receiving to a parallel format and compares with pre-determined conditions and generates control signals.

The SCLK signal is a 20 MHz signal used to perform data conversion. The ADC7927 performs data conversion at the falling edge of the SCLK.

CS signal in the compiler is defined as the flag, at the rising edge of the flag, the data is received and waits for the falling edge of the SCLK. Once the falling edge of the SCLK is intercepted, the data is converted.

Since there are 16bits required for the complete information to be transmitted (16-bits data, 3-bits of channel address and one leading zero) it is not possible to load this into a 12bit AD7927[8] IC. Therefore this is achieved by taking a resolution of 1/(2^12) for each sample.

The required range for the proposed system is 0-5V voltage, 0-5A current, and -40° to 125 °degree Celsius

Hence the simulation windows show 0-4096 samples where each sample equals 1.44amps or volts. And the last 4-bits of the information remain constant.

Hence the channel selection is done by the MISO signal where the FPGA requests for the values of a certain parameter and the AD7927[8] responds with the corresponding channel information only.

Before receiving the values, the data is converted from serial to parallel format for comparison with pre-determined values. Which helps in generating signals that indicate for a remote ON/OFF function to take place. Thus, concluding the SPI operation of the proposed system and constantly updates these values at a rate of 1ms (User defined). These values are converted into a serial bit stream format for communication with the FPGA via SPI. The FPGA in turn converts these values on receiving to a parallel format and compares with pre-determined conditions and generates control signals.

5. POWER UTILIZATION

The duty cycle concept is used to realize the ON period (Functioning period) of a system to its maximum operational range.

The duty cycle of any machine is a key aspect to consider during power optimization to ensure the system yields high results with optimum utilization of power. Since the implementation of remote on/off switches off a couple of TR modules functioning in the Radar, the overall power the radar yields is significantly reduced.

This resulting in the reduction of detection range of radars allowing unauthorized entities to come closer than earlier without alarms.

This is a sincere concern of security breach and needs resolve immediately. The power utilization concept comes into play in such scenarios.

Typically, each TR module produces up to 100Watts of power and functions at 10-15% duty cycle. Once the module is switched off because of malfunctioning, the neighboring TR modules can increase their duty cycle up to 18% and produce up to 120Watts; hence utilizing the available voltage of the switched off modules, and the overall power the radar yields is not affected significantly.

This is achieved by performing pulse width modulation techniques on the duty cycle, this entity is compiled on the FPGA board only when control signals are generated to the RF card of the DC-DC convertors [3].

6. FUTURE SCOPE

- **DC\DC Convertor:** Increasing the efficiency of DC\DC convertor helps in the optimization of the specific TR modules and hence provides for a better environment of relaxed constraints in designing a power supply circuit.
- **Transmit/receive efficiency:** New semiconductor material such as gallium arsenide and gallium nitride are helping to improve the efficiency of the TR modules.
- **Future of RADAR**: Placing information received through radars on the tactical network and analyzing the data through internet like interfaces or realizing radars in more secure systems and networks may open new possibilities in disseminating radar in today's growing technological applications

7. CONCLUSION

We have simulated a power supply circuit that brings down the voltage level to a standard +/-5V and 4A current.

The final observations made and studied in the circuit simulation are its Steady state AC analysis, Transient analysis, Frequency response and behavioural analysis.

This paper eliminates the conventional method of switching of the power supply of the entire system when a cooling machine fails, but instead remotely monitors and controls the power supply of individual TR modules.

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[7] Datasheet of TPS54560.

[8] Datasheet of AD7927.