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Modified Multi-level Dual Input Dual Buck Inverter

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Abstract - *A novel dual-input dual-buck inverter (DIDBI) can interface a low voltage DC source, a high voltage DC source and an AC load simultaneously. The DIDBI allows a low voltage DC source, e.g. low voltage bus, battery and renewable source, to supply power to the AC load directly, even though the voltage of the low voltage DC source is lower than the peak amplitude of the output AC voltage. Therefore, the conversion stages can be reduced to improve the conversion efficiency. In addition, the two DC sources provide multiple voltage levels for the inverter, which is benefit for reducing the switching losses and size/volume of filter inductor. Conventional DIDBI circuit is modified by reducing the circuit components. This modified circuit is successfully simulated using MATLAB R2014a. The simulation results say that the modified DIDBI has reduced 27.12% THD and improved 1.02% efficiency compared to the conventional DIDBI. A multilevel inverter is a power electronic device that is used for high voltage and high power application because of its characteristics of synthesizing a sinusoidal voltage on several DC levels. They produce lower harmonic distortion in the output. The Launch Pad TMS 320 is used for making the switching pulses. For prototype input voltages used are 10V and 20V and the obtained the maximum output voltage of 21.2V.*

Key Words: **dual input, dual buck, five-level inverter, modified DIDBI, phase opposition disposition, reduced switches**

1. INTRODUCTION

In recent years, multilevel inverters are attracting lot of attentions due to the increasing higher power quality requirements. It possesses the several features such as reduced harmonic distortion, near sinusoidal output voltage waveform and reduces dv/dt stress. As a result, multilevel inverters are used in industrial applications to meet the requirements. Inverter performs DC to AC conversion for distributed electrical energy systems and electrical vehicles. Multilevel inverter produce a stepped output voltage with are fined harmonic profile compared to two level inverters.

Among various inverter topologies, the dual buck inverter is promising because of high reliability and no dead-time requirement. In addition to these features, a dual-buck inverter has the advantage of low common mode leakage current. These features make the dual-buck inverters attractive for high efficiency and high reliability applications, such as grid-tied photovoltaic power systems and air-plane power supplies. In addition to these advantages, a dual-buck inverter still has some drawbacks, such as lower power density because of low utilization of filter inductors.

In order to overcome the drawbacks and further improve the conversion efficiency of dual-buck inverters, novel dual buck inverter topologies are still evolving. Since the dual-buck inverter can only realize step down voltage conversion, to satisfy the requirement of the peak amplitude of the AC output voltage, the DC input voltage of the inverter must be greater than the peak value of AC output voltage. However, the voltages of renewable sources, batteries, and super-capacitors are usually low and cannot meet this demand. Therefore, a front-end Boost converter is required to boot the low voltage to a high voltage level. As a result, the overall efficiency will be hurt because all the power has to be processed twice. In order to achieve high overall conversion efficiency, both the front-end DC/DC converter and the downstream DC/AC inverter should be taken into consideration. Considering the fact that the AC output voltage is time varying between zero and its peak value, it is possible that the low voltage DC source can directly supply power to the AC load in part of the voltage cycle. In these scenario, the low voltage DC source can supply power to the AC output directly and without being processed by the front-end Boost converter. As a result, the conversion stage of the overall DC/AC power system can be reduced. Meanwhile, the power losses of the front-end Boost converter can be reduced as well.

2. Conventional DIDBI

Dual Input Dual Buck inverter topology [1] has been shown in Figure 2. The circuit contains two sources, four diodes and six switches.

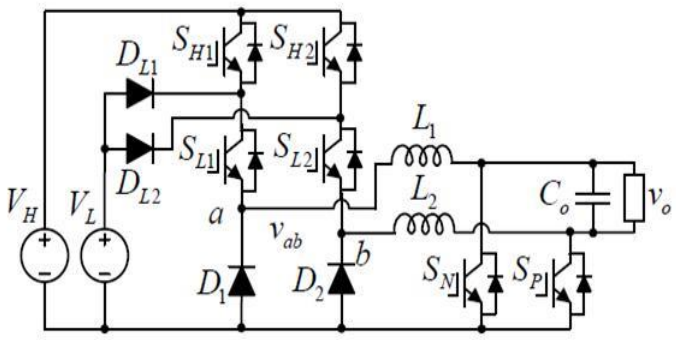

Figure 1: Circuit Diagram

V_L and V_H are the low voltage and high voltage DC port, respectively, S_{H1}, S_{H2}, S_{L1} and S_{L2} are high frequency switches while S_N and S_P are low frequency switches.

It is seen that low voltage sources, e.g. PV and battery, can be directly connected to the low voltage DC port of the DIDBI. Therefore, when the PV source or battery supplies power to the AC load/grid, part of the energy can be only processed by the DIDBI within single stage power conversion. Therefore, the power losses and power rating of the front end DC-DC converter can be reduced significantly, and the overall efficiency of the DC/AC power system can be improved.

3. Modified DIDBI

Compared to the conventional single-input dual-buck inverter, two additional diodes, D_{L1} and D_{L2}, and two switches, S_{H1} and S_{H2}, are required to extend the DC input port. In order to further simplify the inverter topology and reduce the component count of the DIDBI, the two diodes can be merged into one diode, so are the two switches S_{H1} and S_{H2}. In this case, the simplified topology of DIDBI is shown in Figure 2. The operation principle of the simplified DIDBI topology is similar to the original one. The only difference is that the high side switch, S_H, and diode D_L has to be worked in both the positive and negative half-cycle of the AC output voltage.

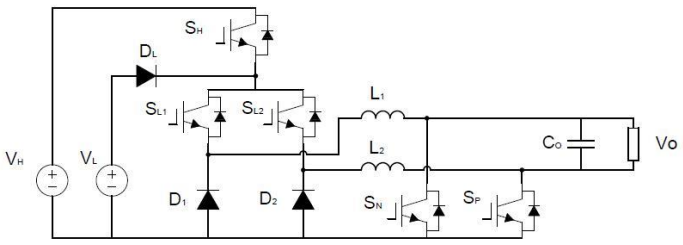

Figure 2: Circuit Diagram of Modified DIDBI

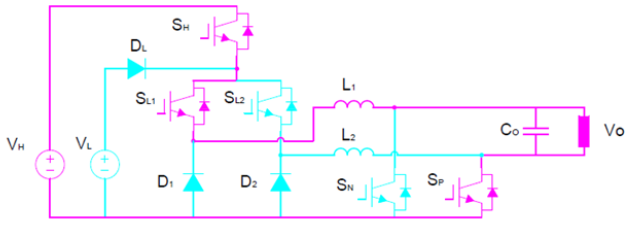

Figure 3: Modified Mode 1

In mode 1 switch S_H, S_{L1} and S_P are ON. $V_a=V_H$. The voltage applied on the inductor L_2 is zero and $V_b=0$ because the current owing through the inductor L_2 is zero. Therefore, $V_{ab} = V_a - V_b = + V_H$. The voltage of the diode D_{L1} is $(V_H - V_L)$, while the voltage on D_1 is V_H. During this stage, the high voltage port V_H supplies power to the AC output, the inductor current i_{L1} increases linearly.

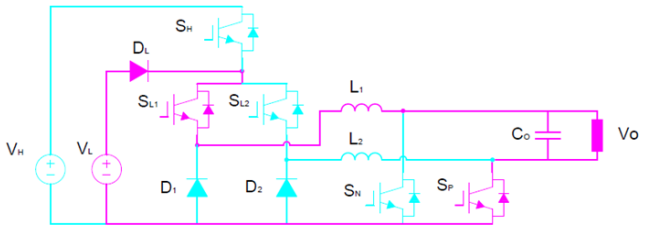

Figure 4: Modified Mode 2

In mode 2, the switches S_{L1} and S_P are ON, $V_a=V_L$. The voltage applied on the inductor L_2 is zero and $V_b=0$ because the current owing through the inductor L_2 is zero. Therefore, $V_{ab} = V_a - V_b = + V_L$. The voltage on the switch S_{H1} is $(V_H - V_L)$, while the voltage on D_1 is V_L. During this stage, the low voltage port V_H supplies power to the AC output.

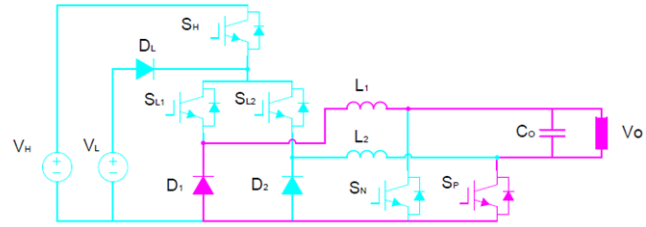

Figure 5: Modified Mode 3

In mode 3, the switch S_P is ON while the other switches are OFF. Therefore, the current of L_1 freewheels through D_1. Hence, $V_a = V_b=0$ and $V_{ab} = V_a - V_b=0$. The voltage on the switch S_{L1} is V_L, while the voltage on S_{H1} is (V_H-V_L). During this stage, neither the high voltage source V_H nor the low voltage source V_L supply power to the AC output.

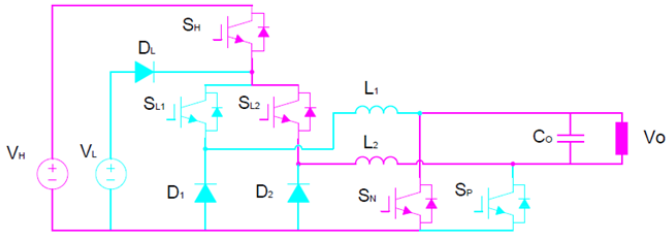

Figure 6: Modified Mode 4

In mode 4, the switches S_H, S_{L2} and S_N are ON, and the other switches are OFF. Therefore, $V_a = -V_H$. The voltage on the inductor L1 is zero and $V_b=0$, because the current owing through the inductor L1 is zero. Thus, $V_{ab}=V_a-V_b = -V_H$. The voltage on the diode D_{L2} is $(V_H - V_L)$, while the voltage on D2 is V_H. During this stage, the high voltage port V_H supplies power to the AC output, the inductor current i_{L2} decreases linearly.

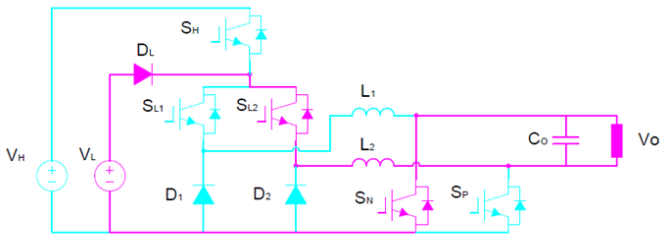

Figure 7: Modified Mode 5

In mode 5, the switches S_{L2} and S_N are ON and the other switches are OFF. $V_b=V_L$ and $V_a=0$, $V_{ab}=V_a-V_b=-V_L$. The voltage on the switch S_{H2} is $(V_H - V_L)$, while the voltage on D2 is V_L. During this state, the low voltage port V_L supplies power to the AC output.

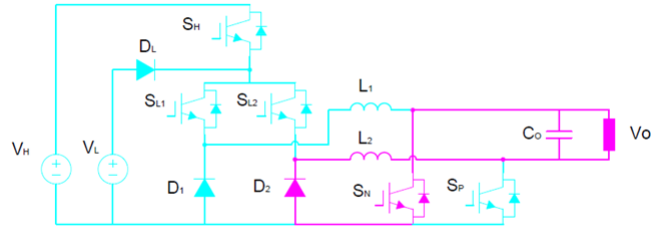

Figure 8: Modified Mode 6

In mode 6, the switch S_N is ON, while the other switches are OFF. The current of L2 freewheels through D2. Therefore, $V_a = V_b=0$ and $V_{ab} = V_a - V_b=0$. The voltage on the switch S_{L2} is V_L, while the voltage on S_{H2} is (V_H-V_L). During this stage, neither the high voltage source V_H nor the low voltage source V_L supply power to the AC output. The inductor current i_{L2} decreases linearly.

By studying the circuit diagrams of both the conventional and modified DIDBI it is noted that there is a considerable reduction in the number of components used in modified DIDBI. Instead of 6 switches and 4 diodes, modified DIDBI uses only 5 switches and 3 diodes. Thereby a considerable amount of switching loss is reduced. The modes of operation of both the conventional and modified DIDBI are almost similar.

4. SIMULATION OF MODIFIED DIDBI WITH RESULTS

4.1 Simulation Of model

The simulation is done in MATLAB/SIMULINK. The figure 9 shows the simulation circuit of DIDBI inverter. In this simulation two DC voltage sources of voltage 180 V and 90 V and 1.5 µF capacitance with load 150 kΩ are used. Switching frequency of carrier wave is 20 kHz and supply frequency is 50Hz.

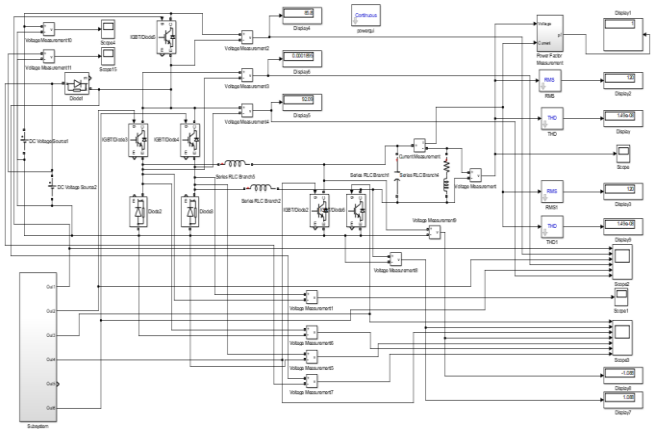

Figure 9: Simulation model of DIDBI

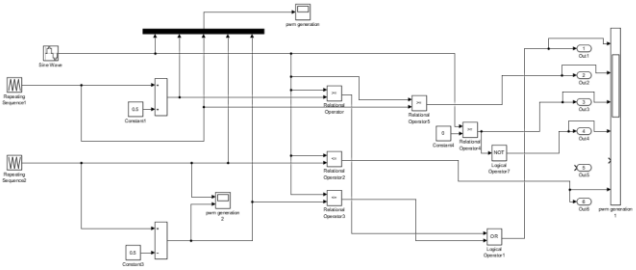

Figure 10: Subsystem of DIDBI

The figure 10 shows the subsystem of DIDBI inverter. Multi-carrier PWM schemes are used to generate gate signals. Gate signals are obtained by comparing sinusoidal signal at fundamental frequency (50Hz) with triangular carrier signal which are at higher frequency. Here switching frequency is selected as 20 kHz for better performance. Switching pulses are generated from the output of each relational operator.

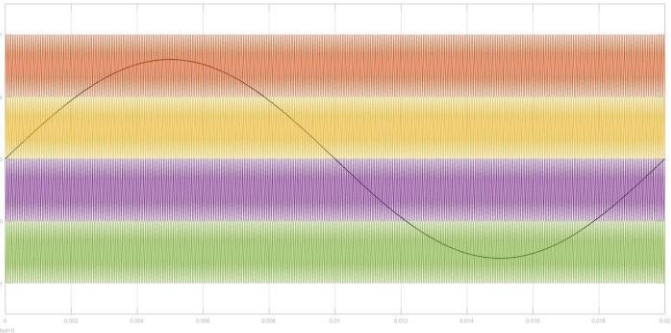

Figure 11: Sinusoidal Phase Opposition Disposition PWM

Here the carrier signal is generated based on Phase Opposition Disposition (POD) and the reference wave is sinusoidaly varying. The reference wave is continuously compared with each of the carrier signals. If the reference wave is more than the carrier signal, then active devices corresponding to that carrier are switched ON. Otherwise, the device is switched OFF.

For Phase Opposition Disposition (POD) modulation all carrier waveforms above the sinusoidal reference zero are 180 degree out of phase with those below the zero point. The carrier signals above the zero axis have same frequency, same amplitude and are in phase with each other. But those below the zero axis ,all carrier wave have same frequency ,same amplitude and in phase but all carrier waves are phase shifted by 180 degrees compared to those above the zero axis carrier waveform. In Phase Opposition Disposition, for a 5 level inverter, it requires 4 carrier signals to be compared with the one reference sine waveform as shown in figure 11.

4.2 Simulation Results

For a switching frequency of 20 kHz and reference frequency of 50Hz, the modified DIDBI inverter was simulated in Matlab Ra2016a.The simulation is carried out to analyse and compare the harmonic behavior on the value of Total Harmonic Distortion (THD).

4.2.1 Switching Pulse and Voltage Stress

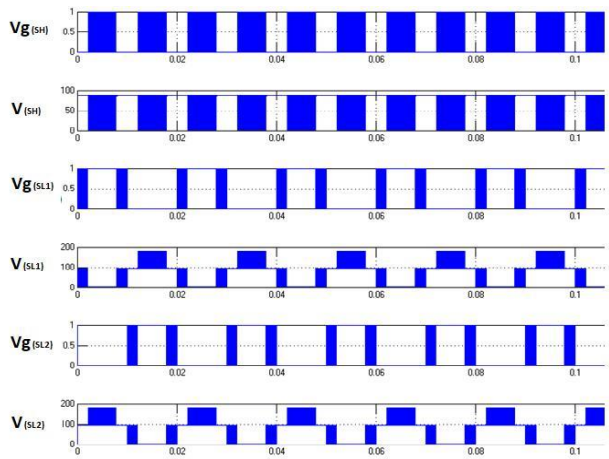

Figure 12: Switching stress of switches S_H, S_{L1} and S_{L2}

The figure 12 shows the switching pulses and switching stress across switches S_H, S_{L1} and S_{L2} using Phase Opposition Disposition (POD) technique. From simulation voltage drop across the switch SH is 85.8V and those across switches S_{L1} and S_{L2} is 94.2V.

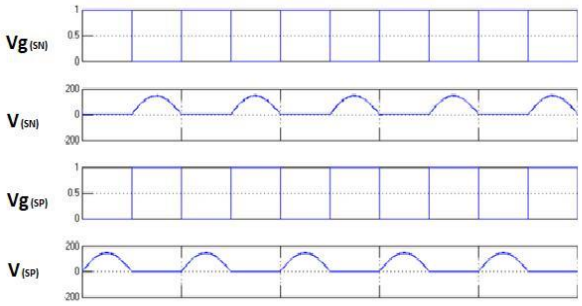

Figure 13: Switching stress of switches S_P and S_N

The figure 13 shows the switching pulses and switching stress across switches S_P and S_N .From simulation voltage drop across the switches S_P and S_N is 33.5V.

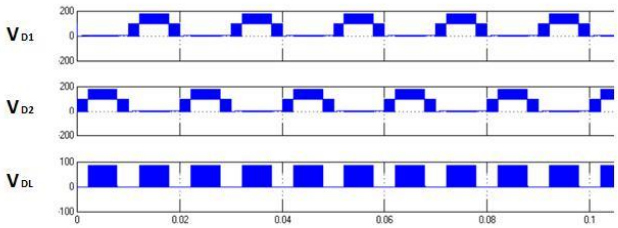

Figure 14: Switching stress of diodes

4.2.2 Input voltages

Among the two inputs provided, one is high voltage and the other one is low voltage. For simulation of modified DIDBI multilevel inverter, the applied voltage at high voltage source is 180V and that applied at low voltage source is 90V.

4.2.3 Output Quantities

Simulation is performed with two DC sources of 180V and 90V and a 150 kilo ohm resistive load. A five level inverter output before filtering contains two steps in addition to the zero level and each step holds for a particular voltage.

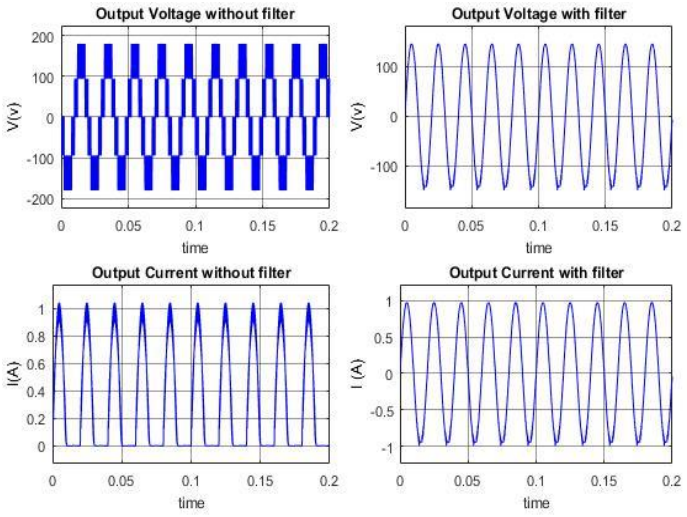

Figure 15: Output Quantities of DIDBI

4.2.4 Analysis of modified DIDBI

THD Analysis

The main criterion for assessing the quality of voltage delivered by an inverter is the Total Harmonic Distortion (THD).In this work %THD of modified DIDBI multilevel inverter is studied. Total Harmonic Distortion analysis of DIDBI is a follows.

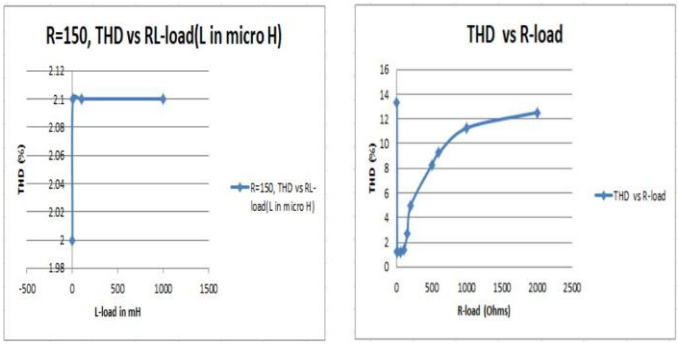

Figure 16: THD vs RL-Load and R-Load

In the analysis of %THD with different values of RL load keeping R constant at 150 Ω (figure 4.20) , %THD was found to be constant with change in L values.

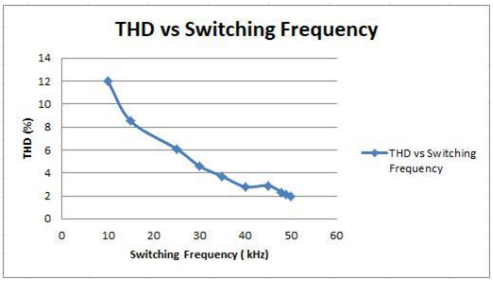

Figure 17: THD vs Switching Frequency

In the analysis of %THD with different switching frequencies (figure 17), %THD decreases as the switching frequency is increased.

FFT Analysis

The %THD of modified five-level DIDBI multilevel inverter is measured using the FFT block of Simulink.

Here % THD is calculated by considering 20 cycles of output voltage with a fundamental frequency of 50Hz.By using modified DIDBI multi level inverter the obtained THD value is 2%.

Sl no	Characteristics	DIDBI	Modified DIDBI
1	THD	7.3%	2%
2	No. of switches	6	5
3	Power Factor	0.988	0.998
4	Stress	SN,SP = 60V SL1,SL2= 120V SH1,SH2=60.8V	SN,SP = 33.5V SL1,SL2=94.2V SH = 85.8V
5	Efficiency	93.01%	94.66%

By doing various analysis like THD analysis, FFT analysis it became more clear that the modified DIDBI has better performance than the conventional DIDBI. The simulation results help to justify that the modified DIDBI has low switching loss, low THD, high efficiency and high power factor compared to the conventional DIDBI.

5. EXPERIMENTAL SETUP WITH RESULTS

The implementation of the dual input dual output inverter circuit requires mainly two steps. First is software implementation. Once the simulink program is done accurately for generating gate switching pulses for switching devices, the hardware implementation of the circuit can be carried out. Software programming is done in TMS320 Launch Pad. The switches used are MOSFET IFR540 along with its driver TLP250 which is an optocoupler used to isolate and protect the launch pad from any damage.

5.1 Switching Pulses

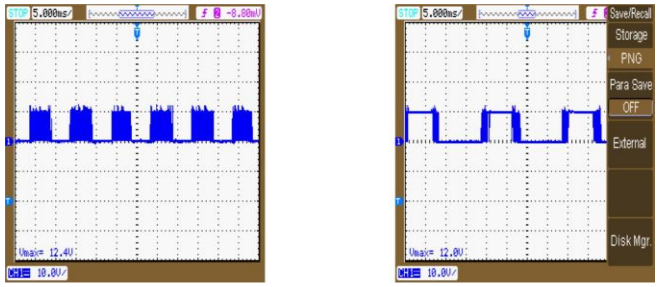

Figure 18: Switching pulse switches SH and SL1

Figure 19: Switching pulse switches SL2 and SP

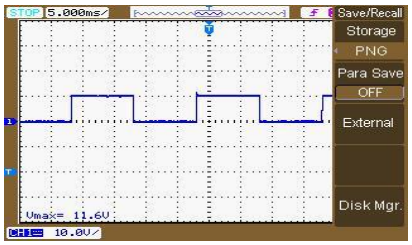

Figure 20: Switching pulse of switch SN

5.2 Hardware Implementation

Figure shows the schematic diagram of hardware prototype. To control MOSFET (IRF540) pulses are created using TMS320 Launch Pad based on Phase Opposition Disposition (POD) modulation technique. These control pulses are amplified using optocoupler TLP250. Essential pulses for turning MOSFETs have to be 15V for ON state and 0V for OFF state. Isolation between power and control circuit is done by a TLP250 driver/Optocoupler IC.

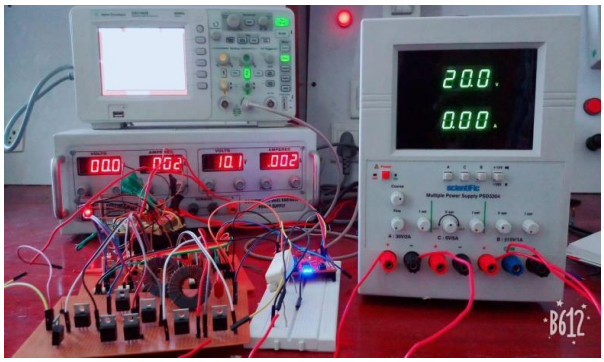

Figure 21: Experimental setup of DIDBI

5.3 Output Voltage

For the hardware prototype 100 Ω, 5W load resistor is used. Figure 22 shows the 5 level output voltage of DIDB Inverter having maximum output voltage of 21.2V with 10V and 20V as DC inputs.

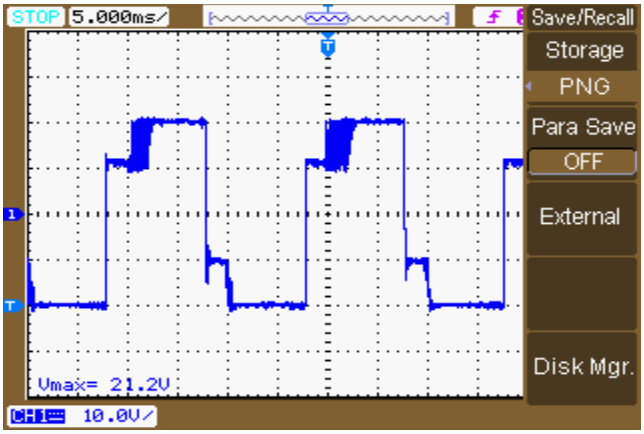

Figure 22: Output Signal without filter

The experimental result of prototype of Dual Input Dual Buck Multilevel Inverter is given here. To generate gate pulses for the switches a Simulink _le is burned in the Launch Pad TMS320.

6. CONCLUSION

A modified dual-input dual-buck inverter (DIDBI) is presented and analyzed with experimental results. A low voltage DC source is connected to the DIDBI and supplies power to the AC load directly, no matter the output voltage of the inverter is lower or higher than the low voltage DC source. Therefore, the power conversion stages are reduced. More importantly, the power losses and power rating of the front-end DC-DC converter can be reduced significantly. The modified multilevel inverter uses very less number of switching devices compared to conventional inverters. The THD has reduced to 2%, efficiency is improved to 94.6% and power factor improved to 0.998. The modified DIDBI is well applicable in Power Grids, Micro Grids and household purposes.

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