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Design of Voltage Controlled Oscillator in 180 nm CMOS Technology

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Abstract - *Voltage Controlled Oscillator is the heart of the many modern electronics as well as communication system. Hence there is necessity of VCO to operate in the GHz frequency range. This project describes a design and implementation of Five Stage Current Starved CMOS Voltage Controlled Oscillator for Phase Locked Loop. Current starved VCO is simple ring oscillator consisting of cascaded inverters. The proposed circuit is implemented in a 0.18µm CMOS technology. By varying the control voltage of VCO from 0.5 to 4.5V, the tuning range from 81.85 MHz-2.433GHz is attained. The Phase Noise at 2.4 GHz offset frequency is -89.0307 dBc/Hz. This project focuses on design of Low Power Consumption, High frequency range of VCO. Current Starved Voltage Controlled Oscillator had been designed in GPDK 180 nm CMOS Technology with supply voltage 1.8V using CADENCE spectre tool. Virtuoso Analog Design Environment tool of Cadence have used to design and simulate the schematic for the post-layout of the schematic.*

Key Words— VCO,CMOS,PLL,Layout,Mosfet.

1. Introduction

CMOS is also sometimes referred to as complementary-symmetry metal oxide semiconductor (or COS-MOS). The words "complementary-symmetry" refer to the fact that the typical digital design style with CMOS uses complementary and symmetrical pairs of p-type and n-type metal oxide semiconductor field effect transistor (MOSFETs) for logic functions. A voltage controlled oscillator or VCO is an electronic oscillator designed for producing oscillation frequency by a controlled input voltage. The frequency of oscillation is varied by the applied controlled voltage.

A voltage controlled oscillator or VCO is an electronic oscillator designed for producing oscillation frequency by a controlled input voltage. The frequency of oscillation is varied by the applied controlled voltage. A VCO plays a vital role in communication system, providing a periodic signal required for digital circuit and also a frequency transmission in digital circuit. Their output frequency is a function of control input voltage. An ideal VCO is a circuit whose output frequency is a linear function of its control voltage. Most of the application as required a variable control input voltage as they required different frequency.

Phase locked loops (PLLs) are common applications for VCOs based frequency synthesizer is usually used in RF transceivers. PLLs can be used for clock generations, such as in a microprocessor, clock andData recovery, such as in an optical transmission system, or frequency synthesis, such as in a wireless radio. The general characteristic for VCOs used in PLL is wide tuning range so that the entire frequency range is covered. Also the phase noise requirement of the VCO can be loosened due to that when the loop is locked, the noise generated by the VCO at the center of oscillation frequency will be filtered out by the loop bandwidth. As a result, PLLs generally use wide tuning range and noisier ring topology VCO.

The voltage controlled oscillator (VCO) plays a very important role in communication systems due to low power consumption, wide frequency range of operation and its high integration capability. It is an electronic device that uses amplification, feedback, and a resonant circuit to generate a repeating voltage waveform at a particular frequency. The frequency, or rate of repetition per unit time, is variable with an applied voltage. VCOs are important integral part of phase locked loops, clock recovery circuits, frequency synthesizers and in almost all digital and analog systems.

The application requirements of VCO include high frequency, low power consumption, phase stability, large electrical tuning range, linearity of frequency on the control voltage, less area, low cost and large gain factor. The design of ring VCO involves tradeoffs in terms of area, speed, power, frequency and different application domain.

2. CIRCUIT DESCRIPTION

A voltage-controlled oscillator or VCO is an electronic oscillator designed to be controlled in oscillation frequency by a voltage input. It generates a clock with a controllable frequency from -50% to +50% of its central value. The frequency of oscillation is varied by the applied DC voltage "Vcontrol". Current Starved VCO is a type of VCO based on ring Oscillator with extra CMOS acting as current source for the inverters.

2.1 OPERATION:

A ring oscillator is comprised of a number of delay stages, with the output of the last stage fed back to the input of the first. This current starved VCO is designed using ring oscillator and its operation is also similar to that. From the schematic circuit shown in the Figure 7, it is observed that MOSFETs M1 and M2 operate as an inverter, while MOSFETs M13 and M14 operate as current sources. The current

sources, M13 and M14, limit the current available to the inverter M1 and M2. In other words, the inverter is starved for the current. The MOSFETs M11 and M12 drain currents are the same and are set by input control voltage. The currents in M11 and M12 are mirrored in each inverter/current source stage. The upper PMOS transistors are connected to the gate of M11 and source voltage is applied to the gates of all low NMOS Transistors. The bias circuit is used to provide correct polarization for transistor M13 and M14. The benefit of this configuration is that the oscillation frequency can be tuned for a wide range by changing the value of control voltage.

2.2 DESIGN:

To determine the design equations for use with the current-starved VCO total capacitance on the drains of M1 and M2 is given by

$$Ctot=Cout+Cin \quad (2.1)$$

$$Ctot=Cox*(WpLp+WnLn)+(3/2)*Cox*(WpLp+WnLn)$$

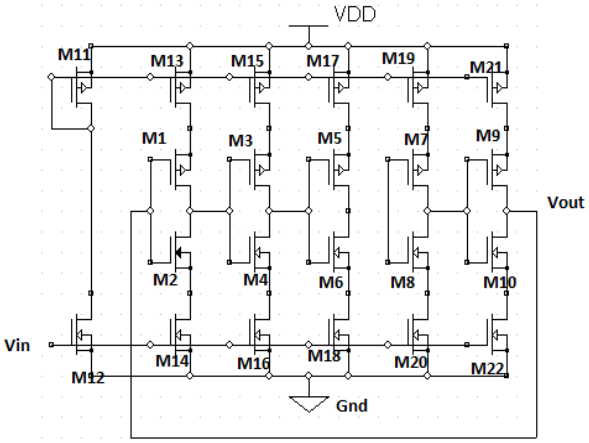

Fig 2.2.1 CS-VCO

This is simply the output and input capacitances of the inverter. The equation can be written in more useful form as

$$Ctot=(5/2)*Cox*(WpLp+WnLn) \quad (2.2)$$

The time it takes to charge Ctot from zero to Vspwith the constant current Id4 is given by

$$t1=Ctot*(Vsp/Id) \quad (2.3)$$

While the time it takes to discharge Ctot from VDD to Vspis given by

$$t2=Ctot*((Vdd-Vsp)/Id1) \quad (2.4)$$

If Id1= Id2=Id(which is labeled as Idcenterwhen in VCO then the sum of t1and t2is simply

$$t1+t2=Ctot*(Vdd/Id) \quad (2.5)$$

The oscillation frequency of the current starved VCO for N (an odd number >= 5) of stages is

$$Fosc=1/(N*(t1+t2))$$

Substitute t1+t2 value in Fosc Equation

$$Fosc=Id/(Vdd*Ctot*N) \quad (2.6)$$

The centre frequency (f centre) of the VCO when Id=Idcenter. The VCO stops oscillating, neglecting sub-threshold currents, when in Vvco<Vth. Therefore, Vmin= Vth and Fmin= 0.The maximum VCO oscillation frequency, Fm axis determined by finding Id when in Vvco=Vdd. At the maximum frequency, Vmax=Vdd.

The output of the current starved VCO normally has its output buffered through one or two inverters. Attaching a large load capacitance on the output of the VCO can significantly affect the oscillation frequency or lower the gain of the oscillator enough to kill oscillations altogether. The average current drawn by the VCO is

Iavg=(N*Vdd*Ctot)/(T)

Here , Fosc=1/T

Iavg=Id

Id=N*Vdd*Ctot*Fosc

$$Fosc=(Id)/(N*Vdd*Ctot) \quad (2.7)$$

Here, Fosc =Oscillation Frequency of VCO

N=No of stages in VC0

Vdd=Supply Voltage

Ctot=Total Capacitance of MOSFET'S M1 and M2

Id=Drain Current

Cox=Oxide Capacitance (8.784*10^-15 F/μm^2)

For 180 nm Technology,

$$Cox=(Eo*Er)/Tox \quad (2.8)$$

Eo=8.85*10^-18 F/μm^2

Er=3.97

Tox(Thickness of Oxide)=4*10^-9

Substitute the values in formula and we get,

$$Ctot=(5/2)*Cox*(WpLp+WnLn) \quad (2.9)$$

Ctot=(5/2)*(8.784*fF/μm^2)*((1μ*180n+1μ*180n)

Ctot=7.9056fF

$$Fosc=(Id)/(N*Vdd*Ctot) \quad (2.10)$$

Fosc=(176*10^-6)/(5*1.8*7.9056*10^-15)

Fosc=2.4 GHz

Table 2.1 Aspect Ratio of Transistor

DEVICE NAME	DEVICE TYPE	ASPECT RATIO(µm/nm)
M11,M13,M15,M17,M19,M21	PMOS	2/180
M1,M3,M5,M7,M9	PMOS	1/180
M2,M4,M6,M8,M10	NMOS	1/180
M12,M14,M16,M18,M20,M22	NMOS	2/180

3. PRELAYOUT DESIGN AND OUTPUT

The heart of the PLL circuit is the voltage controlled oscillator. The circuit is designed to give a center frequency of oscillation of 2.4GHz. The frequency of oscillation of the output signal for the different input control voltage is mentioned in the Table 3. The center frequency of oscillation at an input control voltage of 1.8 V. The schematic view of VCO is shown in the fig 3.1 &the output signal of the VCO is shown in the fig 3.2.

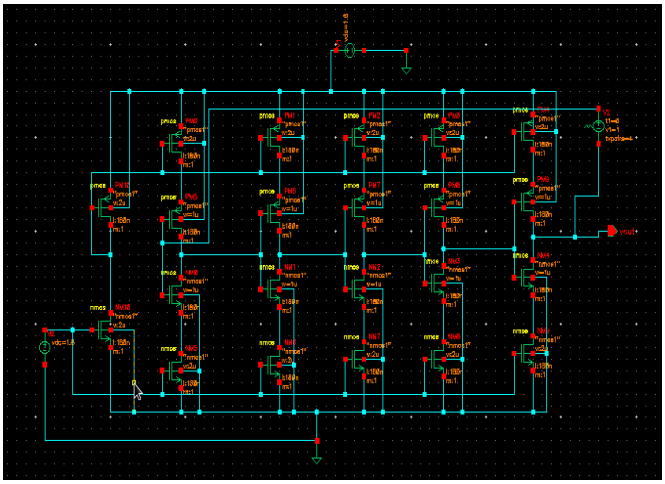

Fig 3.1 Schematic View of CSVCO

3.1 OUTPUT OF VCO:

Modern CMOS designing is very much based upon reducing power consumption and stability of designed circuit. Looking at the results from Figure 9, the highest frequency obtained at 1.8V control voltage is 2.401 GHz. Table 1 shows the setup of the aspect ratio of this experiment, and the results in Table 3 shows the starting frequency from 0.4V to 1.8V control voltage. This implies that the initial setup of the MOS devices aspect ratio needs to be adjusted for VCO higher frequency. The simulation shows varying frequency with respect to time. Power dissipation is observed for frequency near to 2.4 GHz for wireless operations. Current Starved Voltage Controlled Oscillator with 5 inverter stages generates frequency 2.401 GHz in 180nm technology. Graphical Representation of Output Frequency VS Control Voltage is shown in table 3.1.

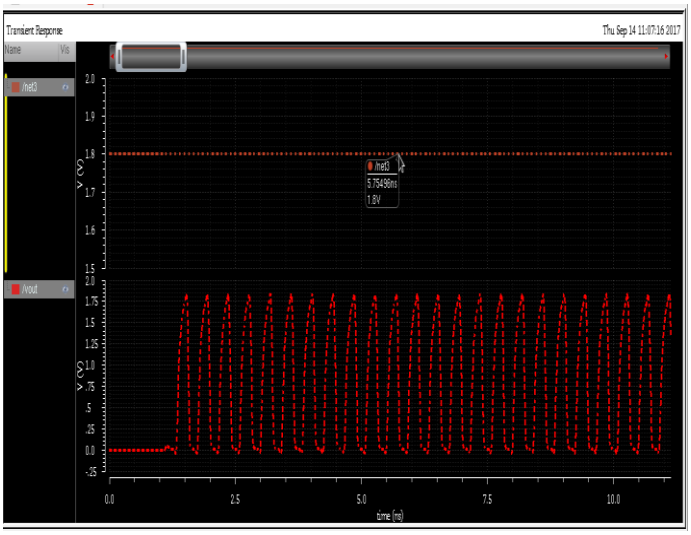

Fig 3.2 Output View of CSVCO

Now the performance analysis for the CSVCO is as shown in table3.1 with different voltages for generating the different frequencies.

Table 3.1 Control Voltage VS Frequency

CONTROL VOLTAGE (VOLT)	FREQUENCY(Hz)
0.4	-
0.5	81.85 M
0.6	441.4 M
0.7	1.09 G
0.8	1.644 G
0.9	1.975 G
1.0	2.146 G
1.1	2.236 G
1.2	2.289 G
1.3	2.324 G
1.4	2.349 G
1.5	2.367 G
1.6	2.381 G
1.7	2.392 G
1.8	2.401 G

The voltage and frequency are varies with linear and the graph shown below.

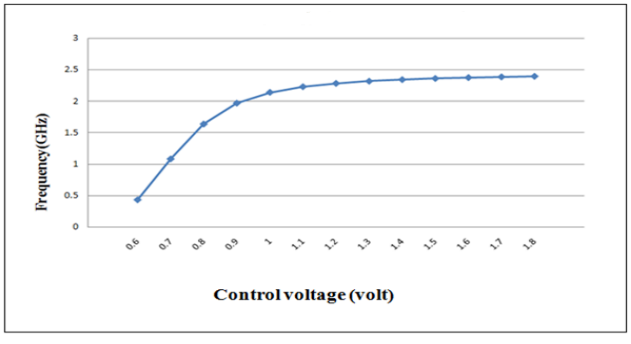

Fig 3.3 Graphical Representation of Output Frequency VS Control Voltage

Table 3.2: Frequency comparison

CONTROL VOLTAGE (VOLT)	FREQUENCY (Hz) REF(1)	REF(2)	REF(3)	REF(4)	PROPOSED WORK
0.4	21.32 M	-	-	Frequency Range (30MHz-1.13GHz)	-
0.5	23.05 M	342.421M	-		81.85M
0.6	23.29 M	675.67M	165.23M		441.4M
0.7	23.57 M	1.244 G	438.94M		1.09G
0.8	25.67 M	1.532 G	754.46M		1.644G
0.9	26.30 M	1.638 G	1.061 G		1.975G
1.0	26.99 M	1.683G	1.333 G		2.146G
1.1	27.62 M	-	1.562 G		2.236G
1.2	28.24 M	-	1.762 G		2.289G
1.3	28.77 M	-	1.926 G		2.324G
1.4	29.34 M	-	2.041 G		2.349G
1.5	29.80 M	-	2.118 G		2.367G
1.6	31.11 M	-	2.200 G		2.381G
1.7	32.52 M	-	2.247 G		2.392G
1.8	33.83 M	-	2.307 G		2.401G

Here the frequency of the designed VCO is compared with the reference papers by changing the control voltage as 0.4 V to 1.8 V.When compared to the REF (1) , it produce the frequency in MHz range.In REF(2) , it produces the frequency ranges from MHz to GHz.In REF (3), it produces the maximum frequency of 2.307 GHz. In REF(4), the frequency ranges from 30 MHz to 1.13 GHz. In the designed VCO, the maximum frequency produced is 2.401 GHz.

In below Here the VCO parameters like input tuning range,frequency range and power consumption are compared with the reference papers .Finally concluding that the designed VCO has better parameters than others. The reference papers taken are worked with the 180nm technology. In REF(1), it consumes the power of 105.3 mW with the input tuning range of 0.4 V to 1.8 V. In REF(2), it consumes the power of 0.2128 mW with the input tuning range of 0.5 V to 1V. In REF(3), it consumes the power of 1.2357 mW with the input tuning range of 0.6 V to 1.8 V. In REF(4), it consumes the power of 0.361 mW with the input tuning range of 0.5 V to 2.1 V.

In our work the power consumed is 1.038 mW and the input tuning range is of 0.5 V to 4.5 V

Table 3.4: Overall Comparison

PARAMETER	REF(1)	REF (2)	REF (3)	REF (4)	THIS WORK
Technology	180 nm	180 nm	180 nm	180 nm	180 nm
Power Supply	0.1 V	1.8 V	1.8 V	1.8 V	1.8 V
Input Tuning Range	(0.4-1.8)V	(0.5-1) V	(0.6-1.8) V	(0.5-2.5) V	(0.5-4.5) V
Frequency Range	(22-315) MHz	342.42 MHz-1.683GHz	165.25 MHz-2.3073 GHz	30 MHz-1.13GHz	81.85 MHz-2.433GHz
Power Consumption	105.3 Mw	0.2128mW	1.2357 mW	0.361 mW	28.36 nW
Phase Noise	-	-	124.52 dBc/Hz @1 MHz	-99.70 dBc/Hz @1 MHz	-89.0307 dBc/Hz @2.4GHz

4. POST LAYOUT

In the pre layout ,only the functioning of the circuit is analysed (i.e) when a particular value of input is given to the circuit ,it produces the corresponding output .But the post-layout of the voltage controlled oscillator is designed to analyse the parasitic values like resistance, capacitance in the pre –layout circuit . The metals placed will act as the capacitor which includes additional value to the layout These parasitic values may affect the power consumed by the voltage controlled oscillator. To overcome those effects post layout design is generated.

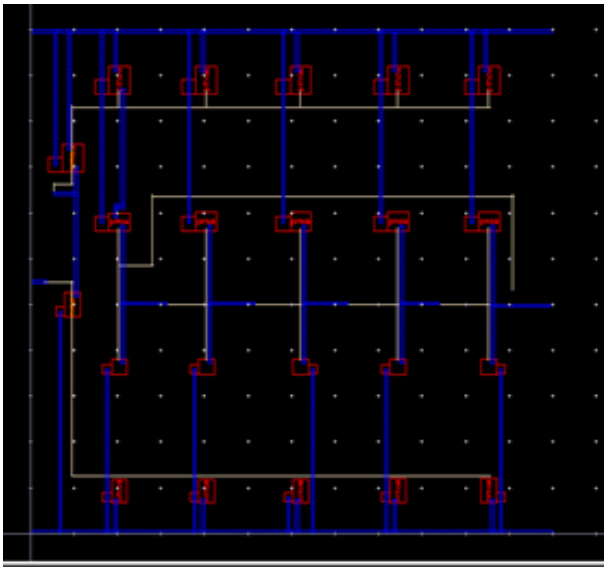

Fig 4.1 Post-Layout of VCO

The above fig.6.1 layout is created to fabricate the IC without any defects. The layout is created in order to reduce the area and the power consumption by the electronic devices. At the required frequency this post layout is designed.

4.1PRE-LAYOUT POWER VS POST-LAYOUT POWER

The pre layout has the low power value as they doesn't have any parasitic values .The power consumption of the post layout is highas they include parasitic values like resistance, capacitance in electronic devices .

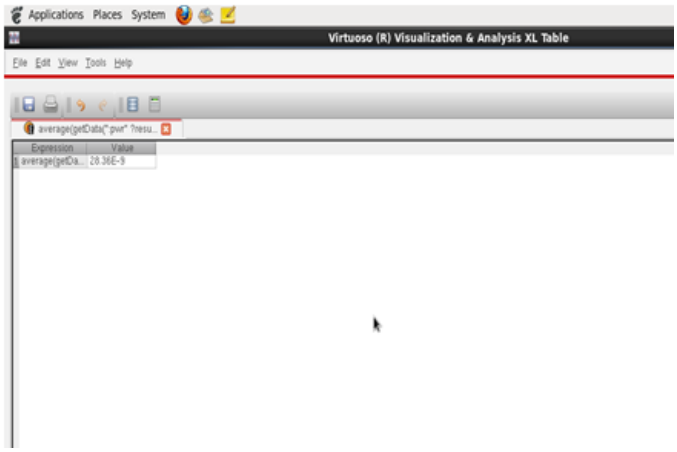

Fig 4.1.1 Power of pre-layout VCO

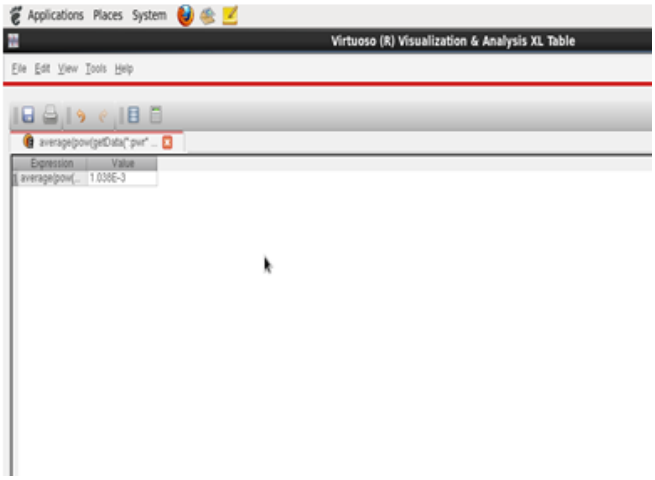

Fig 4.1.2 Power of post-layout VCO

The above fig 4.1 shows that the schematic (pre-layout) of the voltage controlled oscillator consumes the minimum power which is 1.038 mW**.** The schematic is designed only to check the functionality of the VCO circuit properly.

5. CONCLUSION

In this work a VCO with a better Frequency is presented. The Frequency of the VCO is found to 2.4 GHz. The VCO circuit consumes a power of 1.038mW from a 1.8 V D.C. supply. The centre frequency of oscillation of the VCO depends upon the sizing of the transistors. The frequency deviation from the desired value can be reduced by properly choosing the transistor sizes. The other constraints like Frequency Range, Input Tuning Range and phase noise are also measured. We observed that in current starved voltage controlled oscillator (VCO) generates 2.4GHz frequency at input control voltage (Vin) of 1.8V. Since Phase locked loop (PLL) is widely used in wireless communication systems. We can generate any desire frequency based on application requirement. The post layout of the voltage controlled oscillator is designed and configured with the schematic circuit of the voltage controlled oscillator. It consumes the minimum power value which can be used in the other application circuits. This layout can be fabricated in the integrated chips (IC) for various communication purposes .

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