POWER SCHEDULING ALGORITHM BASED POWER OPTIMIZATION OF MPSOCS

Prof. S. Shanmuga Raju[1], Nivetha B[2], RajaDarshini N[3], Ranjith M[4], Sandhiya E[5].

[1]Professor, Dept. of ECE, Dr. N. G. P. Institute of Technology, Cbe, Tamil Nadu, India.
[2,3,4,5] Student, Dept. of ECE, Dr. N. G. P. Institute of Technology, Cbe, Tamil Nadu, India.

ABSTRACT - *Dynamic voltage frequency scaling (DVFS), which is an efficient methodology to provide sufficient energy for the core which needs an energy. But it is lagging when it get implemented in the desired constraint of an circuit. The leakage of power is reduced by C-Mos under static conditions. Our aim is to put CAD methodology for an efficient delivery of the power. The choice of LDO or FIVR as power regulator is user for power performance on On-chip processor for power delivery units*

KEYWORDS: DVFS, SCS, Decoupling capacitors, ECC, LDO, FIVR, Holistic, SCNs, VFI, SC, Folded-Tree, Power gating.

INTRODUCTION:

In a multi core processor, the power consumed by each core is very less. But, the overall power consumption of all the cores is considerably large. So, the proper regulation is to done to provide each core with its required power. This scaling process is called Dynamic Voltage Frequency Scaling. There are two ways to implement regulation, Fully Integrated Voltage Regulator (FIVR), Low Dropout Regulator(LDO). The use of LDO is more efficient than FIVR. Here, some of the papers discusses the characteristics of the LDO and how it can be implemented in the multi core processor for regulation purposes to reduce the power consumption.

Decoupling capacitors are used to separate c-mos circuits. Meta-insulator-metal is used at the output of decoupling capacitors in order to have good transient characteristics. Ceramic capacitor are used at the input terminal. A scheme which reduces power consumption under static conditions by multi threshold c-mos. It also supports multiple power off-modes and reduces leakage of power.

RELATED WORKS:

Koushik Charaborty, et al (2013) states that DVFS is an adoptable technique used for delivering efficient energy. In recent days this technique is becoming inefficient because of two reasons--Based on reliability criteria, supply voltage is not up to the scale level and Dynamic Adaptations is not possible for high power consuming circuits under nominal frequency. DVFS is lagging by 22%-86%, which is in comparison with ground up design .the paper concentrates on energy efficient multi core systems. Using computer aided design (CAD)identical cores are integrated in different voltage frequency domain .the CAD architecture is simulated ,with that we can see improvement of 11%-22%.

Tasreen Charania, et al(2013) state's that there is still noise factors due to power supply, which remains a challenge in CMOS technology decoupling capacitors (Decaps)which is ON-chip are used for suppression of noise that is in association with area and leakage costs .there are various methods to implement Decaps ON-chip but those are not applicable for the given constraints. This paper discusses various Decaps implementation --MOS based Decaps, MIM(Metal insulator Metal)Decaps and Multilayer metal Decaps. It exists in post layout this must be implemented in CMOS technology-65nm.based on area, location, leakage Decaps or designed. To boost the efficiency by25% n-MOS Decaps are used.

Jen-Wei Lee, et al(2014) states that Elliptic Curve cryptography [ECC] is portable with high demand to transfer information over wireless channels. It is a high complex technique but it can be overcome with hardware architecture for sufficient ECC performance. During power analysis to the circuit the private key is revealed from cryptography ICs. Information leakage is happen through side channel. Power analysis can be done by either hetero type dual processor architecture are priority oriented scheduling. Memory hierarchy is built for dual field with local memory to improve the bandwidth. It improves not only the hardware efficiency also protect the power analysis attack.

Cedric Walravens, et al(2014) claims out in wireless sensor networks radio communication consumes more power. In order to communicate data on node the energy from the battery is limited. Off the shell low power microcontrollers were designed but low power consumption is achieved only when more processing elements are used. A folded tree architecture is proposed in wireless network by parallel prefix and data locality. By implementing this on silicon and compare with microcontroller, it is found to be 10-20X the energy is improved.

Zhaobo Zhang, et al(2014) estimates under static conditions the leakage of power is reduced by multi threshold C-Mos .A scheme is already been proposed to support multiple power off modes and to reduce leakage of power in static modes. It lags with high sensitivity to radiations and therefore in manufacturing. A new power gating technique is proposed to tolerate the sensitivity to changes and can be scalable between the two intermediate power Off modes. The outcomes are less design effort , high power reduction, smaller area than previous method. This method is combine exciting methodology to offer more static power reduction.

Hamid Reza Ghasemi, et al(2014) explains that for a particular power the per core voltage domain performance can be improved. All processors cores has single voltage domain. Because of splitting based on core and powering with multiple Off chip for high cost platform. On chip voltage regulators are used as alternate solutions, high quality inductor are integrated which is a challenging task. Cost effect of the device plays a major concern. This methodology says core to core voltage variation are small and per core feedback control is used which is cost efficient. Core to core is used to increase the efficiency of voltage regulation.

Chung-Hsun Huang, et al(2014) experimented that an LDO reduces 1V of input to the 0.85-0.5V in 90nm c-mos technology. Trans conductance amplifier is used as error amplifier [EA], the current splitting technique of EA is used to improve the gain. Also it increases closed loop bandwidth of LDO. In Rail-to-Rail output of EA, minimizing the size of mos transistor the power noise is cancelled. EA path can be reused for designing transient accelerator. Due to all this advantages LDO can operate in wider range with current efficiency of 99.94%, 28mv output for 0-100 mA low transient. The area of LDO is 0.0041mm^2, for compact design.

Pingqiang Zhou, et al(2014) proposed that an Switched capacitor is integrated on-chip to support multi core power delivery of DVFS. Various levels of voltage supply are provided by DC-DC converter's which is capable of multiple conversion ratios. With the distribution result the voltage drop is seems to be reduced and also for better power regulation. Current distribution is unbalanced so CAD system is used to automate the design and distribution. Power loss models were developed as a function of size and distribution. After this an approach was introduced to optimize the SC converter's to increase the efficiency of the system. The optimized result is demonstrated on homogeneous and heterogeneous multi core chips.

Michael Leaders, et al(2014) proposed the concept called holistic power saving is used in ultra low power microcontroller systems. This involves application requirement, system architecture, circuit design technology. LDO is enhanced by making it digitized, by supplying the MCU. With this technology LDO can operate to a maximum of 256mA and to the quiescent current of 659nA. Power consumption is reduced drastically and current saving is 31%, when it operates at low clock speeds of 1MHz. Simultaneously output capacitor is used with low power consumption during sleep mode and energy is efficient in wake-up condition. Therefore the performance is improved by the factor of 4.6.

Ruzica Jevtic, et al(2015) studies that SC converter's, Dc-Dc converter's offers only limited conversion of efficiency under traditional implementation. DVFS with SC improves converter efficiency. This allowing output to ripple and processor core frequency is used to track the ripple. Differential modes of converter's and biasing are followed to achieve minimum core energy. I'm the model of 28nm technology with efficiency of 90% and 25% improvement is achieved in the overall chip efficiency.

Ashis Maity, et al(2016) states that in embedded application, the single stage regulator topologies are used for low power consumption. It has unidirectional behavior and frequency compensation. For single stage the DC load power is poor because of low differential again, over a wide range. LDO is used to achieve the DC load power regulation. Thus can also be applicable for multistage. In order to achieve this adaptive biasing is modified and this amplifies common mode and differential mode. On-chip and off-chip conditions are included for making output capacitance constant. It delivers 100mA load current, DC load regulation is 0.140mV per MA and it is stable with a Co<=3.3nf, on-chip and Co>= 1micro farad, off-chip.

Ryan Gary kim, et al(2017) proposed that Power and thermal constraints dominate the high performance chip. But it have been influenced in computing and data analysis. An efficient energy is carried by Voltage Frequency Island [VFI]. Energy can be saved by dynamically performing VFI. Dynamic VFI based on Immediate Learning [IL] control system core. Because IL is successive over Reinforced Learning [RL]. RL is a strong base in an EDA community. So it ensures that IL is well efficient and higher than RL. It also has of less computation time along with larger area which have been defined as 3.1X and 8.8X respectively.

Natan Krihely, et al(2013) states that in order to keep high efficiency in load voltage down to 200mV a method of binary resolution is implemented in Switched Capacitor Converter [SCC]. To make SCC more efficient it have been presented with digital system along with 1.1v battery. The sub threshold values can be obtained around 0.18-0.6v based on the configuration of a converter which is 40nm of C-Mos and constant low

power. Simulation have been performed and obtained an efficiency of 10-11% with 200mV and it also has been compared with anther aspects. From which we infer that an SCC can be implemented with multi-topology to increase effectiveness and preserver over flow of voltages in circuits.

Tongda WU, et al(2017) states that source which is unstable and limited is solar energy. Its respective sensor lags due to higher values in Deadline Miss Ratio [DMR]. The methodology of Solar-Powered Sensor Nodes [SPSNs] with storage of energy have greater potential in IOTs. To achieve DMR value to higher in dual channel, scheduling has to be made in single queue not in long term task. In order to reduce long term a scheduling of 3 level based DVFS should be framed. It also has an approach of Day-level scheduler by coarse grained task, Neural networks by priority of task, DVFS based algorithm by slot level execution

Seyed Alireza Zahrai, et al(2017) proposed that for a low power application and high speed device, an 8-bit 1-GS/s of hybrid ADC is framed. It has of two stages. First stage is of 3-bit ADC flash and second stage consists of 5-bit four channel time interleaved comparator which is completely based on asynchronous binary search. In every channel a sampling is performed by merging sample and hold along with capacitive DAC. The process over parasitic capacitance is analysed and alternate method is introduced which enable high speed power efficient. The sampling network introduce of error reduction to alleviate an feedback of bootstrap. In an extra channel of flash ADC comparators offset is calibrate with reference signal. By undergoing with simulation, it infer of 1-GS/s of 130nm C-Mos and ADC has an greater efficiency than 7.37 bits up to Nyquist frequency when there is an input of 13.3mW and supply of 1.2v.

CONCLUSION:

A detailed description of the regulating technology, DVFS and its characteristics is presented in this paper. DVFS was initially lagging in energy , it was later rectified. Noise suppression was done using DVFS. FIVR and LDO are the most important regulating schemes used under DVFS. Most of the papers have conveyed LDO seems to be inefficient than FIVR. Switched capacitors, power gating technology, holistic power saving, folded tree method in CAD and SCNS are discussed. So, it is shown that FIVR suits perfect for optimizing a multi core processor in power. If the FIVR is perfectly implemented on chip, the power is optimised to the desired level, for the core which is currently in working.

COMPARISON:

S.No	Technology	Description	Year
1.	Synopsis Design Compiler	DVFS was found to be lagging by 22% to 86% in multi systems. Using CAD, simulated result provides the improvement of 11% to 22%	2013
2.	Decaps in 65 nm C-Mos technology.	Decaps were used to suppress the noise which has raised due to the power.	2013
3.	SCC 1.1V of battery system	In order to preserve high efficiency at load conditions, binary resolution is implemented.	2013
4.	Heterogeneous dual PE and ECSM processing techniques .	Power analysis is done using two methodologies. Hardware efficiency along with protection of power analysis attacking was improved	2014
5.	Multi- threshold C-mos of power gating	It is used for handling the sensitivity of variations in the circuit.	2014
6.	Folded tree architecture in wireless network.	It was designed by parallel prefix and data locality implementing on Si.	2014
7.	LDO of 90nm on C-mos technology.	Gain is increased by closed loop which is called rail – to – rail output of error amplifier.	2014
8.	DVFS along with SC and model of power loss by CSD methodology.	With the simulated result of SC converter voltage drop is reduced and power regulation is better.	2014
9.	Application based holistic power for ultra MCU.	The performance of LDO is improved by making it digitized. Current saving is around 31% and performance is improved by the factor 4.6	2014

10.	Power technique for core to core and per core.	High- Quality inductor is integrated on-chip for high performance. Two techniques are used for its cost effectiveness.	2014
11.	Switched capacitor with dc-dc converter on c-mos processor.	DVFS with SC improves efficiency. Different modes of converter and biasing are used to achieve the minimum core energy.	2015
12.	Single-stage biased LDO.	LDO is used to achieve the dc load power regulation. Also applicable for multi – stage applications.	2016
13.	IL and RL for DVFI systems.	IL based technique is proposed to control the energy many cores. IL is more reliable than RL.	2017
14.	3 level DVFS for dual channel SCNS.	Scheduling strategy is used to reduce long term DMR.	2017
15.	Hybrid ADC 8- bit.	Design approach reduces the sampling capacitance and allows error detection techniques.	2017

REFERENCES:

1. IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 21, NO. 4, APRIL 2013. Architecturally Homogeneous Power-Performance Heterogeneous Multicore Systems. Koushik Chakraborty and Sanghamitra Roy, Member, IEEE.

2. IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 21, NO. 4, APRIL 2013. Analysis and Design of On-Chip Decoupling Capacitors Tasreen Charania, Senior Member, IEEE, Ajoy Opal, Member, IEEE, and Manoj Sachdev, Fellow, IEEE.

3. IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 22, NO. 1, JANUARY 2014 49. Efficient Power-Analysis-Resistant Dual-Field Elliptic Curve Cryptographic Processor Using Heterogeneous Dual-Processing-Element Architecture Jen-Wei Lee, Student Member, IEEE, Szu-Chi Chung, Student Member, IEEE, Hsie-Chia Chang, Member, IEEE, and Chen-Yi Lee, Member, IEEE.

4. IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 22, NO. 2, FEBRUARY 2014 313. Low-Power Digital Signal Processor Architecture for Wireless Sensor Nodes Cedric Walravens, Member, IEEE, and Wim Dehaene, Senior Member, IEEE.

5. IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 22, NO. 1, JANUARY 2014 13. Static Power Reduction Using Variation-Tolerant and Reconfigurable Multi-Mode Power Switches Zhaobo Zhang, Student Member, IEEE, Xrysovalantis Kavousianos, Member, IEEE, Krishnendu Chakrabarty, Fellow, IEEE, and Yiorgos Tsiatouhas, Member, IEEE.

6. IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 22, NO. 4, APRIL 2014 747. Low-Cost Per-Core Voltage Domain Support for Power-Constrained High-Performance Processors Abhishek A. Sinkar, Hamid Reza Ghasemi, Michael J. Schulte, Ulya R. Karpuzcu, and Nam Sung Kim, Senior Member, IEEE.

7. IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 22, NO. 6, JUNE 2014. Design of a Low-Voltage Low-Dropout Regulator Chung-Hsun Huang, Member, IEEE, Ying-Ting Ma, and Wei-Chen Liao.

8. IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 22, NO. 9, SEPTEMBER 2014. Distributed On-Chip Switched-Capacitor DC–DC Converters Supporting DVFS in Multicore Systems Pingqiang Zhou, Ayan Paul, Chris H. Kim, Senior Member, IEEE, and Sachin S. Sapatnekar, Fellow, IEEE.

9. IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 21, NO. 12, DECEMBER 2013 2353. Efficiency Optimization of a Step-Down Switched Capacitor Converter for Sub threshold Applications Natan Krihely, Sam Ben-Yaakov, and Alexander Fish.

10. IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 22, NO. 11, NOVEMBER 2014 2287. Architectural and Circuit Design Techniques for Power Management of Ultra-Low-Power MCU Systems Michael Lueders, Bjoern Eversmann, Johannes Gerber, Korbinian Huber, Ruediger Kuhn,

Michael Zwerg, Doris Schmitt-Landsiedel, and Ralf Brederlow, Senior Member, IEEE.

11. IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 23, NO. 4, APRIL 2015 723. Per-Core DVFS With Switched-Capacitor Converters for Energy Efficiency in Manycore Processors Ruzica Jevti´c, Member, IEEE, Hanh-Phuc Le, Member, IEEE, Milovan Blagojevi´c, Member, IEEE, Stevo Bailey, Student Member, IEEE, Krste Asanovi´c, Fellow, IEEE, Elad Alon, Senior Member, IEEE, and Borivoje Nikoli´c, Senior Member, IEEE

12. IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 24, NO. 6, JUNE 2016 2117. A Single-Stage Low-Dropout Regulator With a Wide Dynamic Range for Generic Applications Ashis Maity, Student Member, IEEE, and Amit Patra, Member, IEEE.

13. IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 25, NO. 9, SEPTEMBER 2017. Imitation Learning for Dynamic VFI Control in Large-Scale Manycore Systems Ryan Gary Kim, Member, IEEE, Wonje Choi, Student Member, IEEE, Zhuo Chen, Janardhan Rao Doppa, Member, IEEE, Partha Pratim Pande, Senior Member, IEEE, Diana Marculescu, Fellow, IEEE, and Radu Marculescu, Fellow, IEEE.

14. IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 25, NO. 11, NOVEMBER 2017. A Low-Power High-Speed Hybrid ADC With Merged Sample-and-Hold and DAC Functions for Efficient Subranging,Time-Interleaved Operation Seyed Ali reza Zahrai, Student Member, IEEE, Marina Zlochisti, Nicolas Le Dortz, Member, IEEE, and Marvin Onabajo, Senior Member, IEEE.

15. IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 25, NO. 11, NOVEMBER 2017. DVFS-Based Long-Term Task Scheduling for Dual-Channel Solar-Powered Sensor Nodes Tongda Wu, Yongpan Liu, Senior Member, IEEE, Daming Zhang, Jinyang Li, Xiaobo Sharon Hu, Fellow, IEEE, Chun Jason Xue, Senior Member, IEEE, and Huazhong Yang, Senior Member, IEEE.